US007667632B2

(12) **United States Patent**
**Baker**

(10) **Patent No.: US 7,667,632 B2**
(45) **Date of Patent: *Feb. 23, 2010**

(54) **QUANTIZING CIRCUITS FOR SEMICONDUCTOR DEVICES**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(22) Filed: **Jun. 15, 2007**

(65) **Prior Publication Data**

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(51) **Int. Cl.**
***H03M 1/12*** (2006.01)

(52) **U.S. Cl.** ..... **341/155**; 341/143; 341/172

(58) **Field of Classification Search** ..... 341/155, 341/143, 141, 172, 162
See application file for complete search history.

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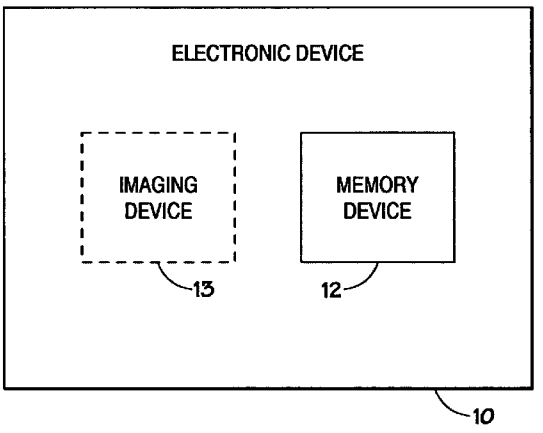
(57) **ABSTRACT**

An electronic device that includes an internal data storage location coupled to an electrical conductor and a quantizing circuit coupled to the internal data storage location via the electrical conductor. In some embodiments, the quantizing circuit includes an analog-to-digital converter having an input and an output, where the input is coupled to the electrical conductor and a digital filter coupled to the output of the analog-to-digital converter.

**30 Claims, 15 Drawing Sheets**



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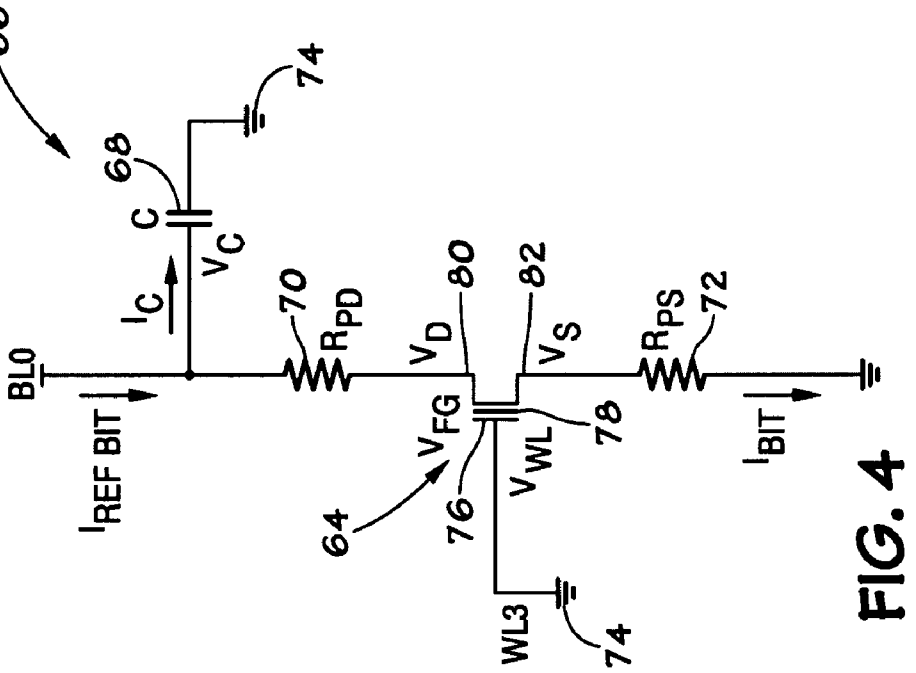

66
74
68
C
$V_C$
$I_C$
70
$R_{PD}$
$V_D$
80
82
$V_S$
$R_{PS}$
72
BL0
$I_{REF\ BIT}$
$V_{FG}$
64
76
$V_{WL}$
78
$I_{BIT}$
WL3
74

FIG. 4

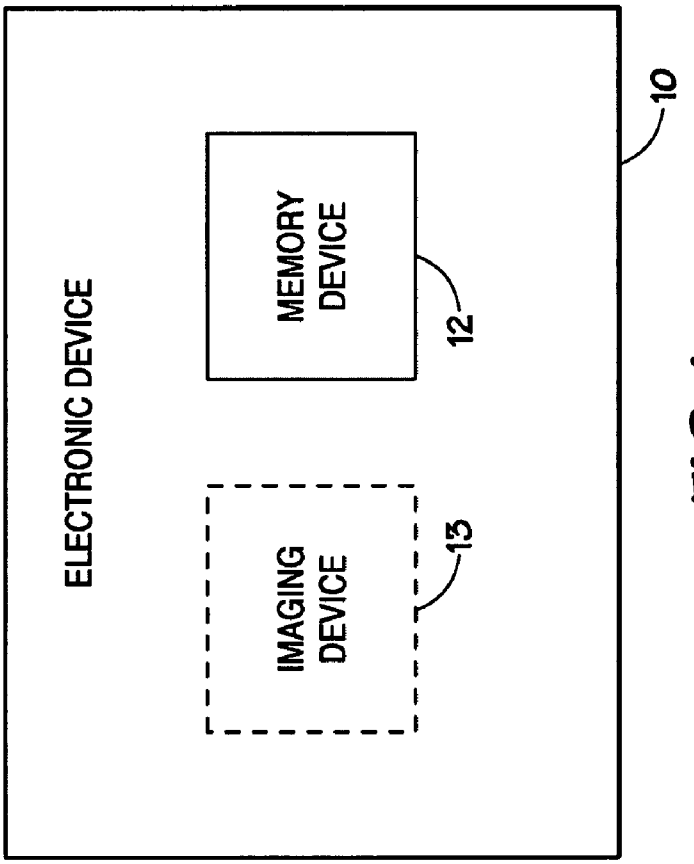

ELECTRONIC DEVICE
MEMORY DEVICE
12
IMAGING DEVICE
13
10

FIG. 1

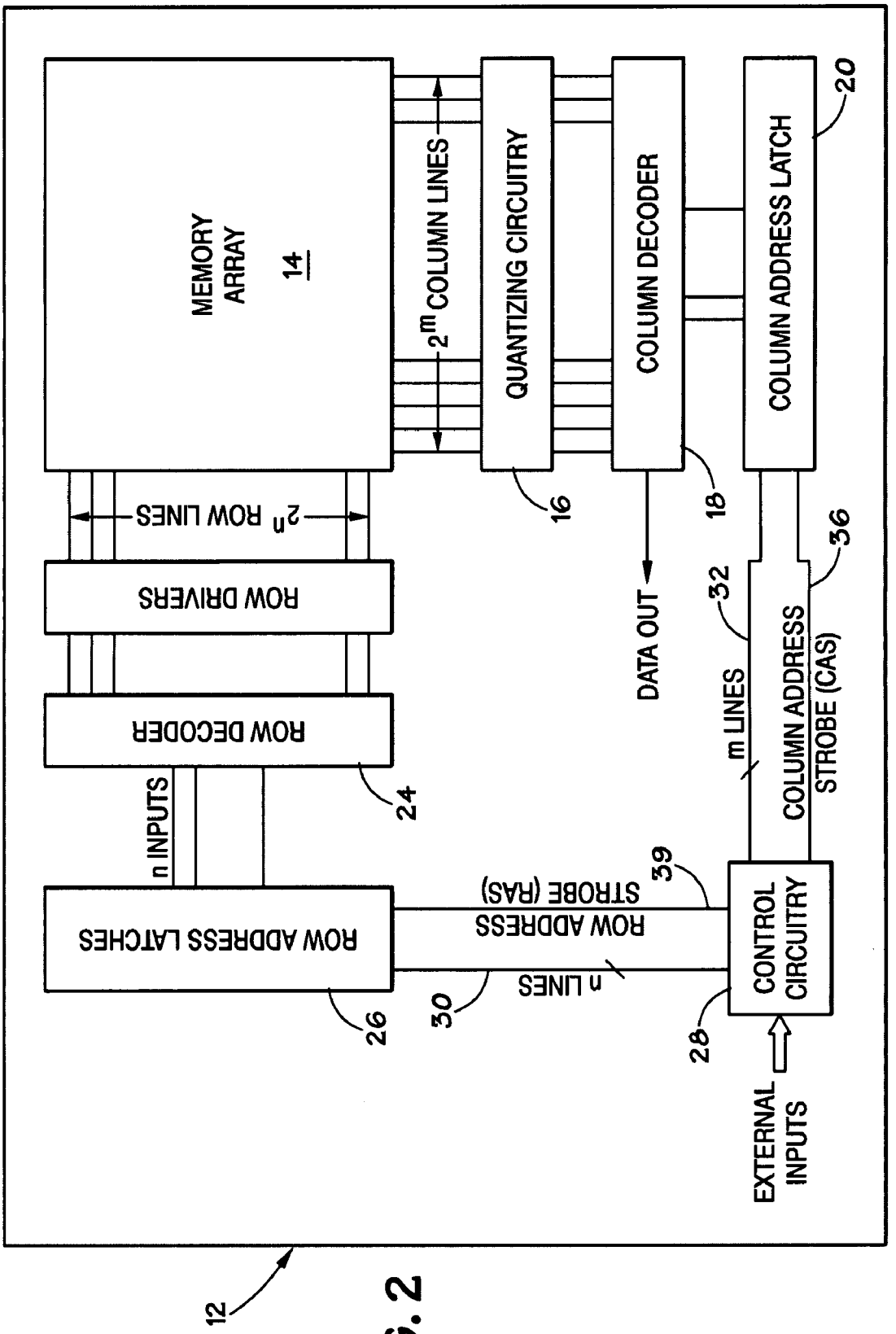

MEMORY ARRAY 14
$2^m$ COLUMN LINES
QUANTIZING CIRCUITRY
COLUMN DECODER
COLUMN ADDRESS LATCH
20
16
18
$2^n$ ROW LINES
ROW DRIVERS
ROW DECODER
24
n INPUTS
ROW ADDRESS LATCHES
26
30
n LINES
ROW ADDRESS STROBE (RAS)
39
CONTROL CIRCUITRY
28
EXTERNAL INPUTS
DATA OUT
32
m LINES
COLUMN ADDRESS STROBE (CAS)
36
12

FIG. 2

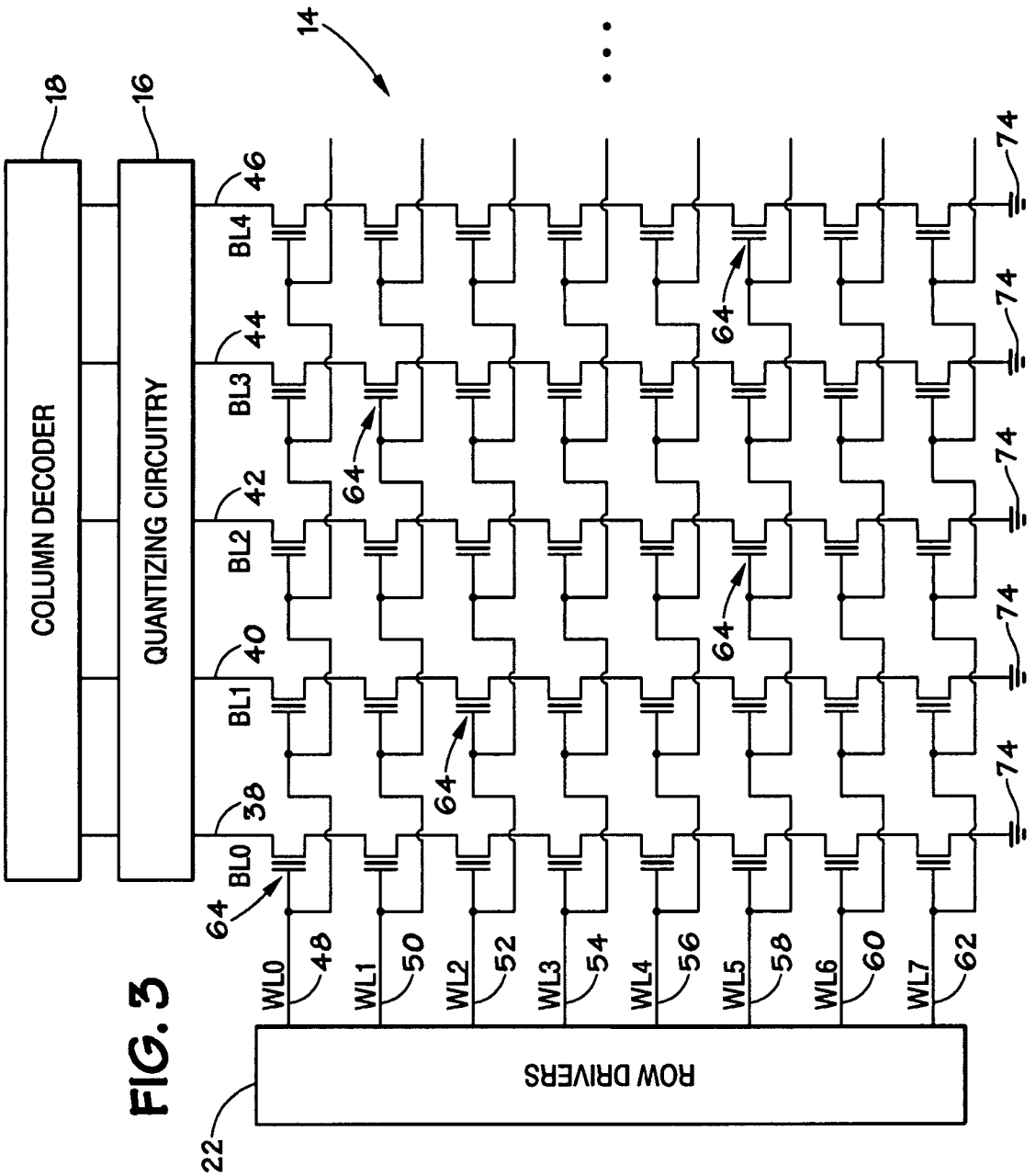

14
18
16
COLUMN DECODER
QUANTIZING CIRCUITRY
BL4
BL3
BL2
BL1
BL0
46
44
42
40
38
64
74
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
48
50
52
54
56
58
60
62
ROW DRIVERS
22

FIG. 3

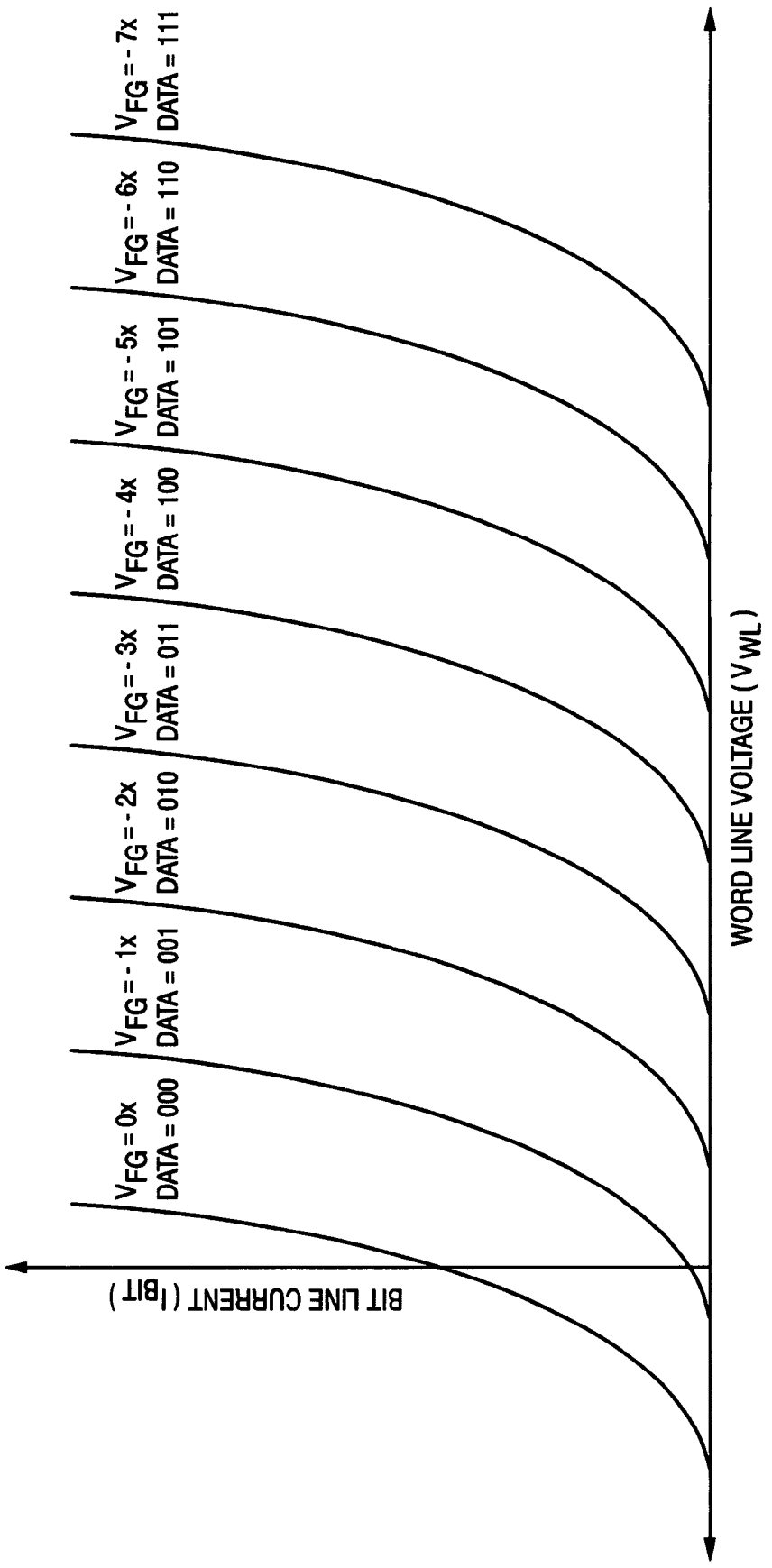

BIT LINE CURRENT ( $I_{BIT}$ )
WORD LINE VOLTAGE ( $V_{WL}$ )
$V_{FG}$ = 0x DATA = 000
$V_{FG}$ = - 1x DATA = 001
$V_{FG}$ = - 2x DATA = 010
$V_{FG}$ = - 3x DATA = 011
$V_{FG}$ = - 4x DATA = 100
$V_{FG}$ = - 5x DATA = 101
$V_{FG}$ = - 6x DATA = 110
$V_{FG}$ = - 7x DATA = 111

FIG. 5

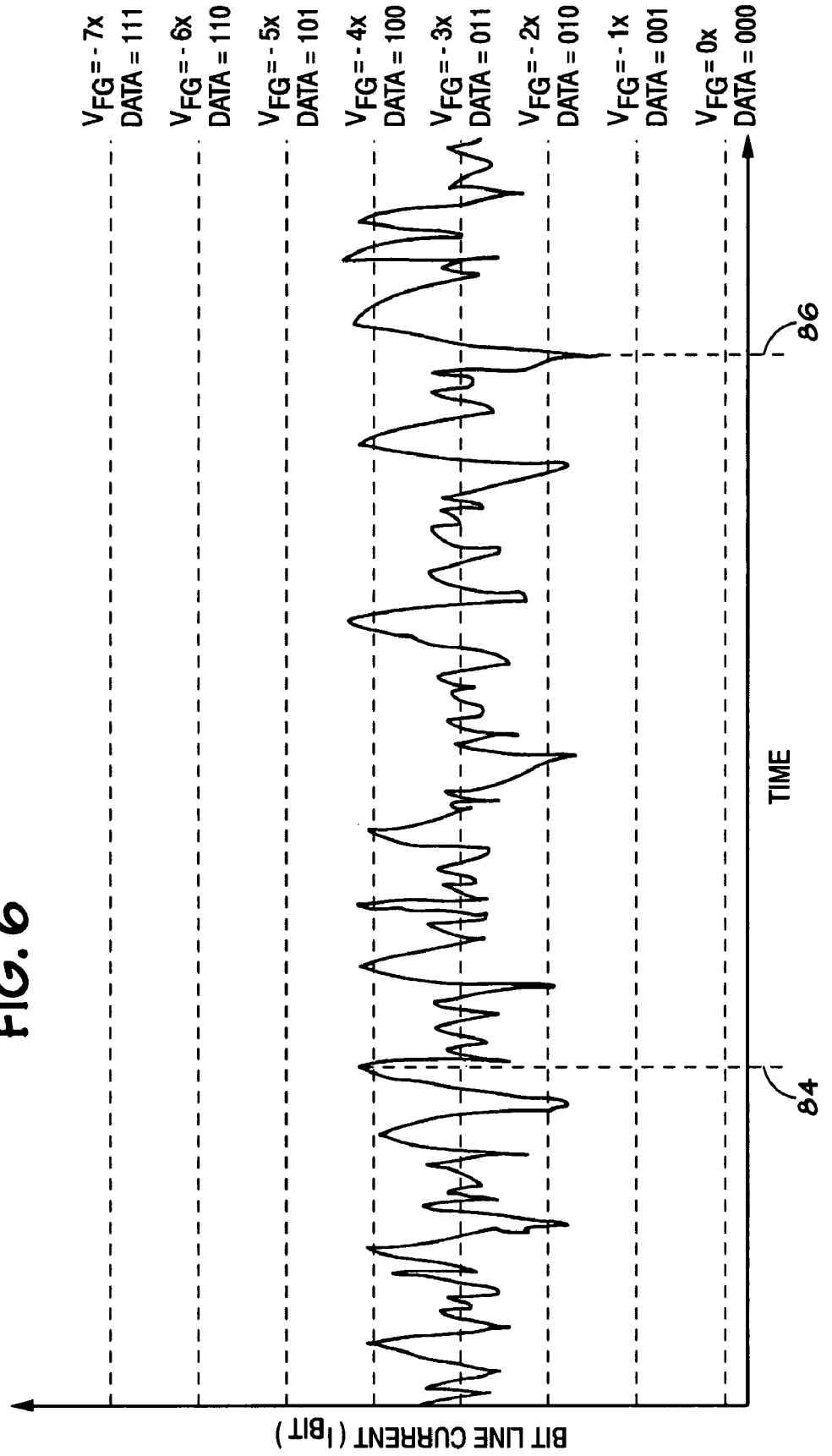

$V_{FG}$ = - 7x
DATA = 111
$V_{FG}$ = - 6x
DATA = 110
$V_{FG}$ = - 5x
DATA = 101
$V_{FG}$ = - 4x
DATA = 100
$V_{FG}$ = - 3x
DATA = 011
$V_{FG}$ = - 2x
DATA = 010
$V_{FG}$ = - 1x
DATA = 001
$V_{FG}$ = 0x
DATA = 000
86
84
TIME
BIT LINE CURRENT ($I_{BIT}$)

FIG. 6

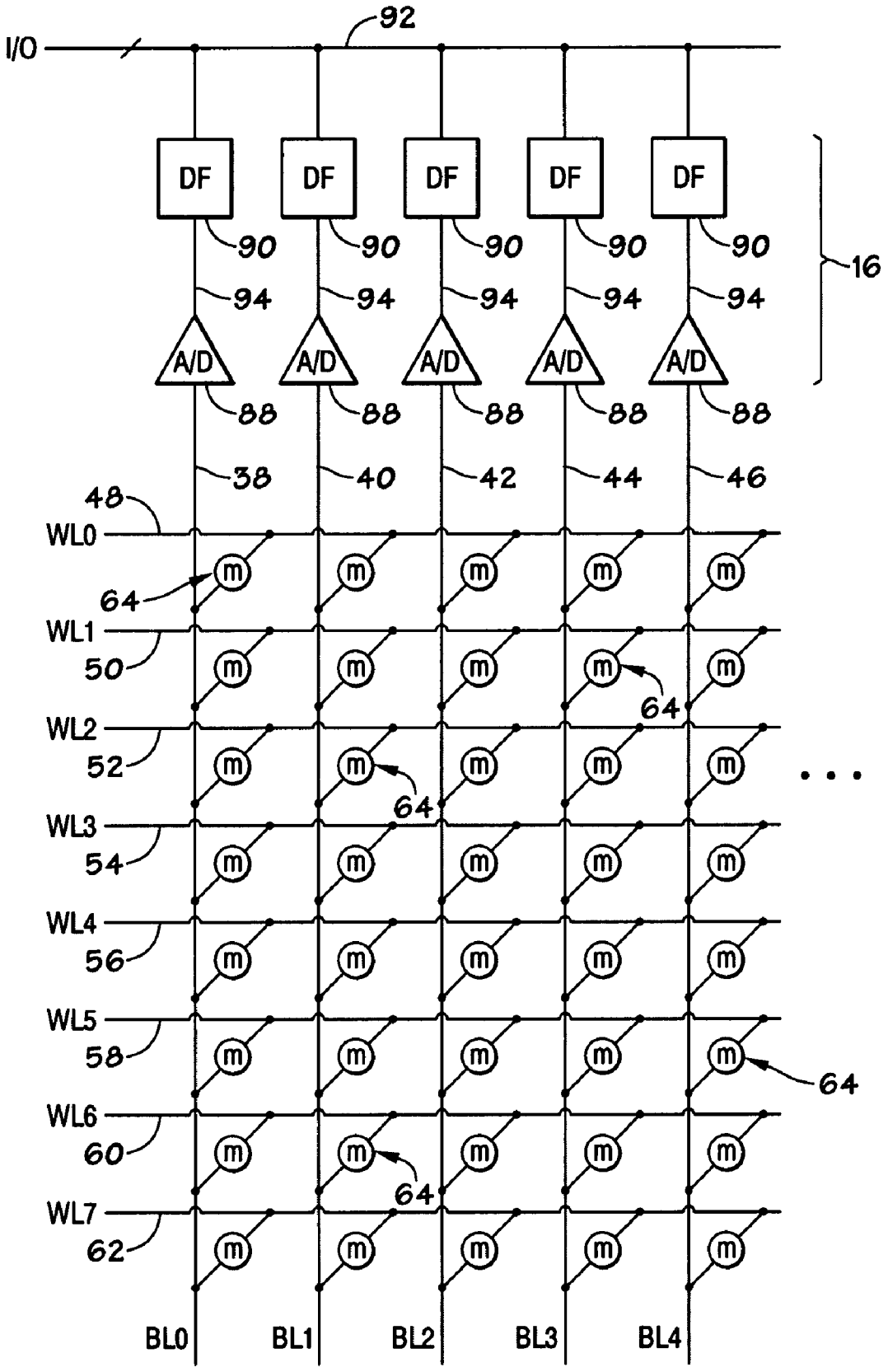

I/O
92
DF
DF
DF
DF
DF
90
90
90
90
90
16
94
94
94
94
94
A/D
A/D
A/D
A/D
A/D
88
88
88
88
88
38
40
42
44
46
48
WL0
64
WL1
50
WL2
52
WL3
54
WL4
56
WL5
58
WL6
60
WL7
62
BL0
BL1
BL2
BL3
BL4

FIG. 7

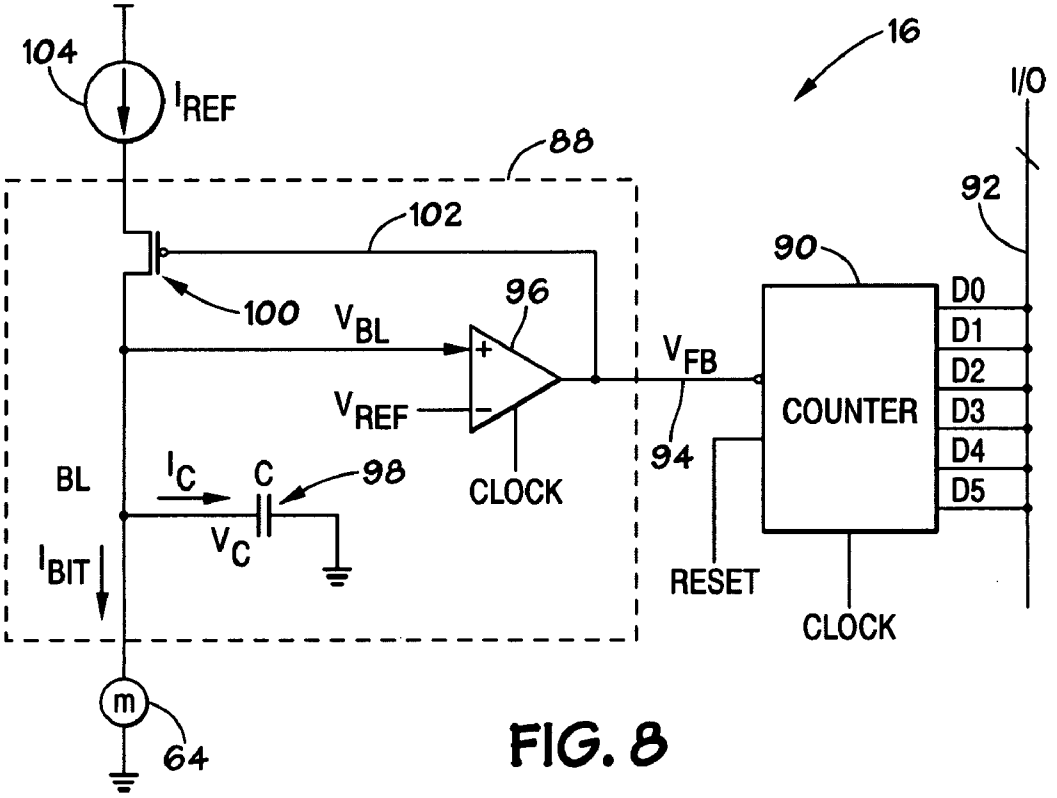

104
$I_{REF}$
16
I/O
88
92
102
90
100
$V_{BL}$
96
D0
D1
D2
D3
D4
D5
$V_{FB}$
$V_{REF}$
COUNTER
BL
$I_C$
C
98
CLOCK
94
$V_C$
$I_{BIT}$
RESET
CLOCK
m
64

FIG. 8

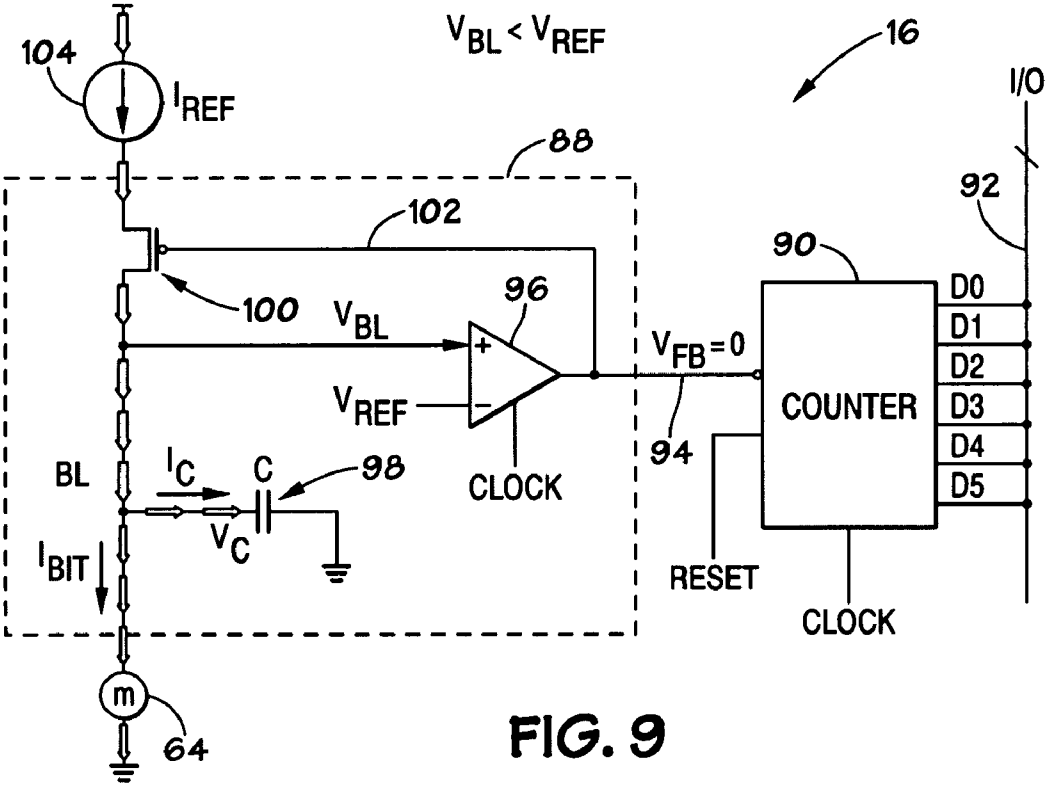

$V_{BL} < V_{REF}$
104
$I_{REF}$
16
I/O
88
92
102
90
100
$V_{BL}$
96
D0
D1
D2
D3
D4
D5
$V_{FB}=0$
$V_{REF}$
COUNTER
BL
$I_C$
C
98
CLOCK
94
$V_C$
$I_{BIT}$
RESET
CLOCK
m
64

FIG. 9

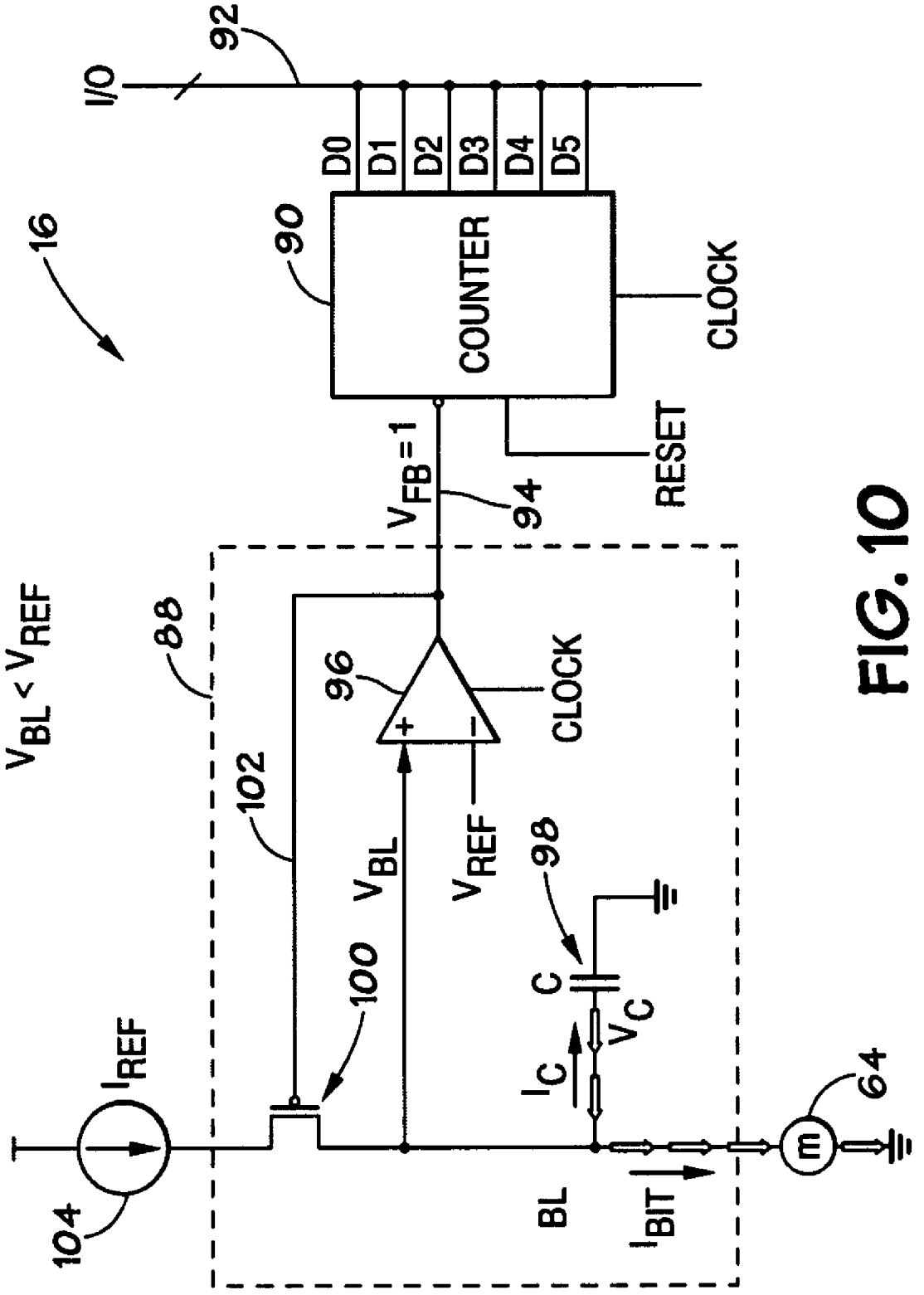

I/O
92
D0
D1
D2
D3
D4
D5
16
90
COUNTER
CLOCK
RESET
$V_{FB}=1$
94
$V_{BL} < V_{REF}$
88
96
CLOCK
102
$V_{BL}$
$V_{REF}$
98
100
C
$V_C$
$I_C$
$I_{REF}$
104
BL
$I_{BIT}$
64

FIG. 10

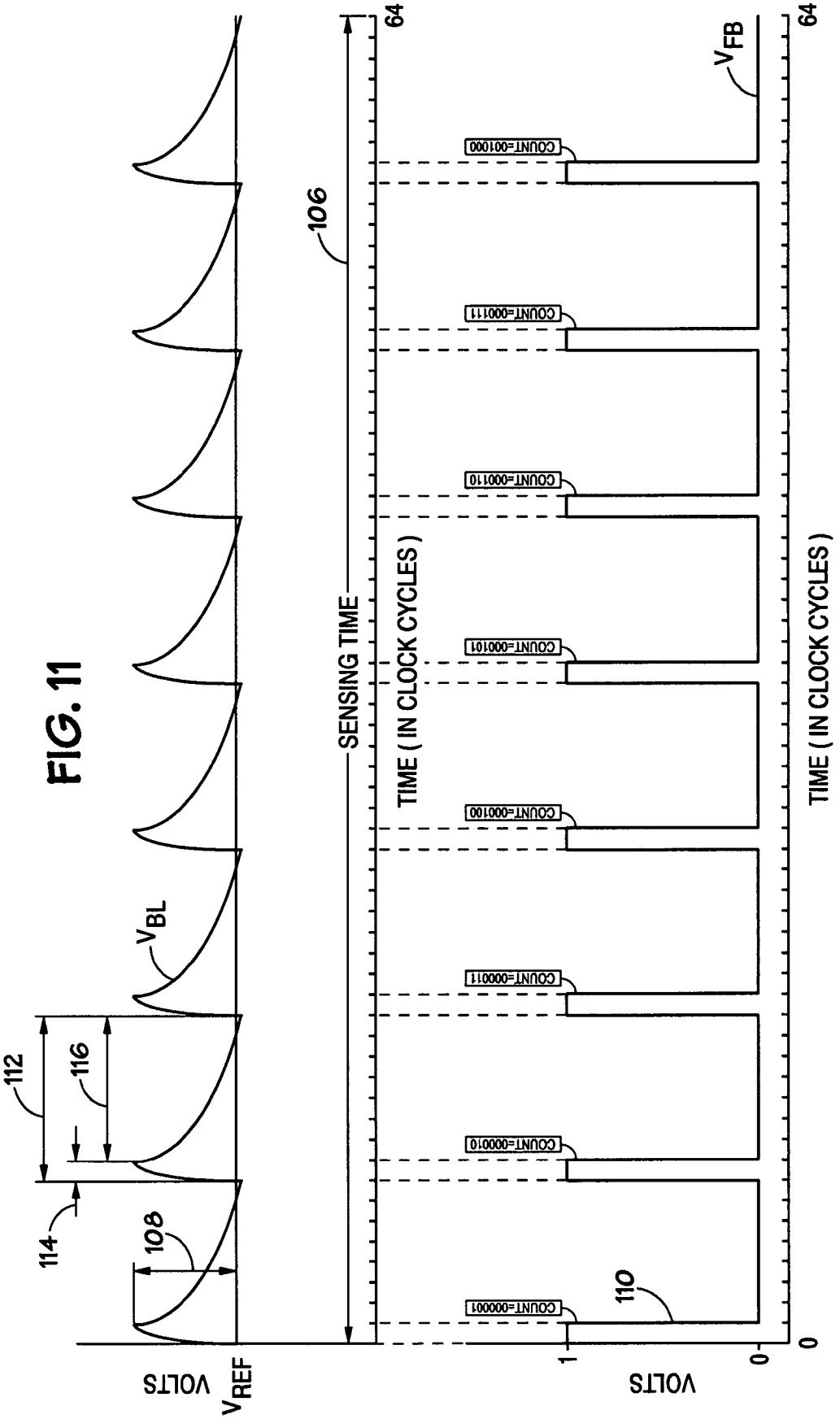

VOLTS
$V_{REF}$
$V_{BL}$
112
116
114
108
106
SENSING TIME
TIME ( IN CLOCK CYCLES )
64
COUNT=000001
COUNT=000010
COUNT=000011
COUNT=000100
COUNT=000101
COUNT=000110
COUNT=000111
COUNT=001000
110
$V_{FB}$
1
0
VOLTS
64
0
TIME ( IN CLOCK CYCLES )

FIG. 11

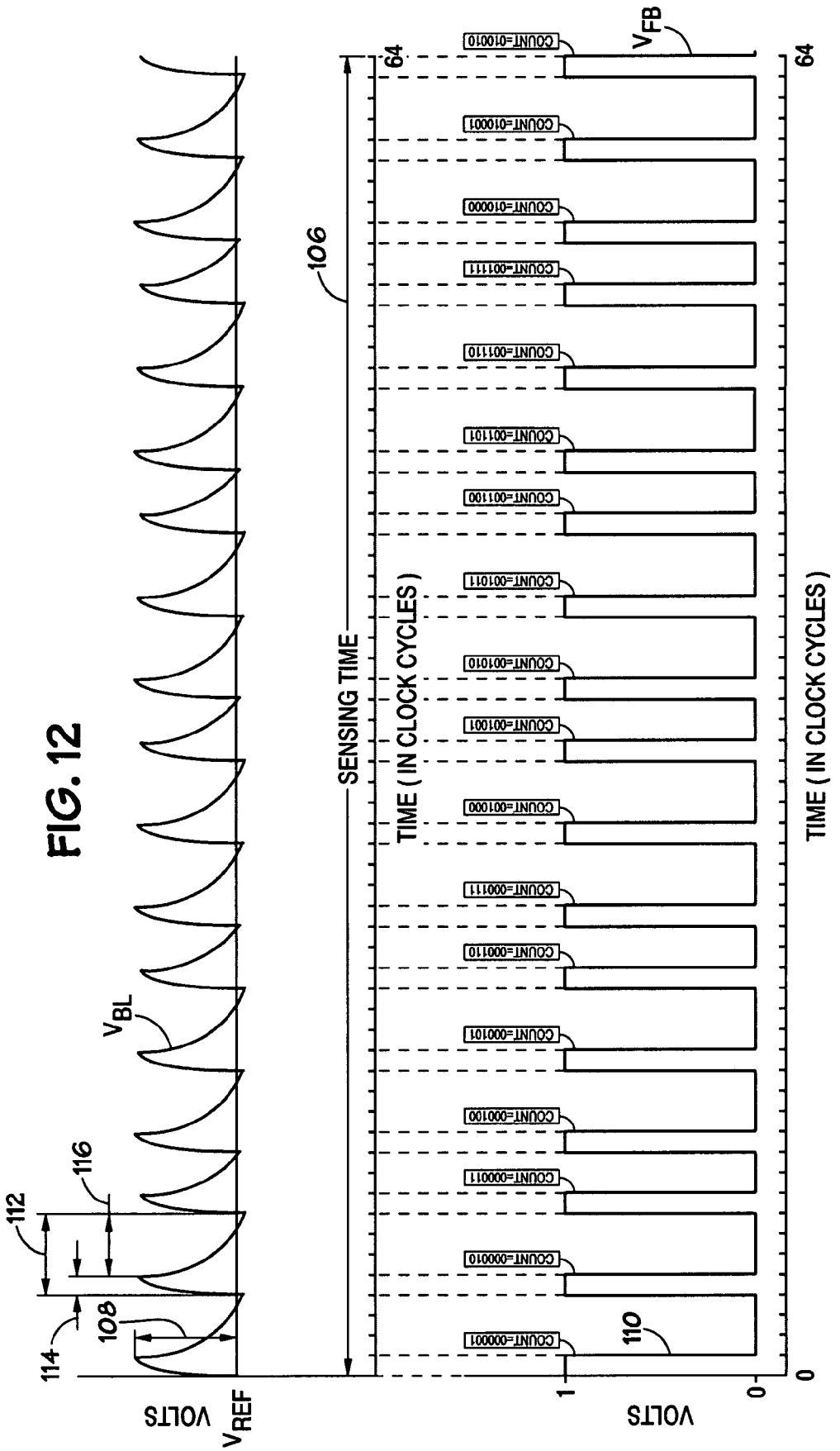

$V_{FB}$
64
COUNT=010010
COUNT=010001
COUNT=010000
COUNT=001111
COUNT=001110
COUNT=001101
COUNT=001100
COUNT=001011
COUNT=001010
COUNT=001001
COUNT=001000
COUNT=000111
COUNT=000110
COUNT=000101
COUNT=000100
COUNT=000011
COUNT=000010
COUNT=000001
106
SENSING TIME
TIME ( IN CLOCK CYCLES )
110
1
0
VOLTS
0
64
TIME ( IN CLOCK CYCLES )
$V_{BL}$
116
112
108
114
VOLTS
$V_{REF}$

FIG. 12

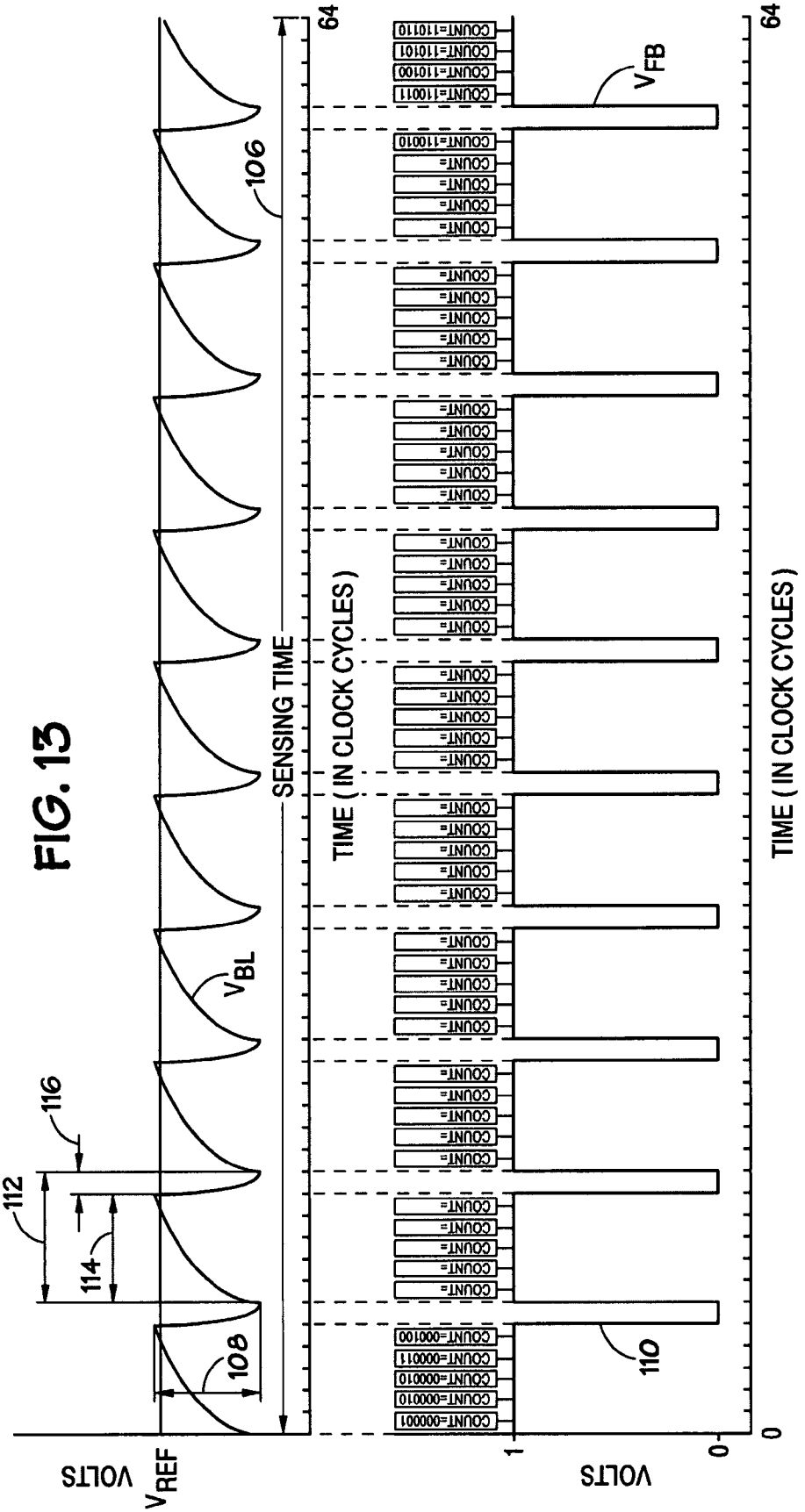

64
106
SENSING TIME
TIME ( IN CLOCK CYCLES )
$V_{BL}$
116
112
114
108
VOLTS
$V_{REF}$
COUNT=000001
COUNT=000010
COUNT=000011
COUNT=000100
COUNT=110011
COUNT=110100
COUNT=110101
COUNT=110110
$V_{FB}$
110
1
0
VOLTS
TIME ( IN CLOCK CYCLES )
64
0

FIG. 13

FIG. 14

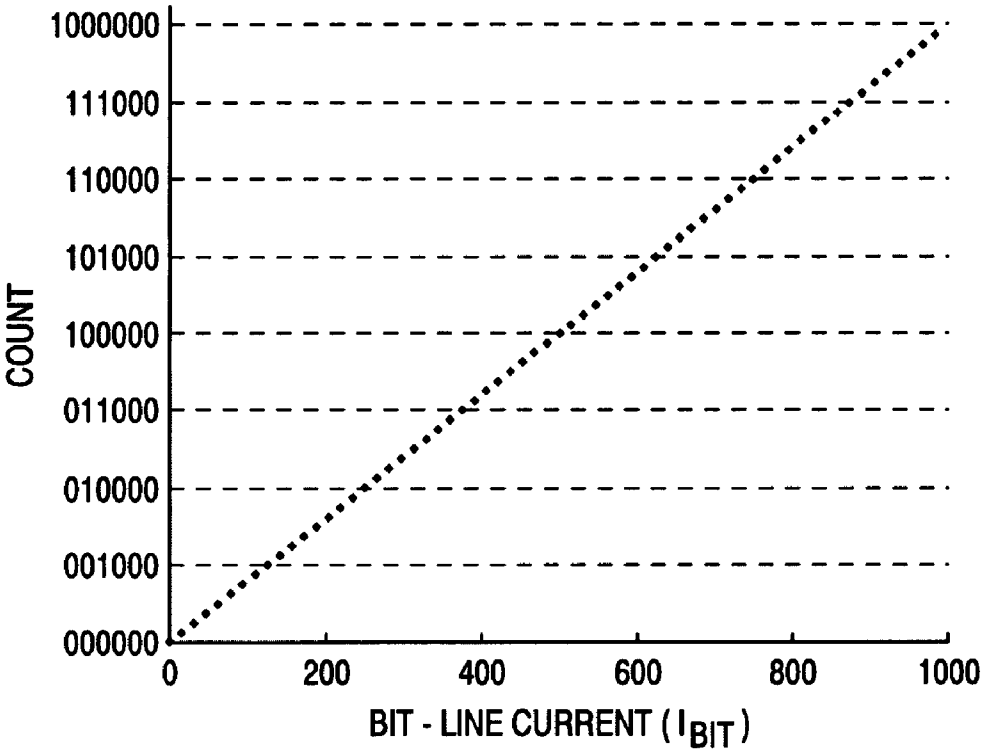

1000000
111000
110000
101000
100000
011000
010000
001000
000000
COUNT
0
200
400
600
800
1000
BIT - LINE CURRENT ( $I_{BIT}$ )

FIG. 15

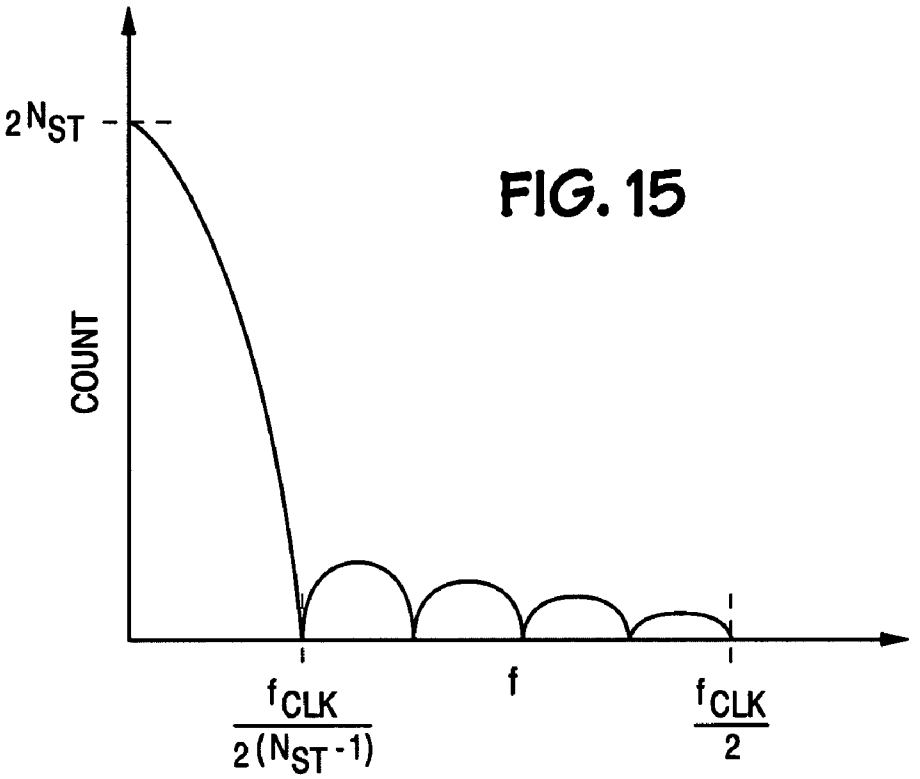
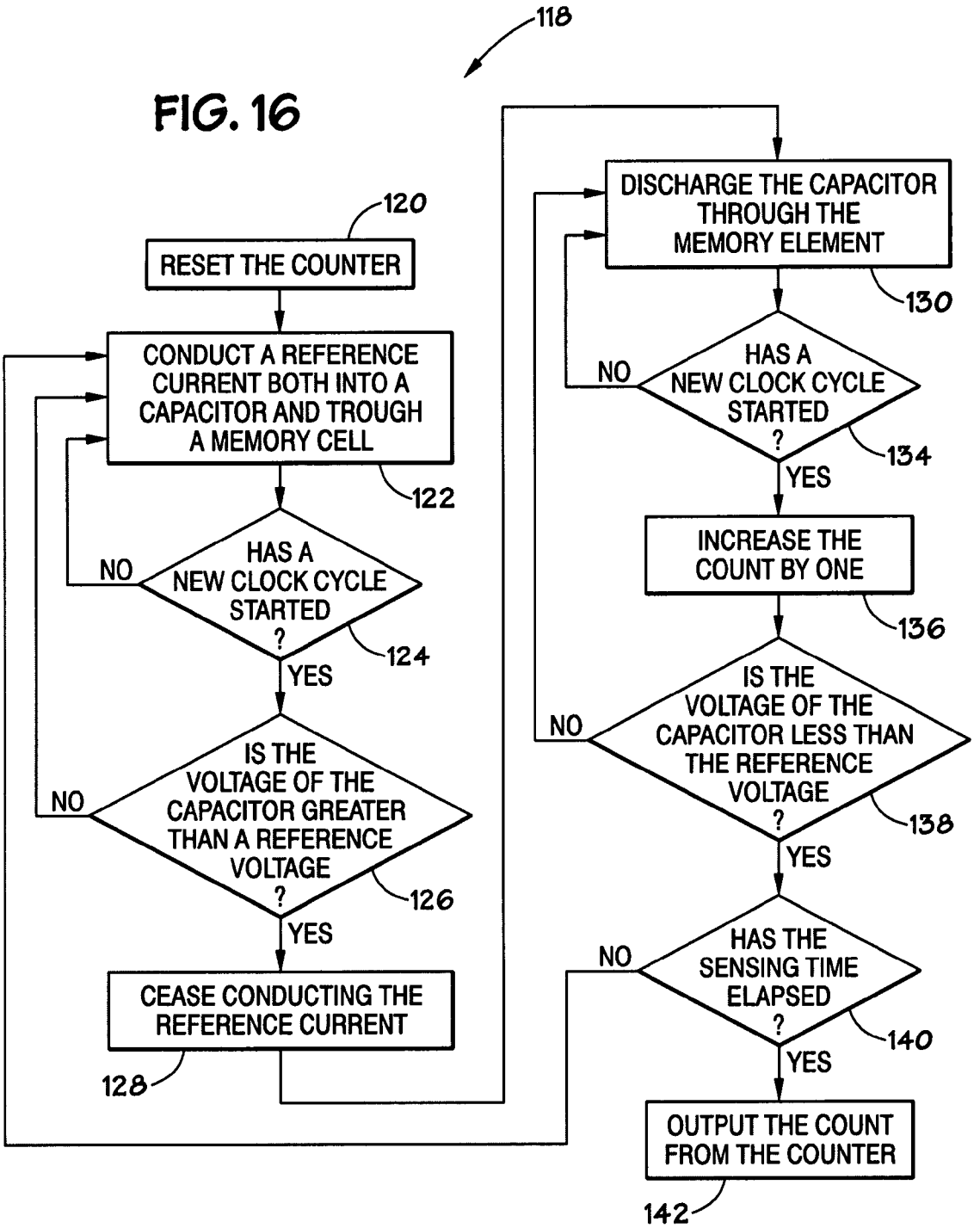

$2^{N_{ST}}$
COUNT
$\frac{f_{CLK}}{2(N_{ST}-1)}$
f
$\frac{f_{CLK}}{2}$

FIG. 16


118
120
RESET THE COUNTER
CONDUCT A REFERENCE CURRENT BOTH INTO A CAPACITOR AND TROUGH A MEMORY CELL
122
HAS A NEW CLOCK CYCLE STARTED ?
NO
124
YES
IS THE VOLTAGE OF THE CAPACITOR GREATER THAN A REFERENCE VOLTAGE ?
NO
126
YES
CEASE CONDUCTING THE REFERENCE CURRENT
128
DISCHARGE THE CAPACITOR THROUGH THE MEMORY ELEMENT
130
HAS A NEW CLOCK CYCLE STARTED ?
NO
134
YES
INCREASE THE COUNT BY ONE
136
IS THE VOLTAGE OF THE CAPACITOR LESS THAN THE REFERENCE VOLTAGE ?
NO
138
YES
HAS THE SENSING TIME ELAPSED ?
NO
140
YES
OUTPUT THE COUNT FROM THE COUNTER
142

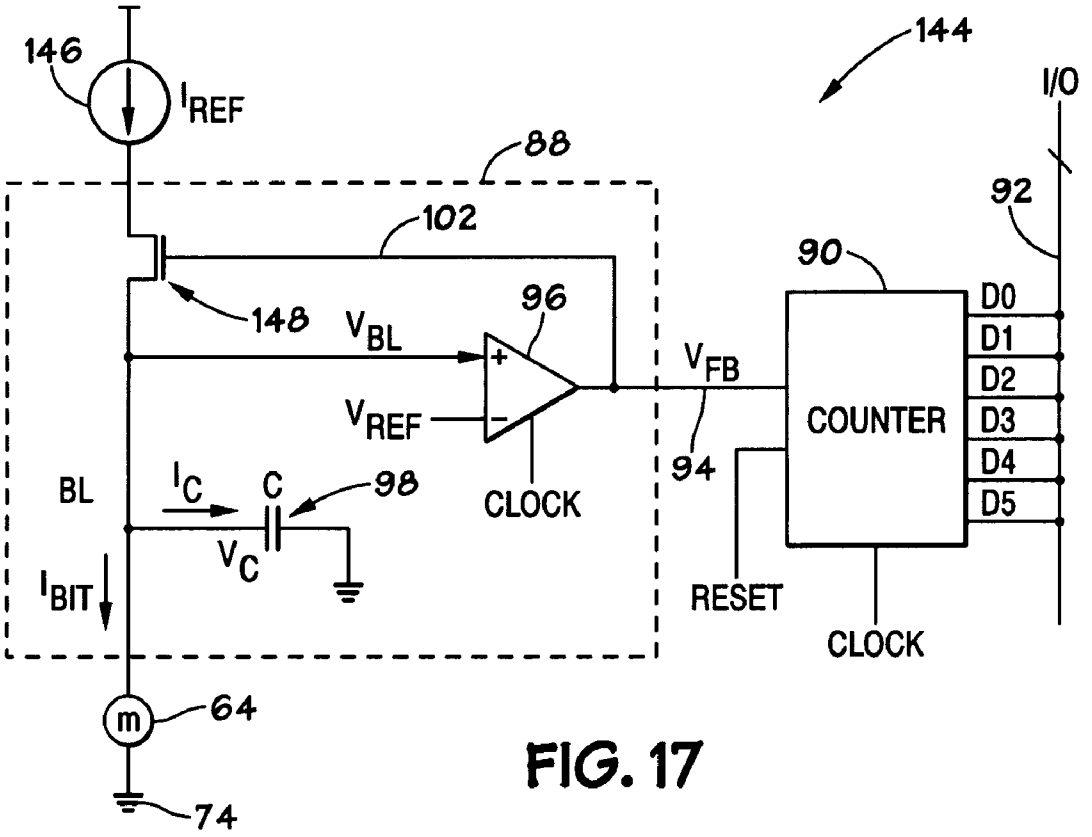

146
$I_{REF}$
144
I/O
88
92
102
90
148
$V_{BL}$
96
D0
D1
D2
D3
D4
D5
$V_{FB}$
$V_{REF}$
COUNTER
BL
$I_C$
C
98
94
CLOCK
$V_C$
RESET
$I_{BIT}$
CLOCK
m
64
74

FIG. 17

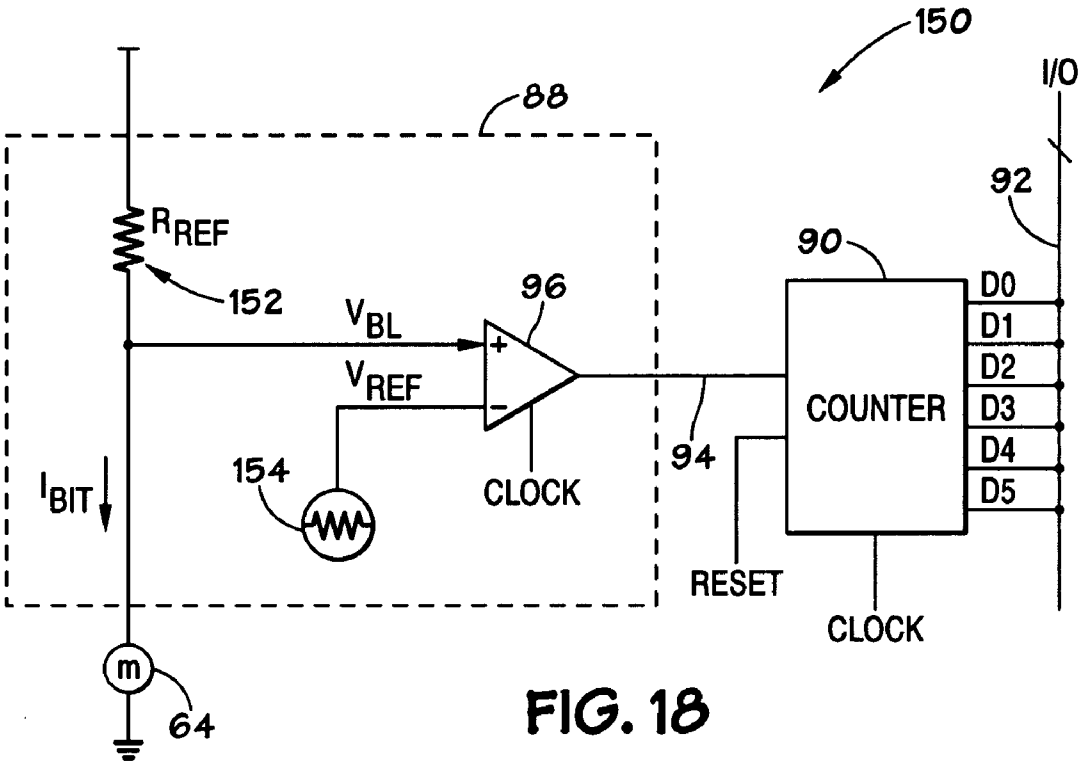

150
I/O
88
92
$R_{REF}$
90
152
$V_{BL}$
96
D0
D1
D2
D3
D4
D5
$V_{REF}$
COUNTER
154
94
$I_{BIT}$
CLOCK
RESET
CLOCK
m
64

FIG. 18

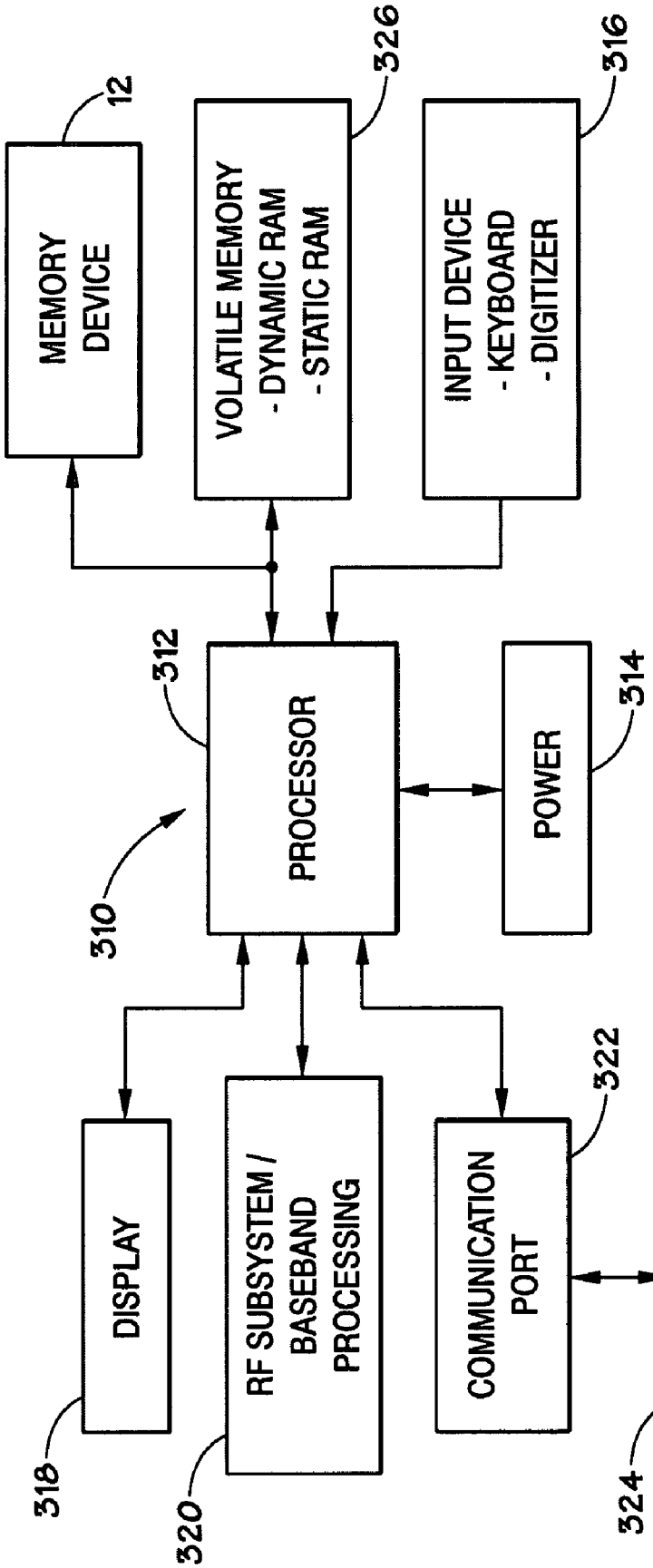

MEMORY DEVICE
12
VOLATILE MEMORY
- DYNAMIC RAM
- STATIC RAM
326
INPUT DEVICE
- KEYBOARD
- DIGITIZER
316
PROCESSOR
312
310
POWER
314
DISPLAY
318
RF SUBSYSTEM / BASEBAND PROCESSING
320
COMMUNICATION PORT
322
PERIPHERAL
324

FIG. 19

# QUANTIZING CIRCUITS FOR SEMICONDUCTOR DEVICES

## BACKGROUND

1. Field of the Invention

Embodiments of the present invention relate generally to sensing devices, and, more specifically, to quantizing devices for sensing multi-bit memory elements or multi-level image sensors.

1. Description of the Related Art

Generally, memory devices include an array of memory elements and associated sense amplifiers. The memory elements store data, and the sense amplifiers read the data from the memory elements. To read data, for example, a current is passed through the memory element, and the current or a resulting voltage is measured by the sense amplifier. Conventionally, the sense amplifier measures the current or voltage by comparing it to a reference current or voltage. Depending on whether the current or voltage is greater than the reference, the sense amplifier outputs a value of one or zero. That is, the sense amplifier quantizes or digitizes the analog signal from the memory element into one of two logic states.

Many types of memory elements are capable of assuming more than just two states. That is, some memory elements are capable of multi-bit storage. For instance, rather than outputting either a high or low voltage, the memory element may output four or eight different voltage levels, each level corresponding to a different data value. However, conventional sense amplifiers often fail to distinguish accurately between the additional levels because the difference between the levels (e.g., a voltage difference) in a multi-bit memory element is often smaller than the difference between the levels in a single-bit memory element. Thus, conventional sense amplifiers often cannot read multi-bit memory elements. This problem may be increased as high performance multi-bit memory elements become increasingly dense, thereby reducing the size of the memory elements and the difference between the levels (e.g., voltage) to be sensed by the sense amplifiers.

A variety of factors may tend to prevent the sense amplifier from discerning small differences in the levels of a multi-bit memory element. For instance, noise in the power supply, ground, and reference voltage may cause an inaccurate reading of the memory element. The noise may have a variety of sources, such as temperature variations, parasitic signals, data dependent effects, and manufacturing process variations. This susceptibility to noise often leads a designer to reduce the number of readable states of the memory element, which tends to reduce memory density and increase the cost of memory.

Conventional sense amplifiers present similar problems in imaging devices. In these devices, an array of light sensors output a current or voltage in response to light impinging upon the sensor. The magnitude of the current or voltage typically depends upon the intensity of the light. Thus, the capacity of the sense amplifier to accurately convert the current or voltage into a digital signal may determine, in part, the fidelity of the captured image. Consequently, noise affecting the sense amplifier may diminish the performance of imaging devices.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an electronic device in accordance with an embodiment of the present invention;

FIG. **2** illustrates a memory device in accordance with an embodiment of the present invention;



FIG. **3** illustrates a memory array in accordance with an embodiment of the present invention;

FIG. **4** illustrates a memory element in accordance with an embodiment of the present invention;

FIG. **5** illustrates I-V traces of memory elements storing different values, in accordance with an embodiment of the present invention;

FIG. **6** illustrates noise in the bit-line current during a read operation, in accordance with an embodiment of the present invention;

FIG. **7** illustrates a quantizing circuit in accordance with an embodiment of the present invention;

FIG. **8** illustrates a delta-sigma sensing circuit in accordance with an embodiment of the present invention;

FIGS. **9** and **10** illustrate current flow during operation of the quantizing circuit of FIG. **8**;

FIGS. **11-13** illustrate voltages in the quantizing circuit of FIG. **8** when sensing small, medium, and large currents, respectively;

FIG. **14** is a graph of bit-line current versus counter output for the quantizing circuit of FIG. **8**;

FIG. **15** is a graph of the frequency response of the quantizing circuit of FIG. **8**;

FIG. **16** is flow chart of a read operation in accordance with an embodiment of the present invention;

FIG. **17** is a second example of a quantizing circuit in accordance with an alternate embodiment of the present invention;

FIG. **18** is a third example of a quantizing circuit in accordance with an alternate embodiment of the present invention;

FIG. **19** is an example of a system that includes the memory device of FIG. **2** in accordance with an embodiment of the present invention.

## DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Various embodiments of the present invention are described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

Some of the subsequently described embodiments may address one or more of the problems with conventional sense amplifiers discussed above. Some embodiments include a quantizing circuit configured to detect small differences in voltages and/or currents. As explained below, the quantizing circuit may sample the measured electrical parameter on multiple occasions and filter, e.g., average or sum, the samples to reduce the impact of noise. As a result, in some embodiments, the quantizing circuit may resolve small differences between voltage or current levels in multi-bit memory elements and/or light sensors, which may allow circuit designers to increase the number of bits stored per memory element and/or the sensitivity of an imaging device.

The following description begins with an overview of examples of systems that employ quantizing circuits in accordance with embodiments of the present invention, and the

problems within these systems that may be addressed by the quantizing circuits as described with reference to FIGS. **1-7**. Then, a specific example of a quantizing circuit is described with reference to FIGS. **8-16**. Finally, design considerations and other examples of quantizing circuits are described with reference to FIGS. **17** and **18**.

FIG. **1** depicts an electronic device **10** that may be fabricated and configured in accordance with one or more of the present embodiments. The illustrated electronic device **10** includes a memory device **12** that, as explained further below, may include multi-bit memory elements and quantizing circuits. Alternatively, or additionally, the electronic device **10** may include an imaging device **13** having the quantizing circuits.

Myriad devices may embody one or more of the present techniques. For example, the electronic device **10** may be a storage device, a communications device, an entertainment device, an imaging system, or a computer system, such as a personal computer, a server, a mainframe, a tablet computer, a palm-top computer, or a laptop.

FIG. **2** depicts a block diagram of an embodiment of the memory device **12**. The illustrated memory device **12** may include a memory array **14**, a quantizing circuit **16**, a column decoder **18**, a column address latch **20**, row drivers **22**, a row decoder **24**, row address latches **26**, and control circuitry **28**. As described below with reference to FIG. **3**, the memory array **14** may include a matrix of memory elements arranged in rows and columns. As will be appreciated, the imaging device **13** (FIG. **1**) may include similar features except that in the case of an imaging device **13**, the memory array **14** will include a matrix of imaging elements, such as complementary-metal-oxide semiconductor (CMOS) imaging elements.

When accessing the memory elements, the control circuitry may receive a command to read from or write to a target memory address. The control circuitry **28** may then convert the target address into a row address and a column address. In the illustrated embodiment, the row address bus **30** transmits the row address to the row address latches **26**, and a column address bus **32** transmits column address to the column address latches **20**. After an appropriate settling time, a row address strobe (RAS) signal **34** (or other controlling clock signal) may be asserted by the control circuitry **28**, and the row address latches **26** may latch the transmitted row address. Similarly, the control circuitry **28** may assert a column address strobe **36**, and the column address latches **20** may latch the transmitted column address.

Once row and column addresses are latched, the row decoder **24** may determine which row of the memory array **14** corresponds to the latched row address, and the row drivers **22** may assert a signal on the selected row. Similarly, the column decoder **18** may determine which column of the memory array **14** corresponds with the latched column address, and the quantizing circuit **16** may sense a voltage or current on the selected column. Additional details of reading and writing are described below.

FIG. **3** illustrates an example of a memory array **14**. The illustrated memory array **14** includes a plurality of bit-lines **38**, **40**, **42**, **44**, and **46** (also referred to as BL**0**-BL**4**) and a plurality of word-lines **48**, **50**, **52**, **54**, **56**, **58**, **60**, and **62** (also referred to as WL**0**-WL**7**). These bit-lines and word-lines are electrical conductors. The memory array **14** further includes a plurality of memory elements **64**, each of which may be arranged to intersect one of the bit-lines and one of the word-lines. In other embodiments, imaging elements may be disposed at each of these intersections. The memory elements and imaging elements may be referred to generally as internal data storage locations, i.e., devices configured to convey data, either stored or generated by a sensor, when accessed by a sensing circuit, such as the quantizing circuits discussed below. The internal data storage locations may be formed on an integrated semiconductor device that also includes the other components of the memory device **12** (or imaging device **13**).

In some embodiments, the illustrated memory elements **64** are flash memory devices. The operation of the flash memory elements is described further below with reference to the FIGS. **4** and **5**. It should be noted that, in other embodiments, the memory elements **64** may include other types of volatile or nonvolatile memory. For example, the memory elements **64** may include a resistive memory, such as a phase change memory or magnetoresistive memory. In another example, the memory elements **64** may include a capacitor, such as a stacked or trench capacitor. Some types of memory elements **64** may include an access device, such as a transistor or a diode associated with each of the memory elements **64**, or the memory elements **64** may not include an access device, for instance in a cross-point array.

FIG. **4** illustrates a circuit **66** that models the operation of an arbitrarily selected memory element **64**, which is disposed at the intersection of WL**3** and BL**0**. This circuit **66** includes a capacitor **68**, a pre-drain resistor **70** ($R_{PD}$), a post-source resistor **72** ($R_{PS}$), and a ground **74**. The resistors **70** and **72** model the other devices in series the memory element **64** being sensed. The illustrated memory element **64** includes a gate **76**, a floating gate **78**, a drain **80**, and a source **82**. In the circuit **66**, the drain **80** and source **82** are disposed in series between the pre-drain resistor **70** and the post-source resistor **72**. The gate **76** is coupled to WL**3**. The pre-drain resistor **70**, the drain **80**, the source **82**, and the post-source resistor **72** are disposed in series on the bit-line BL**0**. The capacitor **68**, which models the capacitance of the bit-line, has one plate coupled to ground **74** and another plate coupled to the bit-line BL**0**, in parallel with the memory elements **64**.

Several of the components of the circuit **66** represent phenomenon affecting the memory elements **64** during operation. The pre-drain resistor **70** generally represents the drain-to-bitline resistance of the memory elements **64** coupled to the bit-line above (i.e., up current from) WL**3** when these memory elements **64** are turned on, (e.g., during a read operation). Similarly, the post source resistor **72** generally corresponds to the source-to-ground resistance of the memory elements **64** coupled to the bit-line below WL**3** when these memory element **64** is selected. The circuit **66** models electrical phenomena associated with reading the memory elements **64** at the intersection of WL**3** and BL**0**.

The operation of the memory elements **64** will now be briefly described with reference to FIGS. **4** and **5**. FIG. **5** illustrates one potential relationship between the bit-line current ($I_{Bit}$), the word-line voltage ($V_{WL}$), and the voltage of the floating gate **78** ($V_{FG}$). As illustrated by FIG. **5**, $V_{FG}$ affects the response of the memory element **64** to a given $V_{WL}$. Decreasing the voltage of the floating gate shifts the I-V curve of the memory elements **64** to the right. That is, the relationship between the bit-line current and a word-line voltage depends on the voltage of the floating gate **78**. The memory elements **64** may store and output data by exploiting this effect.

To write data to the memory elements **64**, a charge corresponding to the data may be stored on the floating gate **78**. The charge of the floating gate **78** may be modified by applying voltages to the source **82**, drain **80**, and/or gate **76** such that the resulting electric fields produce phenomenon like Fowler-Northam tunneling and/or hot-electron injection near the floating gate **78**. Initially, the memory elements **64** may be

erased by manipulating the word-line voltage to drive electrons off of the floating gate **78**. In some embodiments, an entire column or block of memory elements **64** may be erased generally simultaneously. Once the memory elements **64** are erased, the gate **76** voltage may be manipulated to drive a charge onto the floating gate **78** that is indicative of a data value. After the write operation ends, the stored charge may remain on the floating gate **78** (i.e., the memory elements **64** may store data in a nonvolatile fashion).

As illustrated by FIG. **5**, the value stored by the memory element **64** may be read by applying a voltage, $V_{WL}$, to the gate **76** and measuring a resulting bit-line current, $I_{Bit}$. Each of the I-V traces depicted by FIG. **5** correspond to a different charge stored on the floating gate, $V_{FG}$, which should not be confused with the voltage that is applied to the gate, $V_{WL}$. The difference in floating gate **70** voltage, $V_{FG}$, between each I-V trace is an arbitrarily selected scaling factor "x." The illustrated I-V traces correspond to eight-different data values stored by the memory element **64**, with a $V_{FG}$ of 0x representing a binary data value of 000, a $V_{FG}$ of 1x representing a binary data value of 001, and so on through $V_{FG}$ of 7x, which represents a binary data value of 111. Thus, by applying a voltage to the gate **76** and measuring the resulting bit-line current, the charge stored on the floating gate **78** may be measured, and the stored data may be read.

The accuracy with which the bit-line current is sensed may affect the amount of data that a designer attempts to store in each memory element **64**. For example, in a system with a low sensitivity, a single bit may be stored on each memory element **64**. In such a system, a floating gate voltage $V_{FG}$ of 0x may correspond to a value of 0, and a floating gate voltage $V_{FG}$ of −7x may correspond to a value of one. Thus, the difference in floating gate voltages $V_{FG}$ corresponding to different data values may be relatively large, and the resulting differences and bit-line currents for different data values may also be relatively large. As a result, even low-sensitivity sensing circuitry may discern these large differences in bit-line current during a read operation. In contrast, high-sensitivity sensing circuitry may facilitate storing more data in each memory element **64**. For instance, if the sensing circuitry can distinguish between the eight different I-V traces depicted by FIG. **5**, then the memory elements **64** may store three bits. That is, each of the eight different charges stored on the floating gate **78** may correspond to a different three-bit value: 000, 001, 010, 011, 100, 101, 110, or 111. Thus, circuitry that precisely measures the bit-line current $I_{BIT}$ may allow a designer to increase the amount of data stored in each memory element **64**.

However, as mentioned above, a variety of effects may interfere with accurate measurement of the bit-line current. For instance, the position of the memory elements **64** along a bit-line may affect $R_{PD}$ and $R_{PS}$, which may affect the relationship between the word-line voltage $V_{WL}$ and the bit-line current $I_{BIT}$ To illustrate these effects, FIG. **6** depicts noise on the bit-line while reading from the memory element **64**. As illustrated, noise in the bit-line current $I_{BIT}$ may cause the bit-line current $I_{BIT}$ to fluctuate. Occasionally, the fluctuation may be large enough to cause the bit-line current $I_{BIT}$ to reach a level that corresponds with a different stored data value, which could cause the wrong value to be read from the memory elements **64**. For instance, if the bit-line current is sensed at time **84**, corresponding to an arbitrarily selected peak, a data value of 100 may be read rather than the correct data value of 011. Similarly, if the bit-line current is sensed at time **86**, corresponding to an arbitrarily selected local minimum, a data value of 010 may be read rather than a data value of 011. Thus, noise on the bit-line may cause erroneous readings from memory elements **64**.

FIG. **7** depicts a quantizing circuit **16** that may tend to reduce the likelihood of an erroneous reading. The illustrated quantizing circuit **16** includes an analog-to-digital converter **88** and a digital filter **90** coupled to each of the bit-lines **38**, **40**, **42**, **44**, and **46**, respectively. That is, each bit-line **38**, **40**, **42**, **44**, and **46** may connect to a different analog-to-digital converter **88** and digital filter **90**. The digital filters **90**, in turn, may connect to an input/output bus **92**, which may connect to a column decoder **18**, a column address latch **20**, and/or control circuitry **28** (see FIG. **2**).

In operation, the quantizing circuit **16** may digitize analog signals from the memory elements **64** in a manner that is relatively robust to noise. As explained below, the quantizing circuit **16** may do this by converting the analog signals into a bit-stream and digitally filtering high-frequency components from the bit-stream.

The analog-to-digital converter **88** may be a one-bit, analog-to-digital converter or a multi-bit, analog-to-digital converter. In the present embodiment, an analog-to-digital converter **88** receives an analog signal from the memory element **64**, e.g., a bit-line current $I_{BIT}$ or a bit-line voltage $V_{BL}$, and outputs a bit-stream that corresponds with the analog signal. The bit-stream may be a one-bit, serial signal with a time-averaged value that generally represents or corresponds to the time-averaged value of the analog signal from the memory element **64**. That is, the bit-stream may fluctuate between values of zero and one, but its average value, over a sufficiently large period of time, may be proportional to the average value of the analog signal from the memory element **64**. In certain embodiments, the bit-stream from the analog-to-digital converter **88** may be a pulse-density modulated (PDM) version of the analog signal. The analog-to-digital converter **88** may transmit the bit-stream to the digital filter **90** on a bit-stream signal path **94**.

The digital filter **90** may remove high-frequency noise from the bit-stream. To this end, the digital filter **90** may be a low-pass filter, such as a counter, configured to average or integrate the bit-stream over a sensing time, i.e., the time period over which the memory element **64** is read. As a result, the digital filter **90** may output a value that is representative of both the average value of the bit-stream and the average value of the analog signal from the memory element **64**. In some embodiments, the digital filter **90** is a counter, and the cut-off frequency of the digital filter **90** may be selected by adjusting the duration of the sensing time. In the present embodiment, increasing the sensing time will lower the cutoff frequency. That is, the frequency response of the digital filter **90** may be tuned by adjusting the period of time over which the bit-stream is integrated and/or averaged before outputting a final value. The frequency response of the digital filter **90** is described further below with reference to FIG. **15**. For multi-bit memory elements **64**, the output from the digital filter **90** may be a multi-bit binary signal, e.g., a digital word that is transmitted serially and/or in parallel.

Advantageously, in certain embodiments, the quantizing circuit **16** may facilitate the use of multi-bit memory elements **64**. As described above, in traditional designs, the number of discrete data values that a memory element **64** stores may be limited by sense amps that react to noise. In contrast, the quantizing circuit **16** may be less susceptible to noise, and, as a result, the memory elements **64** may be configured to store additional data. Without the high frequency noise, the intervals between signals representative of different data values may be made smaller, and the number of data values stored by a given memory element **64** may be increased. Thus, benefi-

cially, the quantizing circuit **16** may sense memory elements **64** that store several bits of data, e.g., 2, 3, 4, 5, 6, 7, 8, or more bits per memory element **64**.

Although the quantizing circuit **16** may sample the signal from the memory element **64** over a longer period of time than conventional designs, the overall speed of the memory device **12** may be improved. As compared to a conventional device, each read or write operation of the memory device **12** may transfer more bits of data into or out of the memory element **64**. As a result, while each read or write operation may take longer, more data may be read or written during the operation, thereby improving overall performance. Further, in some memory devices **12**, certain processes may be performed in parallel with a read or write operation, thereby further reducing the overall impact of the longer sensing time. For example, in some embodiments, the memory array **14** may be divided into banks that operate at least partially independently, so that, while data is being written or read from one bank, another bank can read or write data in parallel.

FIG. **8** illustrates details of one implementation of the quantizing circuit **16**. In this embodiment, the digital filter **90** is a counter, and the analog-to-digital converter **88** is a first-order delta-sigma modulator. The illustrated delta-sigma modulator **88** may include a latched comparator **96** (hereinafter the "comparator"), a capacitor **98**, and a switch **100**. In other embodiments, other types of digital filters and analog-to-digital converters may be employed, such as those described below in reference to FIGS. **17** and **18**.

As illustrated, an input of the counter **90** may connect to the bit-stream signal path **94**, which may connect to an output of the comparator **96**. The output of the comparator **96** may also connect to a gate of the switch **100** by a feedback signal path **102**. The output terminal (e.g., source or drain) of the switch **100** may connect in series to one of the bit-lines **38**, **40**, **42**, **44**, or **46**, and the input terminal of the switch **100** may connect to a reference current source **104** ($I_{Ref}$), One plate of the capacitor **98** may connect to one of the bit-lines **38**, **40**, **42**, **44**, or **46**, and the other plate of the capacitor **98** may connect to ground.

The illustrated counter **90** counts the number of clock cycles that the bit-stream **94** is at a logic high value or logic low value during the sampling period. The counter may count up or count down, depending on the embodiment. In some embodiments, the counter **90** may do both, counting up one for each clock cycle that the bit-stream has a logic high value and down one for each clock cycle that the bit-stream has a logic low value. Output terminals (D**0**-D**5**) of the counter **90** may connect to the input/output bus **92** for transmitting the count. The counter **90** may be configured to be reset to zero or some other value when a reset signal is asserted. In some embodiments, the counter **90** may be a series connection of D-flip flops, e.g., D-flip flops having SRAM or other memory for storing an initial value and/or values to be written to the memory element **64**.

In the illustrated embodiment, the clocked comparator **96** compares a reference voltage ($V_{Ref}$) to the voltage of one of the bit-lines **38**, **40**, **42**, **44**, or **46** ($V_{BL}$), which may be generally equal to the voltage of one plate of the capacitor **98**. The comparator **96** may be clocked (e.g., falling and/or rising edge triggered), and the comparison may be performed at regular intervals based on the clock signal, e.g., once per clock cycle. Additionally, the comparator **96** may latch, i.e., continue to output, values ($V_{FB}$) between comparisons. Thus, when the clock signals the comparator **96** to perform a comparison, if $V_{BL}$ is less than $V_{Ref}$, then the comparator **96** may latch its output to a logic low value, as described below in reference to FIG. **9**. Conversely, if $V_{BL}$ is greater than $V_{Ref}$, then the comparator **96** may latch a logic high value on its output, as described below in reference to FIG. **10**. As a result, the illustrated comparator **96** outputs a bit-stream that indicates whether $V_{BL}$ is larger than $V_{Ref}$, where the indication is updated once per clock cycle.

Advantageously, in some embodiments, the quantizing circuit **16** may include a single comparator (e.g., not more than one) for each column of multi-level memory elements **64**. In contrast, conventional sense amplifiers often include multiple comparators to read from a multi-bit memory cell, thereby potentially increasing device complexity and cost.

The capacitor **98** may be formed by capacitive coupling of the bit-lines **38**, **40**, **42**, **44**, and **46**. In other designs, this type of capacitance is referred to as parasitic capacitance because it often hinders the operation of the device. However, in this embodiment, the capacitor **98** may be used to integrate differences between currents on the bit-lines **38**, **40**, **42**, **44**, or **46** and the reference current to form the bit-stream, as explained further below. In some embodiments, the capacitor **98** may be supplemented or replaced with an integrated capacitor that provides greater capacitance than the "parasitic" bit-line capacitance.

The illustrated switch **100** selectively transmits current $I_{Ref}$ from the reference current source **104**. In various embodiments, the switch **100** may be a PMOS transistor (as illustrated in FIGS. **8**-**10**) or an NMOS transistor (as illustrated in FIG. **17**) controlled by the $V_{FB}$ signal on the feedback signal path **102**.

The operation of the quantizing circuit **16** will now be described with reference to FIGS. **9**-**12**. Specifically, FIGS. **9** and **10** depict current flows in the quantizing circuit **16** when the comparator **96** is latched low and high, respectively. FIG. **11** illustrates $V_{BL}$, the bit-stream output from the comparator **96**, and the corresponding increasing count of the counter **90** for a relatively small bit-line current. FIG. **12** depicts the same voltages when measuring a medium sized bit-line current, and FIG. **13** depicts these voltages when measuring a relatively large bit-line current.

To measure the current through the memory element **64**, the illustrated delta-sigma modulator **88** exploits transient effects to generate a bit-stream representative of the bit-line current $I_{BIT}$. Specifically, the delta-sigma modulator **88** may repeatedly charge and discharge the capacitor **98** with a current divider that subtracts the bit-line current $I_{BIT}$ from the reference current $I_{REF}$. Consequently, a large current through the memory element **64** may rapidly discharge the capacitor **98**, and a small current through the memory element **64** may slowly discharge the capacitor **98**.

To charge and discharge the capacitor **98**, the delta-sigma modulator **88** switches between two states: the state depicted by FIG. **9** (hereinafter "the charging state") and the state depicted by FIG. **10** (hereinafter "the discharging state"). Each time the delta-sigma modulator **88** changes between these states, the bit-stream changes from a logic high value to a logic low value or vice versa. The proportion of time that the delta-sigma modulator **88** is in the state illustrated by either FIGS. **9** or FIG. **10** may be proportional to the size of the bit-line current $I_{BIT}$ through the memory element **64**. The larger the bit-line current $I_{BIT}$, the more time that the delta-sigma modulator **88** is in the state illustrated by FIG. **9**, rather than the state illustrated by FIG. **10**, and the more time that the bit-stream has a logic low value.

Starting with the charging state (FIG. **9**), the capacitor **98** may initially accumulate a charge. To this end, the output of the comparator **96** is latched to logic low, which, as mentioned above, may occur when $V_{BL}$ is less than $V_{Ref}$. The logic low may be conveyed to switch **100** by the feedback signal path **102**, and the switch **100** may close, thereby conducting

the reference current $I_{Ref}$ through one of the bit-lines **38**, **40**, **42**, **44**, or **46**, as indicated by the larger arrows in FIG. **9**. A portion of the electrons flowing through the reference current source **104** may be stored by the capacitor **98**, as indicated by the smaller-horizontal arrows, and the remainder may be conducted through the memory element **64**, i.e., the bit-line current $I_{Bit}$, as indicated by the smaller vertical arrows. Thus, the capacitor **98** may accumulate a charge, and $V_{BL}$ may increase.

The comparator **96** and the reference current source **104** may cooperate to charge the capacitor **98** for a discrete number of clock cycles. That is, when the delta-sigma modulator **88** enters the charging state, the delta-sigma modulator **88** may remain in this state for an integer number of clock cycles. In the illustrated embodiment, the comparator **96**, the output of which is latched, changes state no more than once per clock cycle, so the switch **100**, which is controlled by the output of the comparator **96**, $V_{FB}$, conducts current for a discrete number of clock cycles. As a result, the reference current source **104** conducts current $I_{Ref}$ through the bit-line and into the capacitor **98** for an integer number of clock cycles.

After each clock cycle of charging the capacitor **98**, the delta-sigma modulator **88** may transition from the charging state to the discharging state, which is illustrated by FIG. **10**, depending on the relative values of $V_{BL}$ and $V_{Ref}$. Once per clock cycle (or at some other appropriate interval, such as twice per clock cycle), the comparator **96** may compare the voltage of the capacitor $V_{BL}$ to the reference voltage $V_{Ref}$. If the capacitor **98** has been charged to the point that $V_{BL}$ is greater than $V_{Ref}$, then the output of the comparator **96** may transition to logic high, as illustrated in FIG. **10**. The logic high signal may be conveyed to the switch **100** by the feedback signal path **102**, thereby opening the switch **100**. As a result, the reference current source **104** may cease flowing current through the memory element **64** and into the capacitor **98**, and the capacitor **98** may begin to discharge through the memory element **64**.

In the present embodiment, the delta-sigma modulator **88** discharges the capacitor **98** for a discrete number of clock intervals. After each clock cycle of discharging the capacitor **98**, the delta-sigma modulator **88** compares $V_{BL}$ to $V_{Ref}$. If $V_{BL}$ is still greater than $V_{Ref}$, then the comparator **96** may continue to output a logic high signal, i.e., $V_{FB}$=1, and the switch **100** remains open. On the other hand, if enough current has flowed out of the capacitor **98** that $V_{BL}$ is less than $V_{Ref}$, then the comparator **96** may output a logic low signal, i.e., $V_{FB}$=0, and the switch **100** may close, thereby transitioning the delta-sigma modulator **88** back to the charging state and initiating a new cycle.

The counter **90** may count the number of clock cycles that the delta-sigma modulator **88** is in either the charging state or the discharging state by monitoring the bit-stream signal path **94**. The bit-stream signal path **94** may transition back and forth between logic high and logic low with the output of the comparator **96**, $V_{FB}$, and the counter **90** may increment and/or decrement a count once per clock cycle (or other appropriate interval) based on whether the bit-stream is logic high or logic low. After the sensing time has passed, the counter **90** may output a signal indicative of the count on output terminals D**0**-D**5**. As explained below, the count may correspond, e.g., proportionally, to the bit-line current, $I_{Bit}$.

FIGS. **11**-**13** illustrate voltages $V_{FB}$ and $V_{BL}$ in the quantizing circuit **16** when reading a memory element **64**. Specifically, FIG. **11** illustrates a low-current case, in which the value stored by the memory element **64** corresponds to a relatively low bit-line current. Similarly, FIG. **12** illustrates a medium-current case, and FIG. **13** illustrates a high-current case. In each of these figures, the ordinate of the lower trace represents the voltage of the bit-stream signal path **94**, $V_{FB}$, and the ordinate of the upper trace illustrates the bit-line voltage, $V_{BL}$. The abscissa in each of the traces represents time, with the lower trace synchronized with the upper trace, and the duration of the time axes is one sensing time **106**.

As illustrated by FIG. **11**, the counter **90** is initially set to zero (or some other appropriate value) by asserting a reset signal. In some embodiments, the delta-sigma modulator **88** may undergo a number of start-up cycles to reach steady-state operation before initiating the sensing time and resetting the counter **90**. At the beginning of the illustrated read operation, the delta-sigma modulator **88** is in the charging state, which charges the capacitor **98** and increases $V_{BL}$, as indicated by dimension arrow **108**. At the beginning of the next clock cycle, the comparator **96** compares the bit-line voltage to the reference voltage and determines that the bit-line voltage is greater than the reference voltage. As a result, the bit-stream signal path **94** ($V_{FB}$) transitions to a logic high voltage, and the delta-sigma modulator **88** transitions to the discharging state. Additionally, the counter **90** increments the count by one to account for one clock cycle of the bit-stream signal **94** holding a logic low value. Next, the charge stored on the capacitor **98** drains out through the memory element **64**, and the bit-line voltage drops until the comparator **96** detects that $V_{BL}$ is less than $V_{Ref}$, at which point the cycle repeats. The cycle has a period **112**, which may be divided into a charging portion **114** and a discharging portion **116**. Once during each cycle in the sensing time **106**, the count stored in the counter **90** may increase by one. At the end of the sensing time **106**, the counter **90** may output the total count.

A comparison of FIG. **11** to FIGS. **12** and **13** illustrates why the count correlates with the bit-line current. In FIG. **13**, the high-current case, the stored charge drains from the capacitor **98** quickly, relative to the other cases, because the bit-line current $I_{BIT}$ is large and, as a result, the delta-sigma modulator **88** spends more time in the charging state than the discharging state. As a result, the bit-stream has a logic low value for a large portion of the sensing time **106**, thereby increasing the count.

The capacitance of the capacitor **98** may be selected with both the clock frequency and the range of expected bit-line currents in mind. For example, the capacitor **98** may be large enough that the capacitor **98** does not fully discharge or saturate when the bit-line current $I_{BIT}$ is either at its lowest expected value or at its highest expected value. That is, in some embodiments, the capacitor **98** generally remains in a transient state while reading the memory element **64**. Similarly, the frequency at which the comparator **96** is clocked may affect the design of the capacitor **98**. A relatively high frequency clock signal may leave the capacitor **98** with relatively little time to discharge or saturate between clock cycles, thereby leading a designer to choose a smaller capacitor **98**.

Similarly, the size of the reference current may be selected with the range of expected bit-line currents in mind. Specifically, in certain embodiments, the reference current is less than the largest expected bit-line current $I_{BIT}$, so that, in the case of maximum bit-line current $I_{BIT}$, the capacitor **98** can draw charge from the reference current while the rest of the reference current flows through the memory element **64**.

FIG. **14** illustrates the relationship between the bit-line current $I_{BIT}$ and the count for the presently discussed embodiment. As illustrated by FIG. **14**, the count is generally proportional to the bit-line current $I_{BIT}$. This relationship is described by the following equation (Equation 1), in which $N_{ST}$ represents the number of clock cycles during the sensing time:

$$I_{Bit}/I_{Ref}=\text{Count}/N_{ST}$$

Thus, in the illustrated embodiment, the count is indicative of the bit-line current $I_{BIT}$, which is indicative of the value stored by the memory element **64**.

Advantageously, the quantizing circuit **16** may categorize the bit-line current $I_{BIT}$ as falling into one of a large number of categories, each of which is represented by an increment of the count. That is, the quantizing circuit **16** may resolve small differences in the bit-line current $I_{BIT}$. The resolution of the quantizing circuit **16** may be characterized by the following equation (Equation 2), in which $I_{MR}$ represents the smallest resolvable difference in bit-line current $I_{BIT}$, i.e., the resolution of the quantizing circuit **16**:

$$I_{MR}=I_{Ref}/N_{ST}$$

Thus, the resolution of the quantizing circuit **16** may be increased by increasing the sensing time or the clock frequency or by decreasing $I_{Ref}$, which may limit the maximum cell current since $I_{MR}$ is less than $I_{Ref}$.

The resolution of the quantizing circuit **16** may facilitate storing multiple bits in the memory element **64** or detecting multiple levels of light intensity in an image sensor element. For example, if the quantizing circuit **16** is configured to categorize the bit-line current $I_{BIT}$ into one of four different levels, then the memory element **64** may store two-bits of data or, if the quantizing circuit **16** is configured to categorize the bit-line current $I_{BIT}$ into one of eight different current levels, then the memory element **64** may store three-bits of data. For the present embodiment, the number of bits stored by the memory element **64** may be characterized by the following equation (Equation 3), in which $N_B$ represents the number of bits stored by a memory element **64** and $I_{Range}$ represents the range of programmable bit-line currents through the memory element **64**:

$$N_B=\log(I_{Range}/I_{MR})/\log 2$$

In short, in the present embodiment, greater resolution translates into higher density data storage for a given memory element **64**.

FIG. **15** illustrates another advantage of the present embodiment: the quantizing circuit **16** may filter out the effects of noise. In the illustrated embodiment, high-frequency fluctuations in the bit-line current $I_{BIT}$ are filtered out of the final value by summing or averaging the bit-stream over the sensing time **106**. In FIG. **15**, $f_{CLK}$ represents the clock frequency, and $N_{ST}$ represents the number of clock cycles per sensing time **106**, as mentioned above. Thus, to reduce the cutoff frequency and to further mitigate the effect of noise, $N_{ST}$ may be increased by increasing the frequency or the sensing time **106**. As a result, in some embodiments, the quantizing circuit **16** may be tuned to trade off signal-to-noise ratio for speed.

FIG. **16** depicts an example of a read operation **118** that is performed by certain embodiments of the quantizing circuit **16**. The read operation **118** begins with resetting the counter, as illustrated by block **120**. Next, the reference current is conducted both into the capacitor and through the memory cell, as illustrated by block **122**. Then, a determination is made as to whether a new clock cycle has started, as depicted by block **124**. Depending on the result, the read operation **118** either returns to block **122** or continues to block **126**, where a determination is made as to whether the voltage of the capacitor is greater than a reference voltage. Depending on the result, the read operation **118** either returns to block **122** or continues to block **128**, at which point the reference current is no longer conducted. Next, the capacitor is discharged through the memory element, as depicted by block **130**, and a determination is made as to whether a new clock cycle has started, as depicted by block **134**. Based on the results of the determination, either the capacitor continues to discharge through the memory cell, as described by block **130**, or the count is increased by one, as depicted by block **136**. Then, a determination is made as to whether the voltage of the capacitor is less than the reference voltage, as depicted by block **138**. Based on the result of the determination, the read operation **118** either returns to block **130** to continue discharging the capacitor or continues to block **140**, where a determination is made as to whether the sensing time has elapsed. Based on the determination at block **140**, the read operation **118** either returns to block **122** to initiate a new charge and discharge cycle or outputs a count from the counter, as depicted by block **142**.

FIG. **17** illustrates another embodiment of a quantizing circuit **144**. The quantizing circuit **144** is similar to the quantizing circuit **16** illustrated in FIG. **8** with a few exceptions: the bit-stream **94** is not inverted before reaching the counter **90** and the switch **148** is a PMOS transistor. The quantizing circuit **144** operates in a similar manner to the quantizing circuit **16** except that the comparator **96** generates a feedback signal/bit-stream signal that tends to keep the bit-line voltage below the reference voltage rather than above it.

FIG. **18** illustrates a third embodiment of a quantizing circuit **150**, which compares the bit-line voltage to a triangle waveform or a saw-tooth waveform to generate the bit-stream **94**. In the present embodiment, the quantizing circuit includes a reference resistor, $R_{Ref}$, that forms a voltage divider **152** with the memory element **64** and a waveform generator **154** that supplies the reference voltage. The waveform generator **154** may be configured to output a triangle wave or a saw-tooth wave voltage signal to the comparator **96**. The reference voltage waveform may be centered within the range of expected bit-line voltages and the amplitude of the reference voltage waveform may exceed the range of expected bit line voltages. As with previously described embodiments, in operation, the amount of the time that the bit-stream **94** is logic high may be proportional to the bit-stream voltage, which is indicative of the data stored by the memory element **64**.

FIG. **19** depicts an exemplary processor-based system **310** that includes the memory device **12**. Alternatively or additionally, the system **310** may include the imaging device **13**. The system **310** may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, control circuit, etc. In a typical processor-based system, one or more processors **312**, such as a microprocessor, control the processing of system functions and requests in the system **310**. The processor **312** and other subcomponents of the system **310** may include quantizing circuits, such as those discussed above.

The system **310** typically includes a power supply **314**. For instance, if the system **310** is a portable system, the power supply **314** may advantageously include a fuel cell, permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply **314** may also include an AC adapter, so the system **310** may be plugged into a wall outlet, for instance. The power supply **314** may also include a DC adapter such that the system **310** may be plugged into a vehicle cigarette lighter, for instance.

Various other devices may be coupled to the processor **312** depending on the functions that the system **310** performs. For instance, a user interface **316** may be coupled to the processor **312**. The user interface **316** may include buttons, switches, a

keyboard, a light pen, a mouse, a digitizer and stylus, and/or a voice recognition system, for instance. A display **318** may also be coupled to the processor **312**. The display **318** may include an LCD, an SED display, a CRT display, a DLP display, a plasma display, an OLED display, LEDs, and/or an audio display, for example. Furthermore, an RF sub-system/baseband processor **320** may also be coupled to the processor **312**. The RF sub-system/baseband processor **320** may include an antenna that is coupled to an RF receiver and to an RF transmitter (not shown). One or more communication ports **322** may also be coupled to the processor **312**. The communication port **322** may be adapted to be coupled to one or more peripheral devices **324** such as a modem, a printer, a computer, or to a network, such as a local area network, remote area network, intranet, or the Internet, for instance.

The processor **312** generally controls the system **310** by implementing software programs stored in the memory. The memory is operably coupled to the processor **312** to store and facilitate execution of various programs. For instance, the processor **312** may be coupled to the volatile memory **326** which may include Dynamic Random Access Memory (DRAM) and/or Static Random Access Memory (SRAM). The volatile memory **326** is typically large so that it can store dynamically loaded applications and data. As described further below, the volatile memory **326** may be configured in accordance with embodiments of the present invention.

The processor **312** may also be coupled to the memory device **12**. The memory device **12** may include a read-only memory (ROM), such as an EPROM, and/or flash memory to be used in conjunction with the volatile memory **326**. The size of the ROM is typically selected to be just large enough to store any necessary operating system, application programs, and fixed data. Additionally, the non-volatile memory **328** may include a high capacity memory such as a tape or disk drive memory.

The memory device **10** and volatile memory **326** may store various types of software, such as an operating system or office productivity suite including a word processing application, a spreadsheet application, an email application, and/or a database application.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

**1**. An electronic device, comprising:
- an internal data storage location coupled to an electrical conductor; and
- a quantizing circuit coupled to the internal data storage location via the electrical conductor, the quantizing circuit comprising:
- an analog-to-digital converter having an input and an output, wherein the input is coupled to the electrical conductor, wherein the analog-to-digital converter comprises a delta-sigma modulator comprising:
  - a comparator having first and second inputs and an output, wherein the output of the comparator is coupled to the digital filter, wherein the first input is coupled to the electrical conductor, and wherein the second input is coupled to a reference voltage source;
  - a capacitor having one plate coupled to the electrical conductor; and
  - a switch coupled to the electrical conductor in series with the internal data storage location, wherein the switch comprises a gate coupled to the output of the comparator; and
- a digital filter coupled to the output of the analog-to-digital converter.

**2**. The electronic device of claim **1**, wherein the internal data storage location comprises a non-volatile memory element selected from a floating-gate transistor, a phase-change memory element, or a magneto-resistive memory element.

**3**. The electronic device of claim **1**, wherein the internal data storage location comprises a light sensor.

**4**. The electronic device of claim **1**, wherein the digital filter comprises a counter.

**5**. A semiconductor device, comprising:
- a plurality of internal data storage locations coupled to an electrical conductor in series;
- an analog-to-digital converter with an input coupled to the electrical conductor; and
- a digital filter with an input coupled to an output of the analog-to-digital converter, wherein the analog-to-digital converter comprises:
- a comparator having a first input coupled to the electrical conductor, a second input coupled to a reference voltage source, and an output coupled to an input of the digital filter, wherein the comparator is configured to latch the output to logic high or logic low once per clock cycle based on whether the voltage of the first input is greater than the voltage of the second input; and
- a switch having a first terminal, a second terminal coupled to the electrical conductor, and a gate coupled to the output of the comparator; and
- a reference current source coupled to the first terminal of the switch.

**6**. The semiconductor device of claim **5**, wherein the analog-to-digital converter is configured to output a pulse-density modulated bit-stream that has an average value that is generally proportional to the current through the electrical conductor.

**7**. The semiconductor device of claim **5**, wherein the digital filter is a low-pass digital filter comprising a counter.

**8**. The semiconductor device of claim **5**, wherein the analog-to-digital filter comprises a comparator with a first input coupled to the electrical conductor, a second input coupled to a voltage-signal generator configured to output a triangle wave or a saw-tooth wave, and an output coupled to the digital filter.

**9**. A method of digitizing an analog signal, the method comprising:
- receiving an analog signal from an internal data storage location of an integrated semiconductor device;
- converting the analog signal into a binary bit-stream, wherein converting the analog signal comprises charging a capacitor and discharging the capacitor, wherein the proportion of time that the capacitor is charging is generally proportional to the current on the electrical conductor; and
- filtering the binary bit-stream through a digital filter.

**10**. The method of claim **9**, wherein converting the analog signal comprises comparing a voltage of a bit-line connected to the internal data storage location to a reference voltage.

**11**. The method of claim **9**, wherein converting the analog signal comprises integrating a difference between a current on the electrical conductor and a reference current.

**12**. The method of claim **9**, wherein digitally filtering comprises removing low-frequency components of the binary

bit-stream by incrementing a count, decrementing the count, or both based on the value of the binary bit-stream.

**13**. The method of claim **12**, comprising determining a multi-bit value stored by the internal data storage location based on an output from the digital filter.

**14**. A method of digitizing an analog signal, the method comprising:

receiving an analog signal from an internal data storage location;

convening the analog signal into a binary bit-stream, wherein converting the analog signal comprises:

comparing a voltage of the electrical conductor to a reference voltage; and

charging a capacitor and discharging the capacitor, wherein the proportion of time that the capacitor is charging is generally proportional to the current on the electrical conductor; and

filtering the binary bit-stream through a digital filter.

**15**. The method of claim **14**, comprising comparing a voltage of the electrical conductor to a reference voltage at a plurality of periodic time intervals based on a clock cycle.

**16**. The method of claim **15**, comprising latching a result of each comparison between comparisons.

**17**. The method of claim **15**, wherein digitally filtering comprises removing low frequency components of the binary bit-stream by incrementing a count, decrementing the count, or both based on the value of the binary bit-stream.

**18**. A method of sensing a signal, the method comprising:

conducting a reference current both into a capacitor and through an internal data storage location;

determining whether the voltage of the capacitor is greater than a reference voltage;

if the voltage of the capacitor is greater than the reference voltage, then:

ceasing to conduct the reference current through the internal data storage location and into the capacitor;

discharging the capacitor through the internal data storage location; and

adjusting a count by one increment.

**19**. The method of claim **18**, wherein conducting the reference current comprises conducting the reference current between a source and a drain of a flash memory device.

**20**. The method of claim **18**, comprising periodically determining whether the voltage of the capacitor is greater than the reference voltage, wherein the determinations are temporally separated from one another by a regular time interval based on a clock cycle.

**21**. The method of claim **18**, comprising, if the voltage of the capacitor is not greater than the reference voltage, then determining whether a predetermined time period for sensing the internal data storage location has elapsed.

**22**. The method of claim **21**, comprising, outputting a value that is based on the count if the predetermined time period for sensing the internal data storage location has elapsed.

**23**. A system, comprising:

an integrated semiconductor device comprising:

a plurality of internal data storage locations;

a delta-sigma modulator coupled to the plurality of internal data storage locations, wherein the delta-sigma modulator is configured to receive an analog signal from the internal data storage locations and generate a pulse-density modulated bit-stream that is representative of the analog signal; and

a low-pass, digital filter coupled to the delta-sigma modulator, wherein the digital filter is configured to filter the bit-stream.

**24**. The system of claim **23**, wherein the plurality of internal data storage locations each comprise an internal data storage location selected from a floating gate transistor, a capacitor, a phase-change resistive memory element, a magneto-resistive memory element, or a floating diffusion region of an imager pixel.

**25**. The system of claim **23**, comprising a processor coupled to the integrated semiconductor device.

**26**. The system of claim **25**, comprising a computer system including a motherboard coupled to the processor and the integrated semiconductor device, a video card coupled to the motherboard, and a hard drive coupled to the motherboard.

**27**. A method of quantizing a signal, comprising:

accessing a charge stored on an internal data storage location;

generating an analog signal from the accessed charge;

convening the analog signal to a pulse-density modulated signal, wherein converting the analog signal comprises comparing a voltage of a bit-line connected to the internal data storage location to a reference voltage; and

digitally filtering the pulse-density modulated signal.

**28**. The method of claim **27**, wherein the internal data storage location comprises a capacitor configured to store the charge.

**29**. The method of claim **27**, wherein the internal data storage location comprises a floating gate transistor.

**30**. The method of claim **27**, wherein the internal data storage location comprises a diffusion region configured to store electrons produced by externally applied photons.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO. : 7,667,632 B2
APPLICATION NO. : 11/818999
DATED : February 23, 2010
INVENTOR(S) : R. Jacob Baker

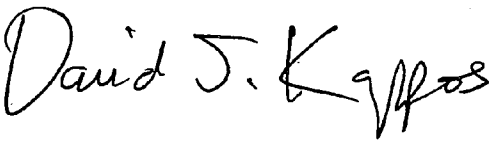
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 15, line 10, in Claim 14, delete "convening" and insert -- converting --, therefor.

In column 16, line 35, in Claim 27, delete "convening" and insert -- converting --, therefor.

Signed and Sealed this

First Day of June, 2010



David J. Kappos
*Director of the United States Patent and Trademark Office*