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(54) **METHOD AND SYSTEM FOR REDUCING MISMATCH BETWEEN REFERENCE AND INTENSITY PATHS IN ANALOG TO DIGITAL CONVERTERS IN CMOS ACTIVE PIXEL SENSORS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1054 days.

This patent is subject to a terminal disclaimer.

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(51) **Int. Cl.**
H04N 5/335　　　(2006.01)
H04N 5/235　　　(2006.01)
(52) **U.S. Cl.** **348/308**; 348/221.1
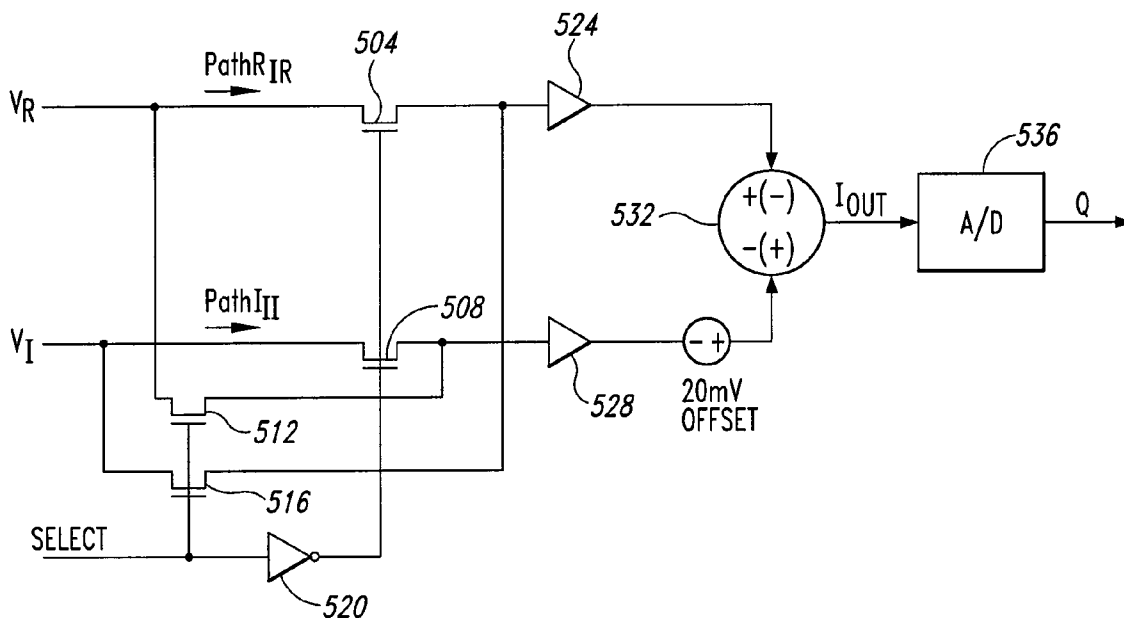(58) **Field of Classification Search** 348/241, 348/308, 333.1, 211.2, 221.1
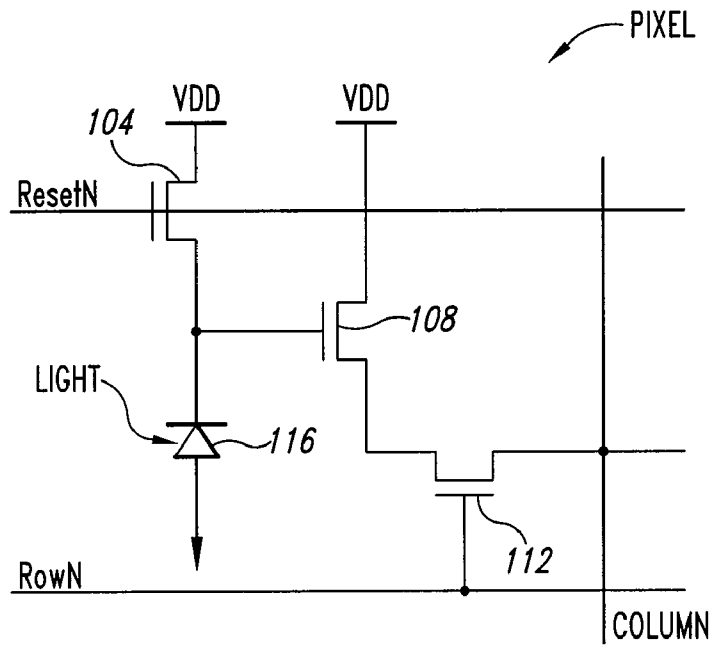See application file for complete search history.

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(57)　　　　　　**ABSTRACT**

A circuit for reducing a mismatch between a reference path to which a reference voltage is applied and an intensity path to which an intensity voltage is applied from an active pixel sensor comprises a first and a second pair of switches and a processing circuit. The first pair of switches couple an intensity input node to which the intensity voltage is applied to a first output node and couple a reference input node to which the reference voltage is applied to a second output node during a first operating period. The second pair of switches couple the intensity input node to the second output node and couple the reference input node to the first output node during a second operating period. A polarity reversing circuit is included in the processing circuit for coupling the first and second output nodes to the processing circuit with one polarity during the first operating period and in a reverse polarity during the second operating period.

14 Claims, 3 Drawing Sheets
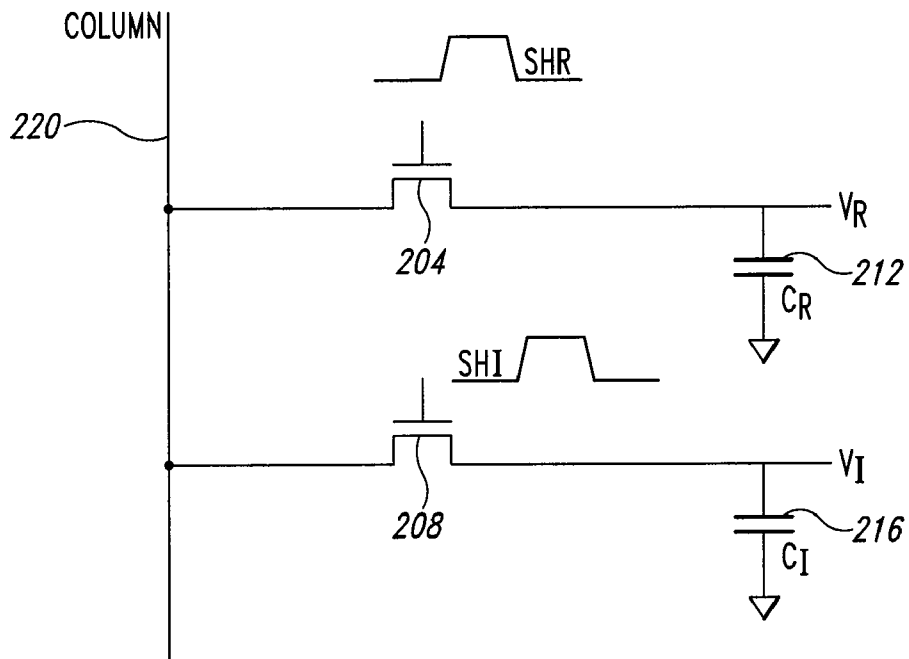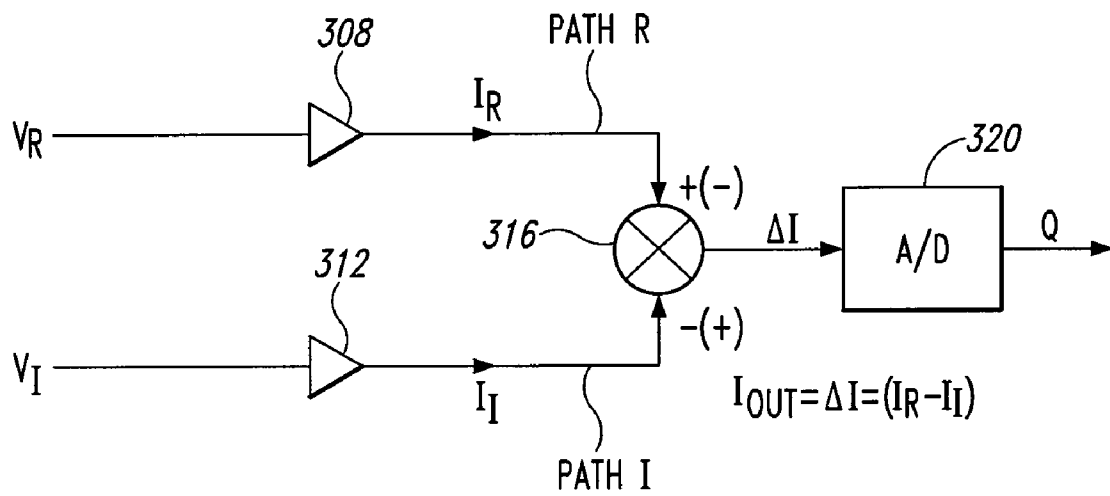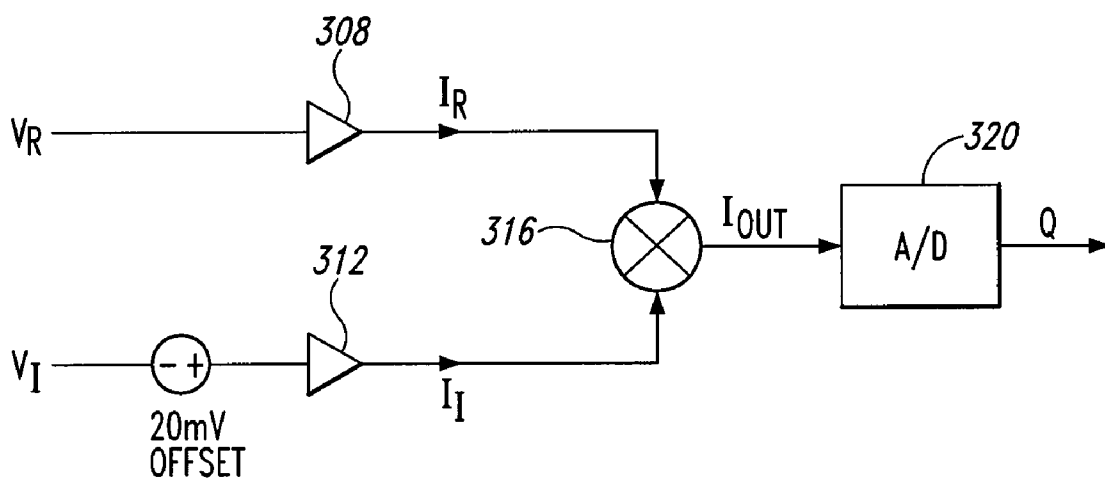
PIXEL

VDD   VDD

104

ResetN

108

LIGHT

116

RowN

112

COLUMN

Fig. 1
(Prior Art)

COLUMN

SHR

220

204

V_R

C_R 212

SHI

208

V_I

C_I 216

Fig. 2
(Prior Art)

308

PATH R

V_R I_R

320

316

$+(-)$

ΔI

A/D

Q

312

$-(+)$

V_I I_I

$I_{OUT} = \Delta I = (I_R - I_I)$

PATH I

Fig. 3
(Prior Art)

308

V_R I_R

320

316

I_{OUT}

A/D

Q

312

V_I I_I

$-+$

20mV
OFFSET

Fig. 4
(Prior Art)

V_R

$PathR_{IR}$ 504   524

V_I

$PathI_{II}$ 508

512

516

SELECT

520

532   $+(-)$ $-(+)$ I_{OUT} A/D   Q

536

528   $-(+)$ 20mV OFFSET

Fig. 5

600

604

608

612

616

Fig. 6

METHOD AND SYSTEM FOR REDUCING MISMATCH BETWEEN REFERENCE AND INTENSITY PATHS IN ANALOG TO DIGITAL CONVERTERS IN CMOS ACTIVE PIXEL SENSORS

TECHNICAL FIELD

The present invention relates generally to CMOS Active Pixel Sensors (APSs), and more specifically to reducing a mismatch between a reference path and an intensity path in an A/D converter in a CMOS APS.

BACKGROUND OF THE INVENTION

In digital and video cameras, CMOS APSs are used to acquire images. An APS is defined as a solid state image sensor that has one or more active transistors within a pixel unit cell. This is in contrast to a passive pixel sensor that uses a simple switch to connect a pixel signal to a column. An APS provides lower noise, improved scalability and higher speed compared to passive pixel sensors.

In an APS, each pixel contains a photosensing means and at least one other active component. When light is incident on a pixel, a charge is created that is converted to a signal, either a voltage or current signal. The signal represents the amount of light incident upon a pixel.

FIG. 1 is a schematic of a portion of a conventional CMOS APS comprising transistors 104, 108, 112 and a photodiode 116. Although circuitry for only a single pixel is shown in FIG. 1, it will be understood that circuitry for a large number of pixels are normally included in an APS array. Light is coupled through a color filter (not shown) to the photodiode 116. Different colored filters are used in an APS array so that signals from different sets of pixels allow a color image to be created. The photodiode 116 changes the light to a charge having a magnitude that is proportional to the intensity of the light. The charge is converted into a voltage and passed to a column line.

Prior to acquiring an image, each pixel in the APS is reset. This is accomplished by driving a reset row line (Reset N) to a voltage, V_{DDP}, where $V_{DDP} > V_{DD} + V_{THN}$, and V_{THN} is the threshold voltage of the transistor 104. This causes the transistor 104 to turn on and sets the voltage across the photodiode 116 to V_{DD}. The voltage on the column line is called the dark or reference voltage level, V_R, of the pixel. Next, the transistor 112 is turned on by driving Row N to V_{DDP} and, with transistor 108 behaving as a source follower, the column line is set to the reference voltage level, V_R. The reference voltage V_R is stored at the beginning of a sense.

After the reference voltage V_R is stored, the Reset N line is driven low, thus turning off the transistor 104 to isolate the photodiode 116 from V_{DD}. The light striking the reverse biased photodiode 116 then generates electron-hole pairs that cause the voltage across the photodiode 116 to decrease. The voltage from the photodiode 116 is applied to the gate of the transistor 108, which couples the voltage to column line through the transistor 112, which is turned on by the high RowN signal. As a result, the decrease in the voltage across the photodiode 116 is sampled on the column line and this voltage is called an intensity voltage V_I.

The time between the Reset N line being driven low and the intensity voltage, V_I, corresponding to the intensity of the light striking the photodiode 116 being sampled on the column line is called the aperture time. Note that the dark signal corresponds to a large voltage ($V_{DD} - V_{THN}$) on the column

line while a bright signal corresponds to a lower voltage, less than ($V_{DD} - V_{THN}$) on the column line.

FIG. 2 illustrates a conventional sample and hold circuit that can be used to sample and hold a reference voltage V_R and an intensity voltage V_I from an APS. The sample and hold circuit comprises transistors 204, 208 and hold capacitors 212, 216. The transistor 204 and the hold capacitor 212 are connected in series between a column line 220 and ground. Similarly, the transistor 208 and the hold capacitor 216 are connected in series between the column line 220 and ground.

When ResetN and RowN are high, the pixel's reference or dark voltage, V_R, is placed on the column line 220. At this time, a sample and hold reference signal, SHR, is driven high, which turns on the transistor 204, thereby placing a sample of V_R on the hold capacitor 212.

Next, ResetN transitions low to allow the photodiode 116 to change light into a corresponding charge. After the aperture time, a sample of the intensity voltage V_I is placed on the column line 220. At this time, the sample and hold intensity signal SHI is driven high, which turns on the transistor 208, thereby placing a sample of V_I on the hold capacitor 216.

Because each pixel in an imaging array will have slightly different characteristics, the differences in the intensity voltage V_I for light having the same intensity can result in speckles in a resulting image. To eliminate this mismatch problem, images are created based on the intensity of the change of light during an aperture time. This is accomplished by subtracting the reference voltage V_R from the actual measured signal or intensity voltage V_I to accurately determine the light intensity applied to the pixel.

FIG. 3 is a schematic of a conventional circuit that uses the differences in V_R and V_I to accurately determine the light intensity applied to the pixel, and to generate a digital output Q by an A/D. As mentioned earlier, V_R and V_I are sampled and held on to capacitors 212 and 216, respectively. V_R is then converted to a current I_R by a voltage to current converter 308. Similarly, V_I is converted to a current I_I by a voltage to current converter 312. The implementation of a voltage to current converter is well understood by those skilled in the art and thus will not be discussed in detail.

The currents I_R and I_I flow through path R and path I, respectively, to a differential circuit 316. The differential circuit generates an output current I_{OUT}, where $I_{OUT} = I_R - I_I$. I_{OUT} is representative of the difference between V_R and V_I. The differential circuit 316 can be implemented using a current mirror circuit or other circuits well known to those skilled in the art. An A/D converter 320 receives I_{OUT} and generates a digital output Q. Thus, the digital output Q is representative of the difference between V_R and V_I.

While the schematic of FIG. 3 eliminates the problem caused by the mismatches in pixel characteristics, the sampling circuit, having two separate paths, i.e., reference path and intensity signal path, is also subject to a mismatch. Each voltage to current converter has a different random offset that creates a mismatch between the two paths, thereby degrading the resulting the image. Also voltage to current converter has a varying transconductance ($gm = I_R/V_R$ or I_S/V_S) that degrades the image. The schematic of FIG. 3 does not eliminate the mismatches in the paths.

FIG. 4 illustrates the mismatch between the reference path and the intensity path. In FIG. 4, a 20 mV offset is in series with the intensity path. The offset voltage, that may be positive or negative, simply represents the mismatch in the paths.

Accordingly, there is a need for a system and a method that reduce the mismatch between the reference path and signal path in an APS.

SUMMARY OF THE INVENTION

According to one aspect of the present invention, a circuit for reducing a mismatch between a reference path to which a reference voltage is applied and an intensity path to which an intensity voltage is applied from an active pixel sensor comprises a first and a second pair of switches and a processing circuit. The first pair of switches couple an intensity input node to which the intensity voltage is applied to a first output node and couple a reference input node to which the reference voltage is applied to a second output node during a first operating period. The second pair of switches couple the intensity input node to the second output node and couple the reference input node to the first output node during a second operating period. A polarity reversing circuit is included in the processing circuit for coupling the first and second output nodes to the processing circuit with one polarity during the first operating period and in a reverse polarity during the second operating period. A toggle switch is coupled to the first and second pair of switches and is adapted to receive a select signal and operable responsive to the select signal to enable the first pair of switches during the first operating period and to enable the second pair of switches during the second operating period.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic of a portion of a conventional CMOS APS.

FIG. 2 illustrates a sample and hold circuit to sample reference and intensity voltages.

FIG. 3 is a schematic for generating a digital output representative of a difference between the reference and intensity voltages.

FIG. 4 illustrates a mismatch between the reference path and the intensity path.

FIG. 5 illustrates a circuit for reducing the mismatch according to one embodiment of the invention.

FIG. 6 shows a digital camera including a circuit for reducing the mismatch.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 5 illustrates a circuit according to one embodiment of the invention in which the inputs to an A/D converter are switched halfway through the A/D conversion to eliminate the mismatch. The circuit comprises transistors 504, 508, 512, 516 and a toggle switch 520. The circuit couples the reference voltage V_R and the intensity voltage V_I to an A/D converter 536. A current to voltage converter 524 is in series with path R, and a current to voltage converter 528 is in series with path I. A 20 mV offset is in series with path I. The 20 mV offset represents a mismatch between the path I and path S. As discussed earlier, the 20 mV offset is caused by a varying transconductance and random offset associated with path R and path I. A differential circuit 532 is coupled to paths R and I. The differential circuit 532 receives the currents I_R and I_I and generates and output I_{OUT}, where $I_{OUT} = I_R - I_I$. The polarity of the 20 mV offset with respect to the differential circuit 532 can be reversed during the operation of the circuit.

Consider, for example, an A/D conversion that occurs over a period of 20 us. During the first 10 μs, the select signal is low, which turns transistors 504 and 508 on and transistors 512 and 516 off. Thus path R applies the current I_R to the differential circuit 532 and path S applies the current I_I to the differential circuit 532.

During the next 10 μs, the select signal is driven high, which turns the transistors 504 and 508 off and turns the transistors 512 and 516 on, thereby switching the inputs to the differential circuit 523. During this time, path I applies the current I_S to the differential circuit 532, and path S applies the current I_I to the differential circuit 532.

During the first 10 μs, the 20 mV offset is connected in series with path I. During the next 10 μs, the 20 mV offset is connected in series with path R but with polarity of the 20 mV offset reversed with respect to the differential circuit 532.

By switching the inputs to the differential circuit 532 halfway through the A/D conversion, each signal is subject to the same amount of offset and gain during the total conversion period. Thus, the mismatch due to the difference in the paths are eliminated.

FIG. 8 illustrates a digital camera 600 that utilizes a circuit in accordance with one embodiment of the invention. The digital camera 600 includes a lens 608, a CMOS APS 612 and a circuit 612. The CMOS APS 612 receives light through the lens 608 and generates a column voltage that is applied to the circuit 612. The circuit 612 reduces the mismatch between a reference path and an intensity path as discussed above.

It is to be understood that even though various embodiments and advantages of the present invention have been set forth in the foregoing description, the above disclosure is illustrative only, and changes may be made in detail, and yet remain within the broad principles of the invention. For example, many of the components described above may be implemented using either digital or analog circuitry, or a combination of both, and also, where appropriate, may be realized through software executing on suitable processing circuitry. Therefore, the present invention is to be limited only by the appended claims.

The invention claimed is:

1. A circuit for coupling an intensity voltage and a reference voltage from an active pixel sensor to a processing circuit, comprising:
    a first pair of switches coupling an intensity input node to which the intensity voltage is applied to a first output node and coupling a reference input node to which the reference voltage is applied to a second output node during a first operating period;
    a second pair of switches coupling the intensity input node to the second output node and coupling the reference input node to the first output node during a second operating period; and
    a polarity reversing circuit operative to couple the first and second output nodes to the processing circuit with one polarity during the first operating period and in a reverse polarity during the second operating period.

2. The circuit of claim 1 further comprising a toggle switch coupled to the first and second pair of switches, the toggle switch being configured to receive a select signal and operable responsive to the select signal to enable the first pair of switches during the first operating period and to enable the second pair of switches during the second operating period.

3. The circuit of claim 1 further comprising a current mirror circuit included in the processing circuit, the current mirror circuit being configured to receive the reference and intensity voltages and operable to generate an output current representative of the difference between the reference and intensity voltages.

4. The circuit of claim 3 further comprising an A/D converter circuit configured to receive the output current and operable to generate a digital output relative to the output current.

5. A circuit for reducing a mismatch between a reference path and an intensity path coupling a CMOS active pixel sensor to a processing circuit, comprising:

a first and a second transistor coupled to the reference and intensity paths, respectively, and operable to apply a reference and an intensity voltage to a first and second input, respectively, of the processing circuit during a first operating period;

a third and a fourth transistor coupled to the reference and intensity paths, respectively, and operable to apply the reference and intensity voltages to the second and first input, respectively, of the processing circuit during a second operating period;

a toggle switch adapted configured to receive a select signal, and operable responsive to the select signal to enable the first and second transistors during the first operating period and to enable the third and fourth transistors during the second operating period; and

a polarity reversing circuit operable to couple the first and second inputs to the processing circuit with one polarity during the first operating period and in a reverse polarity during the second operating period.

6. The circuit of claim **5** further comprising a current mirror circuit included in the processing circuit, the current mirror circuit being configured to receive the reference and intensity voltages and operable to generate an output current representative of the difference between the reference and intensity voltages.

7. The circuit of claim **6** further comprising an A/D converter circuit configured to receive the output current and operable to generate a digital output relative to the output current.

8. A digital camera comprising:

a CMOS active pixel sensor circuit containing a plurality of pixels connected to a column line, each pixel containing a photo sensing diode and at least one transistor, the photo sensing diode operable to generate an intensity voltage on the column line when light is incident on the pixel and to generate a reference voltage when light is not incident on the pixel; and

a circuit for coupling the intensity and reference voltages to a processing circuit, comprising:

a first pair of switches coupling an intensity input node to which the intensity voltage is applied to a first output node and coupling a reference input node to which the reference voltage is applied to a second output node during a first operating period;

a second pair of switches coupling the intensity input node to the second output node and coupling the ref-

erence input node to the first output node during a second operating period; and

a polarity reversing circuit included in the processing circuit, for coupling the first and second output nodes to the processing circuit with one polarity during the first operating period and in a reverse polarity during the second operating period.

9. The digital camera of claim **8** wherein the circuit for coupling the intensity and reference voltages to a processing circuit further comprises a toggle switch coupled to the first and second pair of switches, the toggle switch being configured to receive a select signal and operable responsive to the select signal to enable the first pair of switches during the first operating period and to enable the second pair of switches during the second operating period.

10. The digital camera of claim **9** wherein the circuit for coupling the intensity and reference voltages to a processing circuit further comprises a current mirror circuit included in the processing circuit, the current mirror circuit being configured to receive the reference and intensity voltages and operable to generate an output current representative of the difference between the reference and intensity voltages.

11. The digital camera of claim **10** wherein the circuit for coupling the intensity and reference voltages to a processing circuit further comprises an A/D converter circuit configured to receive the output current and operable to generate a digital output relative to the output current.

12. A method for coupling an intensity voltage and a reference voltage from an active pixel sensor to a processing circuit, the method comprising:

coupling an intensity input node to which the intensity voltage is applied to a first output node and coupling a reference input node to which the reference voltage is applied to a second output node during a first operating period;

coupling the intensity input node to the second output node and coupling the reference input node to the first output node during a second operating period; and

coupling the first and second output nodes to the processing circuit with one polarity during the first operating period and in a reverse polarity during the second operating period.

13. The method of claim **12** further comprising generating an output current representative of the difference between the reference and intensity voltages.

14. The method of claim **13** further comprising generating a digital output relative to the output current.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.   : 7,515,188 B2   Page 1 of 1
APPLICATION NO. : 10/892875
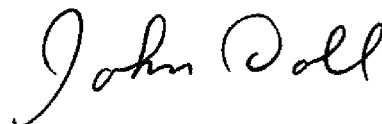DATED   : April 7, 2009
INVENTOR(S)   : Baker

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 5, line 14, in Claim 5, after "switch" delete "adapted".

Signed and Sealed this

Seventh Day of July, 2009

John Doll

JOHN DOLL
Acting Director of the United States Patent and Trademark Office