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Baker

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(54) **METHODS FOR RESISTIVE MEMORY ELEMENT SENSING USING AVERAGING**

(75) Inventor: **R. Jacob Baker**, Meridian, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

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See application file for complete search history.

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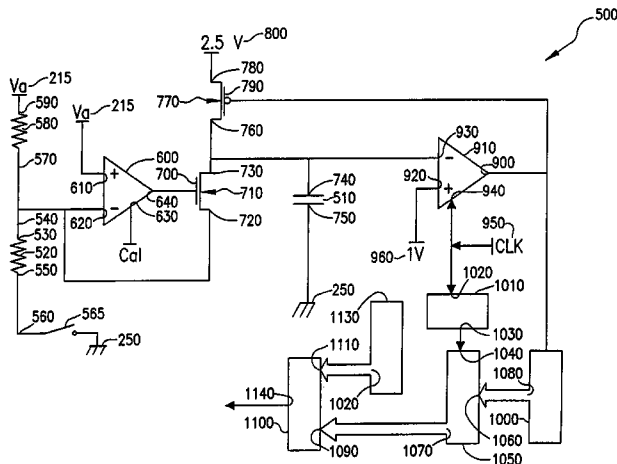FOREIGN PATENT DOCUMENTS

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Primary Examiner—Andrew Q. Tran
(74) *Attorney, Agent, or Firm*—Dickstein Shapiro LLP

(57) **ABSTRACT**

A system for determining the logic state of a resistive memory cell element, for example an MRAM resistive cell element. The system includes a controlled voltage supply, an electronic charge reservoir, a current source, and a pulse counter. The controlled voltage supply is connected to the resistive memory cell element to maintain a constant voltage across the resistive element. The charge reservoir is connected to the voltage supply to provide a current through the resistive element. The current source is connected to the charge reservoir to repeatedly supply a pulse of current to recharge the reservoir upon depletion of electronic charge from the reservoir, and the pulse counter provides a count of the number of pulses supplied by the current source over a predetermined time. The count represents a logic state of the memory cell element.

13 Claims, 6 Drawing Sheets

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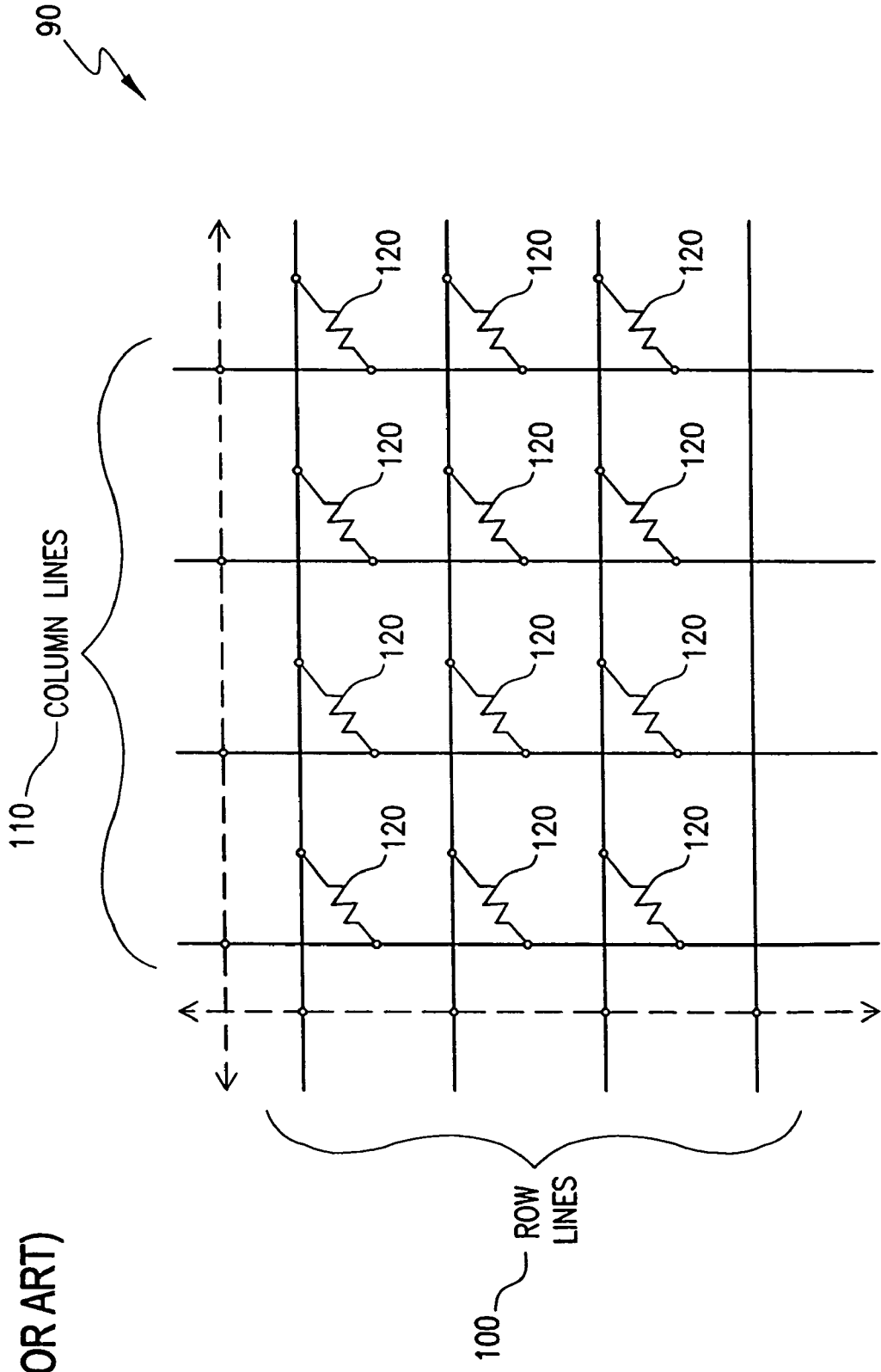|				
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FIG. 1
(PRIOR ART)

FIG. 2

FIG. 3

FIG. 4

FIG. 5

FIG. 6

FIG. 7

1200

CPU
1220

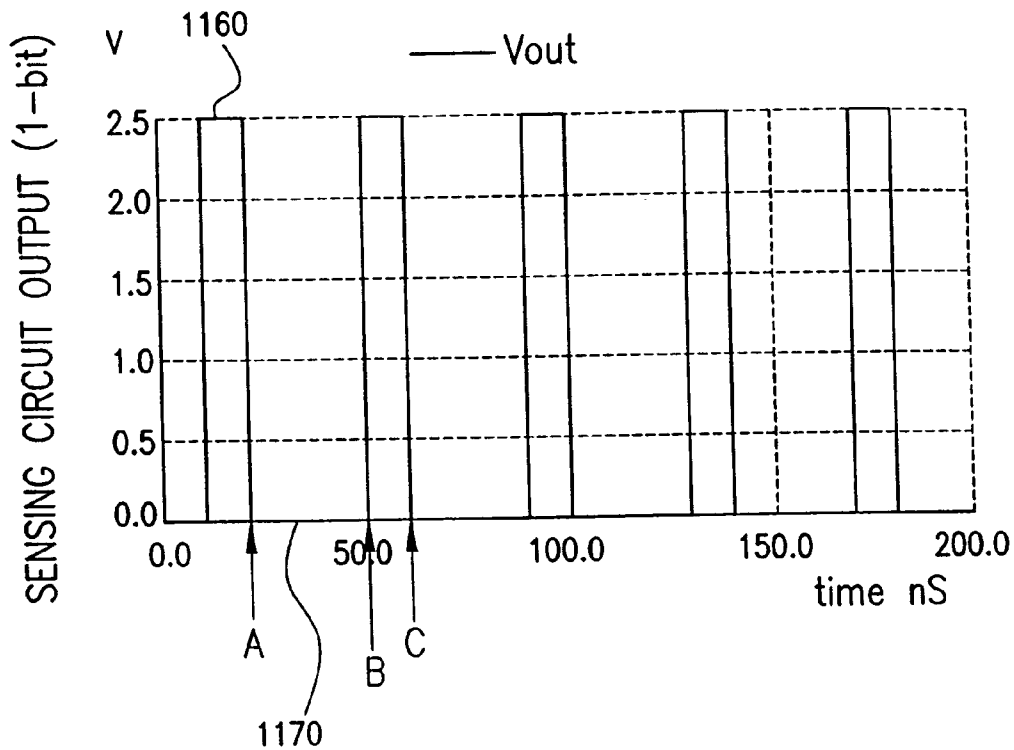DISK STORAGE
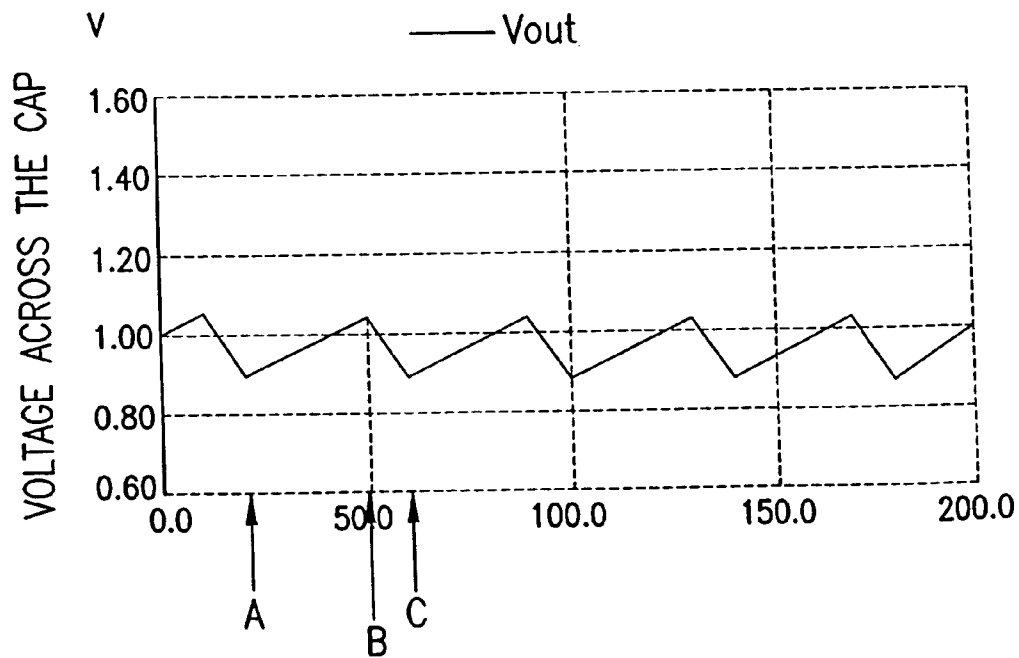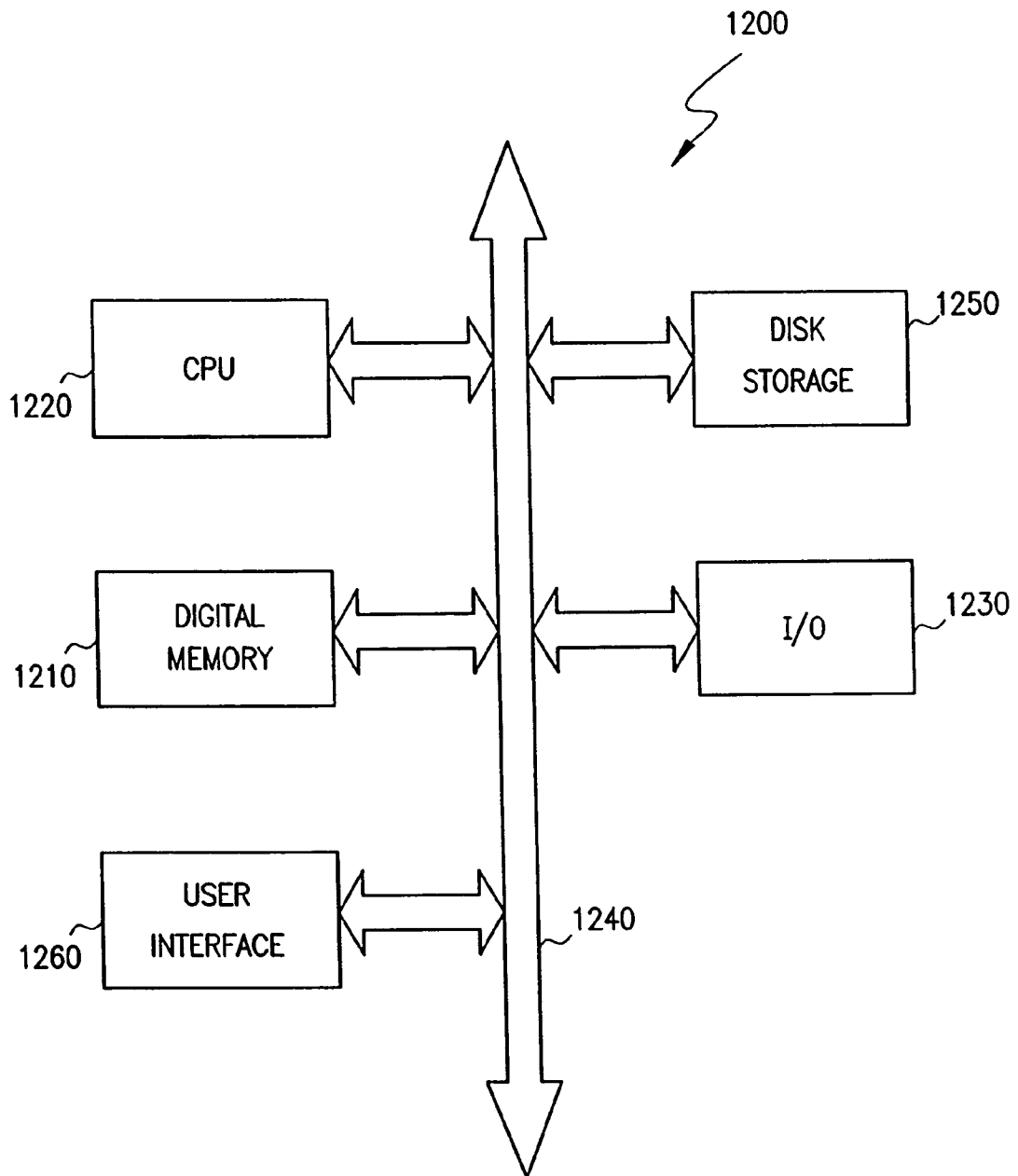1250

DIGITAL MEMORY
1210

I/O
1230

USER INTERFACE
1260

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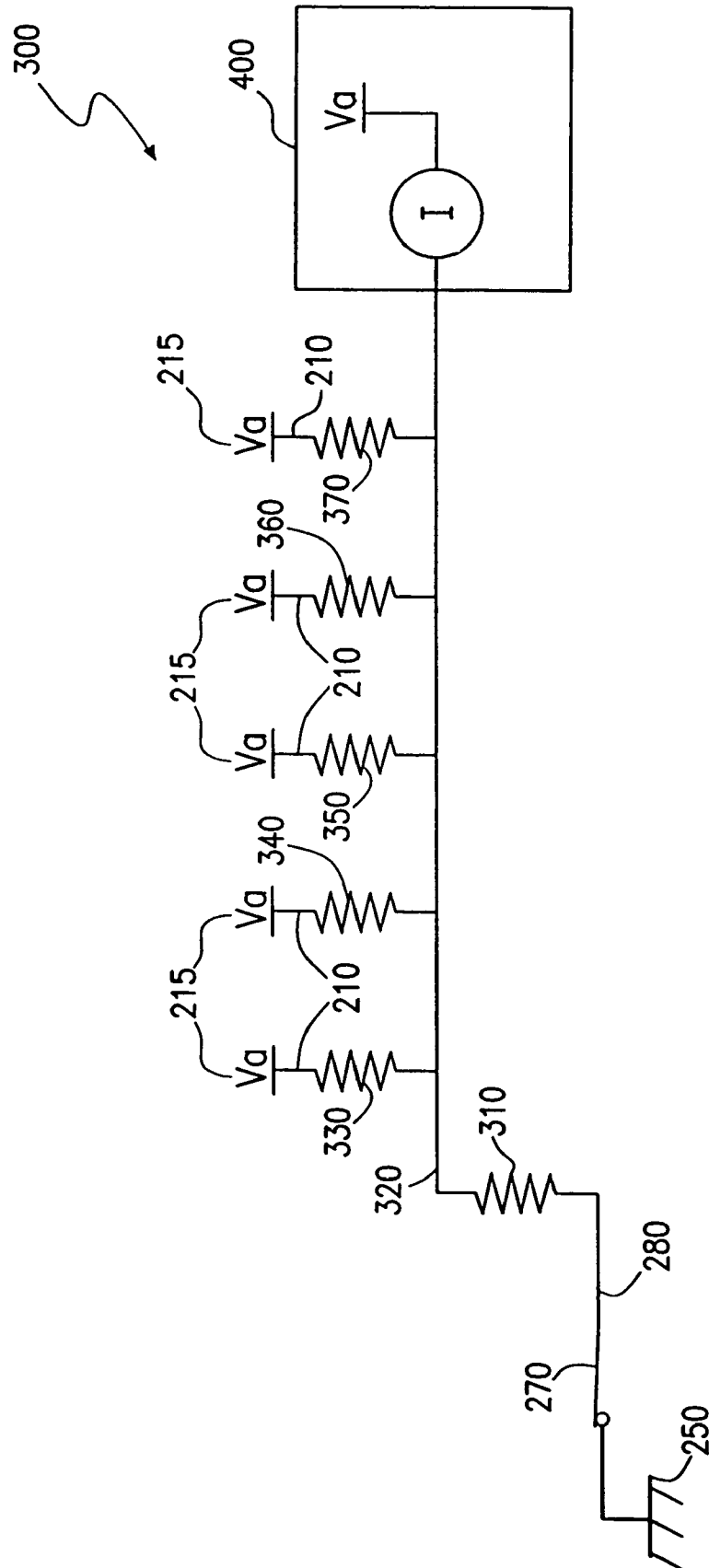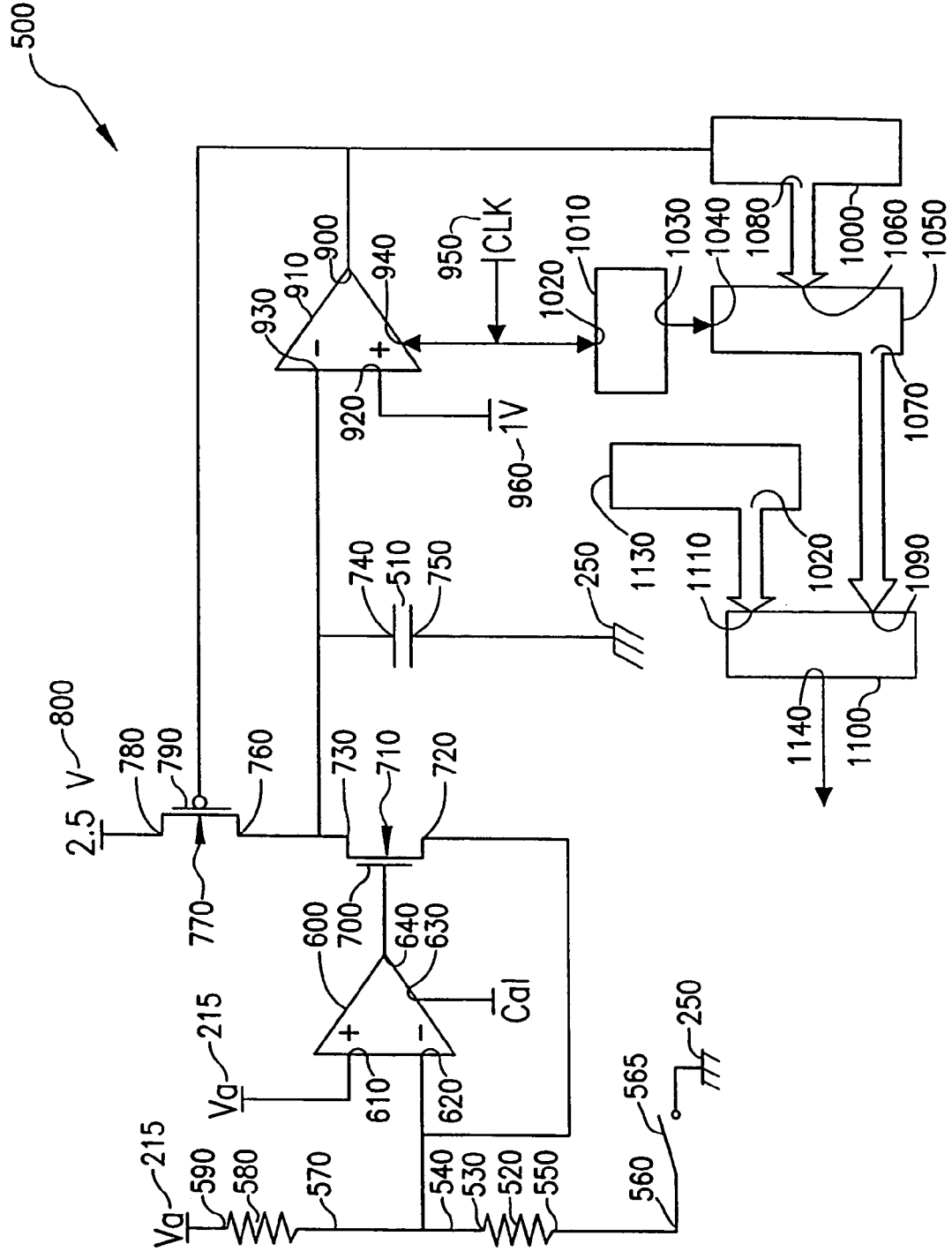
METHODS FOR RESISTIVE MEMORY ELEMENT SENSING USING AVERAGING

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a division of U.S. patent application Ser. No. 10/674,550, filed on Oct. 1, 2003, now U.S. Pat. No. 7,133,307 which in turn is a continuation application of U.S. patent application Ser. No. 10/290,297, filed on Nov. 8, 2002, now U.S. Pat. No. 6,822,892 which in turn is a divisional application of U.S. patent application Ser. No. 09/938,617, filed on Aug. 27, 2001 (now U.S. Pat. No. 6,504,750, issued on Jan. 7, 2003), the entire disclosures of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of resistor-based memory circuits. More particularly, it relates to a method for precisely sensing the resistance value of a resistor-based memory cell, for example, an MRAM magnetic memory cell.

2. Description of the Related Art

FIG. **1** shows one example of a resistor based memory. The memory includes a memory cell array **90** having a plurality of row lines **100** arranged in normal orientation to a plurality of column lines **110**. Each row line is connected to each of the column lines by a respective of resistor **120**.

A magnetic random access memory (MRAM) is one approach to implementing a resistor based memory. In an MRAM, each resistive memory cell includes a magnetizable film. The resistance of the cell varies, depending on the magnetization state of the film. Logical data can be stored by magnetizing the film of particular cells so as to represent logic states of the data. The stored data can be read by measuring the resistance of the cells, and interpreting the resistance values measured as logic states. Making the required resistance measurements, however, is problematic.

In a resistance memory, one resistance value, e.g., a higher value, may be used to signify a logic "HIGH" while another resistance value, e.g., a lower value, may be used to signify a logic "LOW." The stored logic state can be detected by measuring the memory cell resistance using Ohm's law. For example, resistance is determined by holding voltage constant across a resistor and measuring, directly or indirectly, the current that flows through the resistor. Note that, for MRAM sensing purposes, the absolute magnitude of resistance need not be known; only whether the resistance is above or below a value that is intermediate to the logic high and logic low values.

Sensing the logic state of an MRAM memory element is difficult because the technology of the MRAM device imposes multiple constraints. In a typical MRAM device an element in a high resistance state has a resistance of about 1MΩ. An element in a low resistance state has a resistance of about 950KΩ. The differential resistance between a logic one and a logic zero is thus about 50 KΩ, or 5% of scale.

Accordingly, there is a need for a simplified resistance measuring circuit able to repeatably and rapidly distinguish resistance values varying by less than 5% on a one MΩ scale.

BRIEF SUMMARY OF THE INVENTION

The invention provides a method and apparatus for measuring the resistance of a resistive memory element. The resistance is measured by charging a capacitor, allowing the capacitor to discharge through a selected resistive memory element while maintaining a substantially constant voltage across the resistive memory element, sensing the charge remaining on the capacitor, repeatedly recharging the capacitor with a pulse of definite charge each time the capacitor voltage drops to a predetermined value, and determining a time average current into the capacitor based on a duty cycle of the recharging pulses. Knowledge of the time average current into the capacitor yields the current flowing into the resistor since the current flowing into the capacitor must equal the current flowing out of the capacitor and into the resistor. One can measure or set the voltage across the resistive memory element and determine the resistance of the element from the current through the element and the voltage across it.

In various aspects of the invention, the actual resistance of the memory element is not calculated. Instead, the number of capacitor charging pulses is counted, and the numerical count thus acquired is compared to a reference count value. The reference value is chosen to lie between count values representing logical one and logical zero. Therefore a count value greater than the reference indicates one logical state, and a count value less than the reference value indicates another. In a further aspect of the invention, more than one reference value is established, and a memory element capable of exhibiting more than two resistance values is used. Consequently the memory element may store more than two logical values. The logical values are determined based on the relationship between the count value counted and the standard values used to establish thresholds between logical values.

In a further aspect, the apparatus and method of the invention may be used to measure the resistance or impedance of any resistive or impedance device.

These and other aspects and features of the invention will be more clearly understood from the following detailed description which is provided in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a conventional magnetic random access memory array in schematic form;

FIG. **2** shows a magnetic random access memory device according to one aspect of the present invention in schematic form, including resistance sensing circuits;

FIG. **3** shows a portion of a magnetic random access memory device according to one aspect of the invention including a sensing circuit and sneak resistance;

FIG. **4** shows a circuit for sensing resistance using averaging according to one aspect of the present invention;

FIG. **5** shows a graphical representation of sensing circuit digital output over time according to one aspect of the present invention;

FIG. **6** shows a graphical representation of voltage across a capacitor over time according to one aspect of the present invention;

FIG. **7** shows a computer system incorporating a digital memory according to one aspect of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **2** shows a portion of a resistive memory device according to the invention. The device includes an array **200** of Magnetic Random Access Memory (MRAM) elements, a plurality of electrically conductive row lines **210**, and a plurality of electrically conductive column lines **220**. Each row line is connected to each of the plurality of column lines by a respective MRAM resistive element **230**. A plurality of switches **240**, typically implemented as transistors, are each switchingly connected between one of the row lines and a first source of constant potential (ground) **250**. A plurality of sensing circuits **260**, are respectively connected to the plurality of column lines **220**. Each sensing circuit **260** includes a source of constant electrical potential (V_A) which is applied to the respective column line. A plurality of pull-up voltage sources **215**, supplying voltage V_A, are respectively connected to each of the plurality of row lines **210**.

In operation, an exemplary switch **240**, such as switch **270** associated with a particular row line **280**, is dosed so as to bring that row line to ground potential and a particular column line, e.g., **320** is sensed to read the resistance value of a particular resistor **310**.

FIG. **3**, shows the resulting electrical circuit for the relevant portion **300** of the memory array when row **280** is grounded. As shown, memory element **310** to be sensed is connected between a grounded row line **280** and a particular column line **320**. Also connected to the column line **320** are a plurality of other resistive memory elements (e.g. elements **330**, **340**, **350**, **360**, **370**) each of which is connected at its opposite end to a pull-up voltage source V_A **215** through a respective row line **210**. In addition, a respective sensing circuit **400** is connected to the column line **320**. The sensing circuit **400** includes a voltage supply that maintains the column line **320** at electrical potential V_A.

The other resistive memory elements (those tied to ungrounded row lines) **330**, **340**, **350**, **360**, **370**, form an equivalent resistance referred to as sneak resistance. The effective resistance of the sneak resistance is small. A typical value for sneak resistance might be 1 KΩ. Nevertheless, because both ends of each ungrounded resistor are ideally maintained at the same potential (here V_A) as the column line **320**, net current flow through the sneak resistance is desirably nearly zero.

In contrast, a measurable current flows through the grounded resistor memory element **310**. This measurable current allows evaluation of the resistance of the memory element **310** by the sensing circuit **400**.

One proposal for sensing the resistance value of a memory cell is to charge a capacitor to a predetermined first voltage and then discharge the capacitor through the memory cell resistance until it holds a second lower predetermined voltage. The time taken for the capacitor to discharge from the first to the second voltage is a measure of cell resistance. A problem with this approach is that since the resistance values representing the different logic states of a cell are very close in value (only 5% difference) it is difficult to obtain an accurate and reliable resistance measurement, even if digital counting techniques are employed to measure the discharge time of the capacitor.

Thus, even when using digital counting techniques, the discharge capacitor must be counted quite precisely to sense the different resistance values and distinguish logic states. To achieve this precision, either the counting clock must be operated at a high frequency or the capacitor must be disc relatively slowly. Neither of these options is desirable, since

slow capacitor discharge means slow reading of stored memory values, and a high clock frequency requires high frequency components. In either case, a counter having a large number of stages is also required.

The present invention provides a resistive measuring circuit and operating method which rapidly ascertains a resistive value without storing large data counts, and without requiring highly precisioned components.

FIG. **4** illustrates an exemplary embodiment of a resistance sensing circuit **500** constructed in accordance with the invention. Sensing circuit **500** relies on the cyclical discharge of a capacitor **510** to determine the value of a memory cell resistance **520**. The duty cycle of a recharging signal for the capacitor **510** represents a value of resistance **520**.

The resistance measuring circuit **500** outputs a bit stream from an output **900** of a comparator **910**. The ratio of logic one bits to a total number of bits (or, in and other aspect of the invention, the ratio of logic one bits to logic zero bits) in the bit stream yields a numerical value. This numerical value corresponds to the current that flows through the resistance **520** in response to a known applied voltage. For example, assume that a current source can deliver current at two discrete current levels, corresponding to two different states of a logical input signal. When the signal is in logic one state, the source delivers, for example, 2 μA. When the signal is in a logic zero state, the source delivers, for example, 0 μA. The logical input signal is monitored over a finite time span corresponding to a number of bit-length time periods. Over that time span, the number of logic one and logic zero bits are recorded. By straightforward algebra, the average current delivered by the current source over the corresponding time span may be calculated as follows:

$$IAVG = \frac{\text{(number of logic 1 bits)} * 2 \ \mu A + \text{(number of logic 0 bits)} * 0 \ \mu A}{\text{total number of bits in the signal}}$$

As an example, if, over a time span corresponding to 4 cycles, there is one logic one bit and three logic zero bits then the average current over the four cycles is 0.5 μA.

$$IAVG = \frac{1 * 2 \ \mu A + 3 * 0 \ \mu A}{4} = 0.5 \ \mu A$$

The operation of the FIG. **4** sensing circuit is now described in greater detail. An MRAM resistive memory element **520** to be sensed has a first end **530** connected to a column line **540** and a second end **550** connected to ground **250** through a row line **560** and switch **565**. Also connected to the column line **540** is a first end **570** of a sneak resistance **580**. The sneak resistance has a second end **590** connected to a source of constant potential V_A **215**. The sneak resistance **580** represents a plurality of MRAM resistive elements associated with the particular column line **540** and with a respective plurality of unselected row lines, as described above with reference to FIG. **3**.

A first operational amplifier (op-amp) integrator **600** is provided which has a non-inverting (positive) input **610**, an inverting (negative) input **620**, a calibrate offset input **630**, and an output **640**. The output **640** of the first op-amp **600**

is connected to a control input (gate) 700 of a first transistor 710, which in this exemplary embodiment is an N-channel transistor.

The first transistor 710 includes a drain 720 connected to both the selected column line 540 and the inverting input 620 of the first op-amp 600. The first transistor also includes a source 730 operatively connected to a first terminal 740 of a capacitor 510. The capacitor 510 includes a second terminal 750 operatively connected to a ground potential 250. The source 730 of the first transistor 710 is also connected to a drain 760 of a second transistor 770. In this exemplary embodiment, this second transistor 770 is a PMOS transistor. The second transistor 770 includes a source 780 and a gate 790, in addition to the drain 760. The source 780 is operatively connected to a supply voltage 800, which in this exemplary embodiment is 2.5 volts. The gate 790 is operatively connected to an output 900 of a clocked comparator 910. The clocked comparator 910, shown as a clocked second operational amplifier, includes the output 900, a non-inverting (positive) input 920, an inverting (negative) input 930, and a clock input 940 connected to a source of a clock signal 950. The comparator 910 may be implemented as a simple clocked latch, or the comparator 910 may be simply enabled by the clock CLK signal.

The output 900 of the second op-amp is also connected to a counter 1000 which counts the rising transitions at the comparator output 900. The non-inverting input 920 of the second op-amp 910 is connected to a source of a reference voltage 960 (1 volt in the exemplary embodiment shown).

A second counter 1010 counts the total number of transitions of the clock 950 during a measuring cycle. This counter 1010 includes an input 1020 for receiving clock signal 950 and at output 1030 that exhibits a signal when counter 1010 reaches a predetermined count. The output 1030 is connected to a latch input 1040 of a latching buffer 1050. The latching buffer 1050 includes a data input 1060 and data output 1070. The data input 1060 is connected to a data output 1080 of the first counter 1000. The data output 1070 is connected to a first data input 1090 of a digital comparator 1100. The digital comparator 1100 includes a second data input 1110 connected to a data output 1120 of a source of a reference value 1130. In one embodiment, the source of the reference value 1130 is a buffer or other device holding a digital number.

The sensing circuit 500 operates in the following manner when activated when a row line is grounded and a resistance value is to be sensed. Capacitor 510 is initially discharged, resulting in a negative output signal on the output 900 of the second op-amp 910. This causes the second transistor 770 to be placed in a conductive state, permitting capacitor 510 to begin charging. When the voltage on capacitor 510 equals that applied to the non-inverting input 920 of the second op-amp 910 (here 1 volt), the output 900 of the second op-amp changes state to a positive value at the next transition of the clock 950. This turns off the second transistor 770. The charge stored on capacitor 510 is discharged through the first transistor 710 and cell resistance 520 under the control of the first op-amp 600. The first op-amp 600 tries to maintain a constant voltage V_A on the selected column line 540.

As charge is depleted from capacitor 510 the voltage on the capacitor drops until it falls below the voltage (1 volt) applied to the reference input 920 of the clocked comparator 910. After this threshold is passed, the next positive clock transition applied to the clock input 940 causes the output of comparator 910 to go low again turning on the second

transistor 770 and causing current to begin flowing through the second transistor 770 to recharge capacitor 510.

In one embodiment, the capacitor 510 is recharged during one clock cycle of clock source 950, so the comparator output 900 switches to high and the second transistor 770 is shut off again at the next positive clock transition. Transistor 770 is sized to allow a substantially constant current (e.g., 2.5μA) to flow to capacitor 510 when transistor 770 is in a conductive state.

The described charging and discharging of capacitor 510 under the control of the first 710 and second 770 transistors occurs repeatedly during one sense cycle. Each time the output of the comparator 910 goes low, a current pulse is allowed to pass through the second transistor 770 and the first counter 1000 incremented. Each time the clock signal 950 transitions positive, the second counter 1010 is incremented. When the second counter 1010 reaches a preset value, it triggers the latch 1050, which latches that number of pulses counted by the first counter 1000 during the sensing period. The number of pulses counted is latched onto the data output 1070 (and data input 1090). The comparator 1100 then evaluates the values presented at the first and second data inputs 1090, 1110, and ascertains whether the value at the first data input 1090 is larger or smaller than the reference value at the second data input 1110. The reference value at input 1110 is set between two count values which correspond to "hi" and "low" resistance states for resistor 520. Thus if the value of the first data input 1090 is larger than the reference value, then a first logical value (e.g. logic one) is output on an output 1140 of the digital comparator 1100. If the value of the first data input 1090 is smaller than the reference value, then a second logical value (e.g. logic zero) is output on the output 1140 of the digital comparator 1100. In a variation, a comparator 1100 capable of comparing the digital value applied at the data input 1090 to a plurality of reference values 1110 can distinguish a value stored in a single resistive memory element as between multiple resistance values. In a further variation, the capacitor 510 is pre-charged prior to a measuring cycle. By pre-charging the capacitor 510, the number of cycles of the clock signal 950 required to measure the state of the memory element is reduced. In another variation the capacitor is not pre-charged, in which case sensing the resistance of the memory dement takes longer, but the circuitry and/or process is simplified.

FIGS. 5 and 6 show an exemplary relationship between the output signal produced at output 900 of the clocked comparator 910 and the voltage on capacitor 510 over time. FIG. 5 shows the output signal produced by the clocked, comparator when a 100 MHz clock signal is applied to the clock input 940. At a clock frequency of 100 MHz, clock pulses are spaced at an interval of 10 ns. In the example shown, the output of the clocked comparator is high 1160 for one clock pulse (10 ns) and low 1170 for three clock pulses (30 ns). This corresponds to the voltage waveform shown in FIG. 6. In FIG. 6, the voltage of the capacitor 510 is shown to begin rising when the output 900 of the clocked comparator goes low (time A), thereby turning on the PMOS transistor 770. The voltage rises for 30 ns, or three clock pulses until time B. At time B, the output of the clocked comparator goes high again, turning off the PMOS transistor. The voltage on the capacitor 510 then begins to drop again while the PMOS device remains off for one clock pulse, or 10 ns (until time C). Accordingly, in the example shown, the duty cycle of the signal output by the clocked comparator 910 is 75% (three on-pulses for every off-pulse).

FIG. **7** shows a computer system **1200** including a digital memory **1210** having a resistance measuring memory cell sensor according to the invention. The computer **1200**, as shown includes a central processing unit (CPU) **1220**, for example, a microprocessor, that communicates with one or more input/output (I/O) devices **1230** over a bus **1240**. The computer system also includes peripheral devices such as disk storage **1250** and a user interface **1260**. It may be desirable to integrate the processor and memory on a single IC chip.

While preferred embodiments of the invention have been described and illustrated above, it should be understood that these are exemplary of the invention and are not to be considered as limiting. Additions, deletions, substitutions, and other modifications can be made without departing from the spirit or scope of the present invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.

The invention claimed is:

1. A method of measuring the value of a resistance comprising:

producing a plurality of electrical pulses at a rate related to the resistance;

counting the electrical pulses over a predetermined time period to produce a pulse count; and

evaluating the pulse count to determine the resistance.

2. The method of claim **1**, wherein each electrical pulse comprises a pulse of substantially uniform width.

3. The method of claim **1**, wherein the evaluating comprises comparing the pulse count to a reference pulse count to determine the value of the resistance.

4. The method of claim **3**, wherein the evaluating further comprises determining the resistance as one value if the pulse count is above the reference pulse count and as another value if the pulse count is below the reference pulse count.

5. A method of measuring an impedance comprising:

applying a substantially uniform voltage across the impedance;

flowing a substantially uniform current into the impedance from a charge reservoir;

flowing a plurality of current pulses into the charge reservoir;

controlling the flow of the plurality of current pulses in response to a quantity of charge in the charge reservoir;

counting the plurality of current pulses over a definite time to produce a pulse count; and

relating an impedance value to the pulse count.

6. The method of claim **5**, wherein the impedance comprises an electrical resistance.

7. The method of claim **5**, wherein the impedance comprises a capacitance.

8. The method of claim **5**, wherein the impedance comprises an inductance.

9. A method for making a memory integrated circuit comprising steps of:

assembling a first circuit for conducting current from a capacitor through a resistor, the first circuit including a controlled current source for delivering current to the capacitor;

providing a comparator for comparing a voltage on the capacitor to a reference voltage and supplying a pulse to turn on the current source when the voltage on the capacitor falls below the reference voltage;

operatively connecting a pulse counter to the comparator output for counting pulses generated by the comparator; and

providing a second circuit for determining the value of the resistance based on a count value stored in the pulse counter.

10. The method of claim **9**, further comprising providing a clock input to the comparator, and arranging the comparator such that the output of the comparator changes state only when a clock signal applied to the clock input changes state.

11. The method of claim **9** , further comprising arranging the second circuit to compare the value stored in the pulse counter to a reference value and determine whether the stored value is greater or less than the reference value.

12. The method of claim **11**, further comprising steps of:

assembling the first circuit to include a transistor having a source operatively connected to the capacitor, a gate, and a drain; and

operatively connecting a differential amplifier having a non-inverting input connected to a first reference voltage, an output operatively connected to the gate, and an inverting input operatively connected to the drain and to the resistor.

13. The method of claim **12**, further comprising including in the second circuit a digital comparator adapted to receive the value stored in the pulse counter, receive the reference value, and compare the stored value to the reference value to produce an output.

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