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(54) **METHOD OF OPERATING A COMPLEMENTARY BIT RESISTANCE MEMORY SENSOR**

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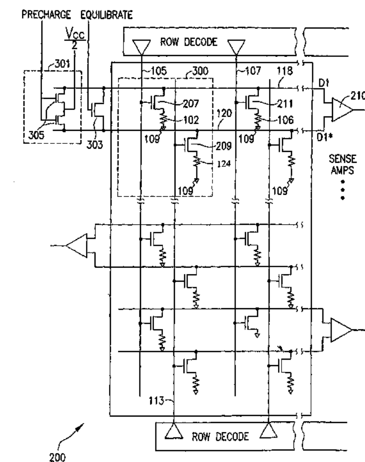
(57) **ABSTRACT**

The present invention relates to a method and apparatus for sensing the resistance state of a programmable resistance memory, using complementary memory elements, one holding the resistance state being sensed and the other holding a complementary resistance state. A sense amplifier detects voltages discharging through the resistance elements to determine the resistance state of an element being read.

16 Claims, 6 Drawing Sheets



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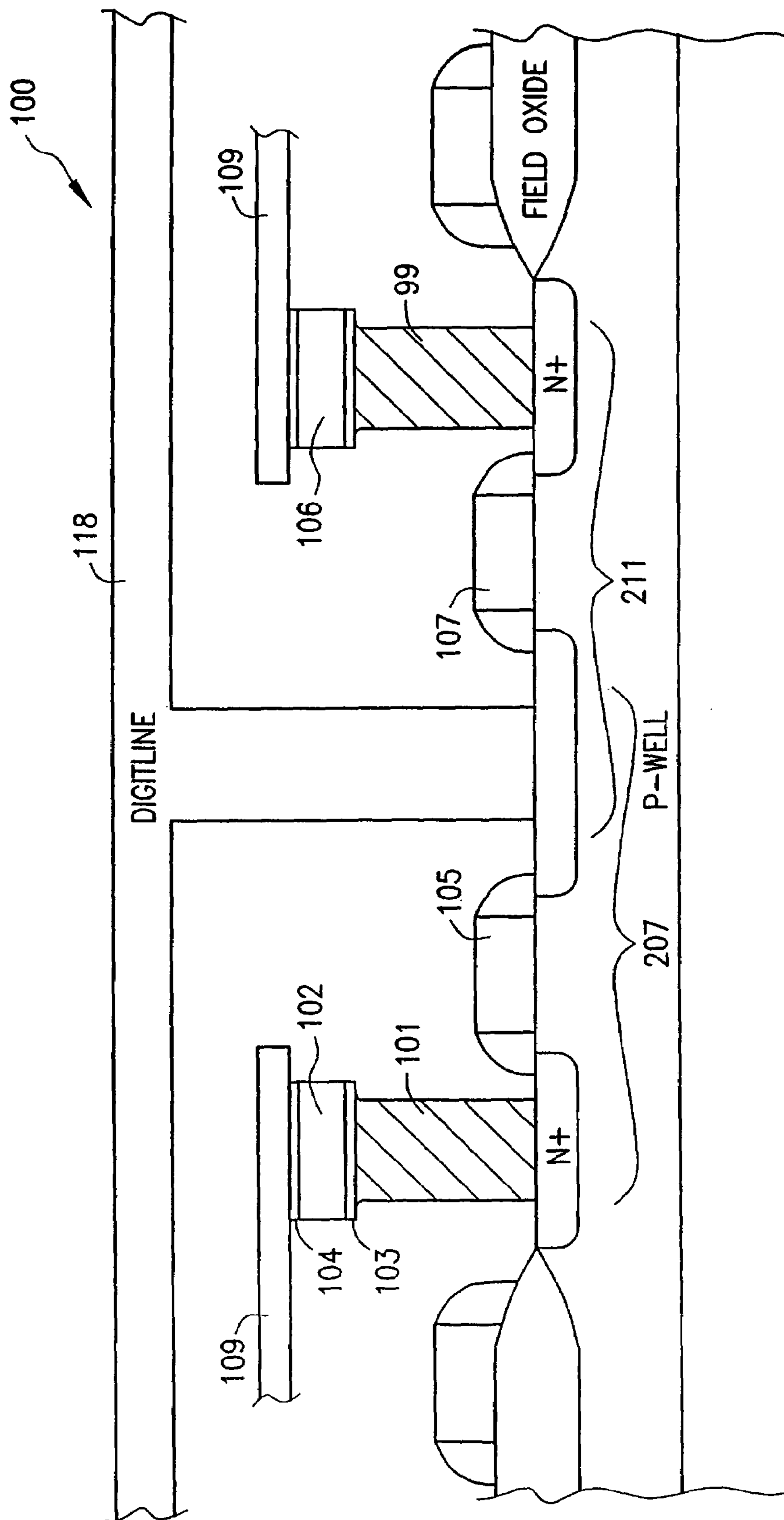
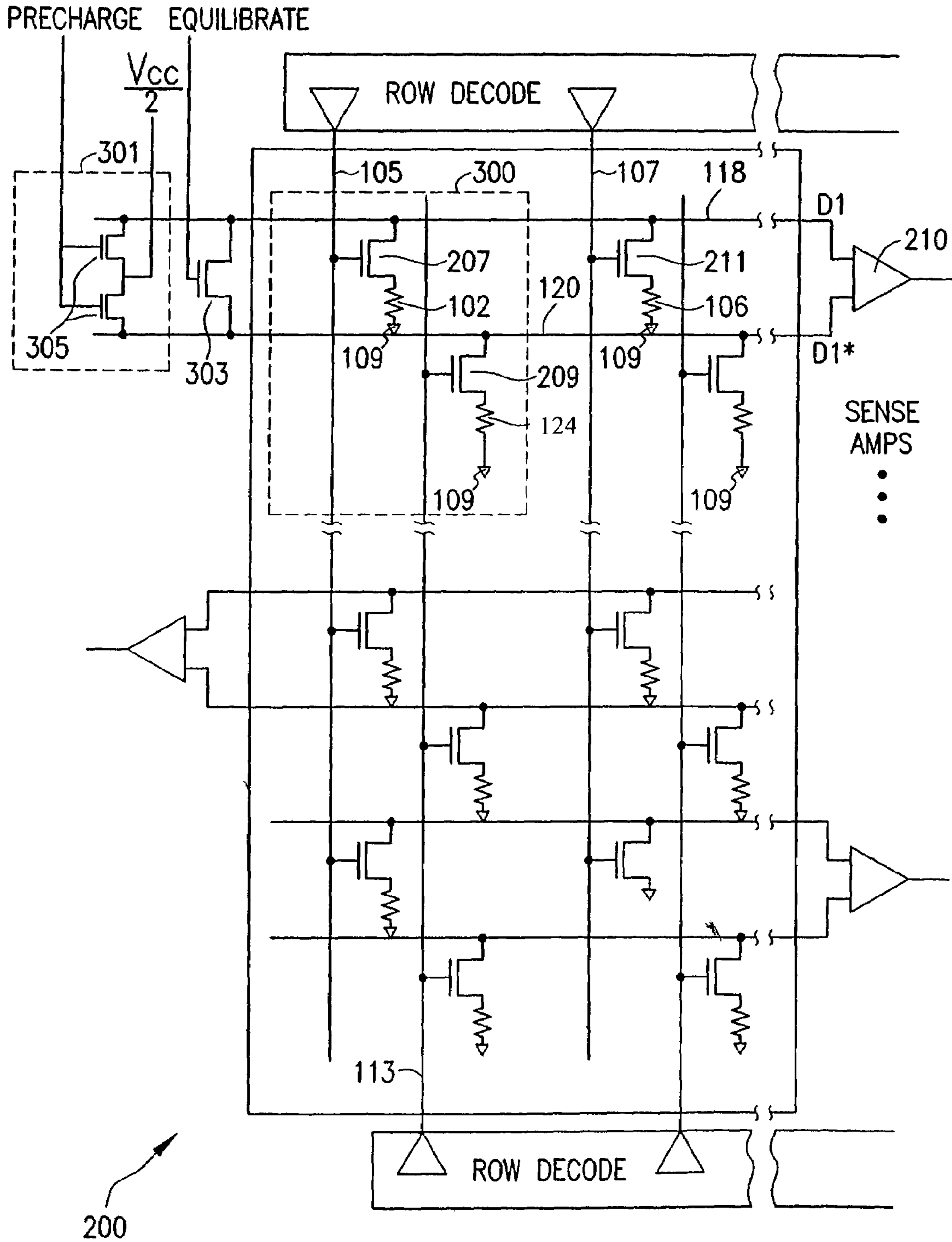


FIG. 1

FIG. 2



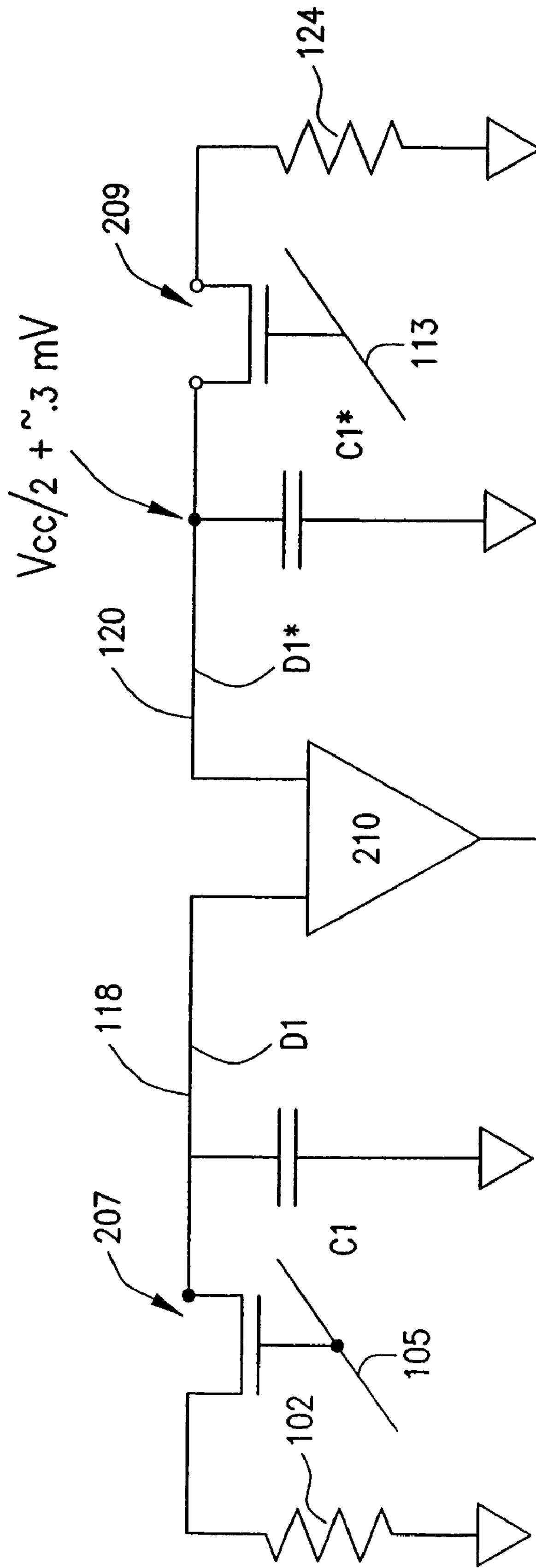


FIG. 3

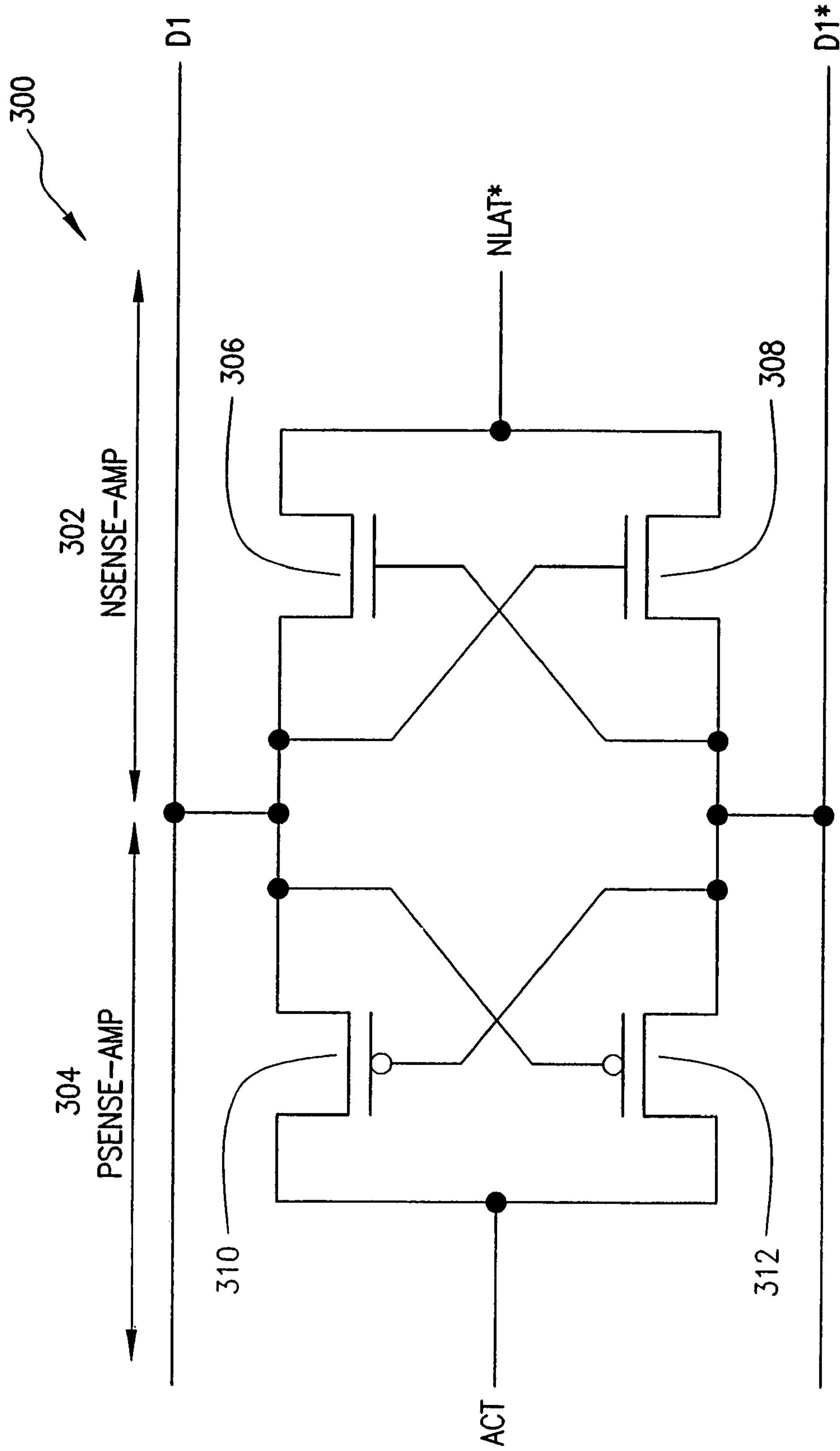


FIG. 4

FIG. 5

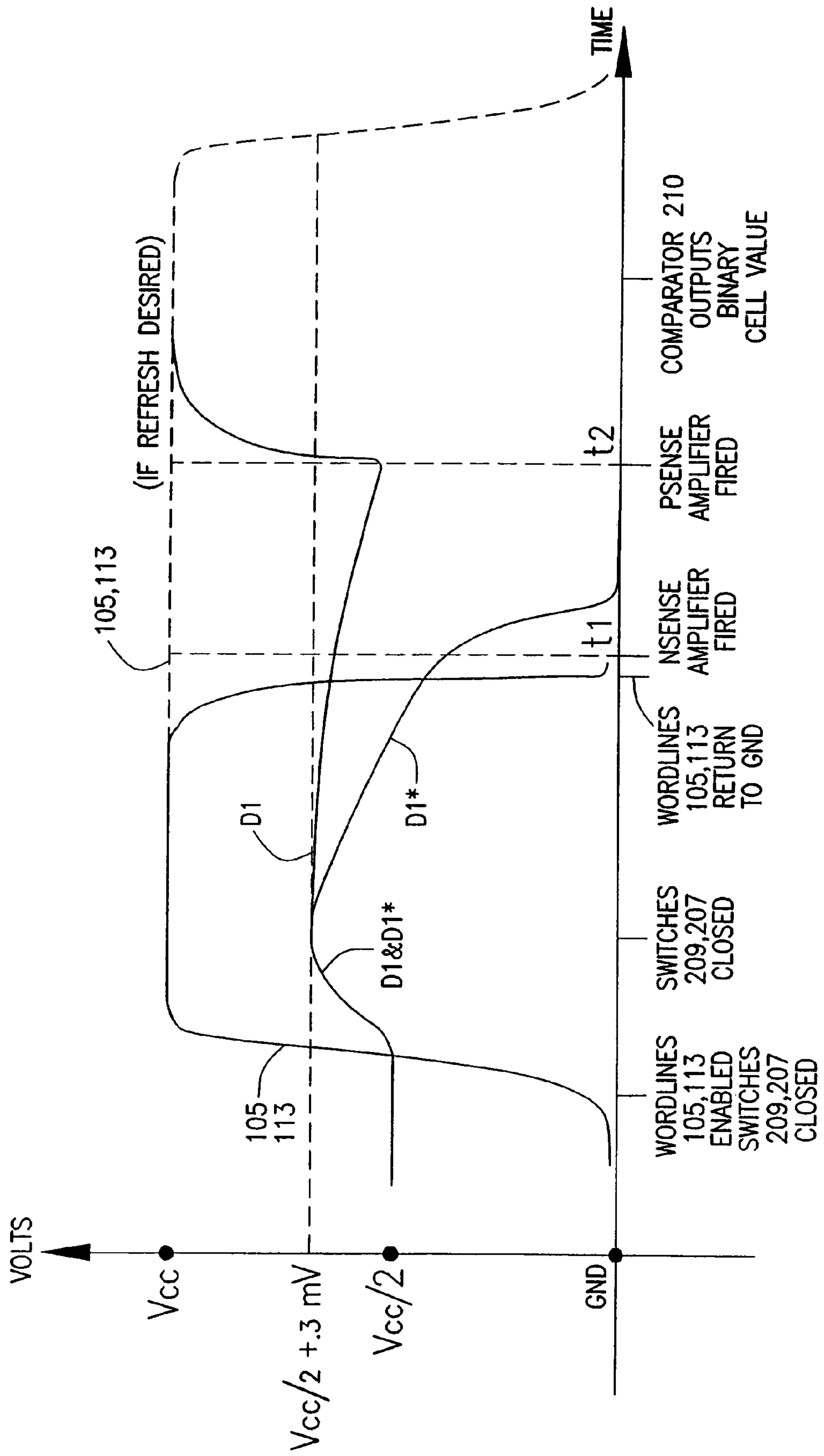
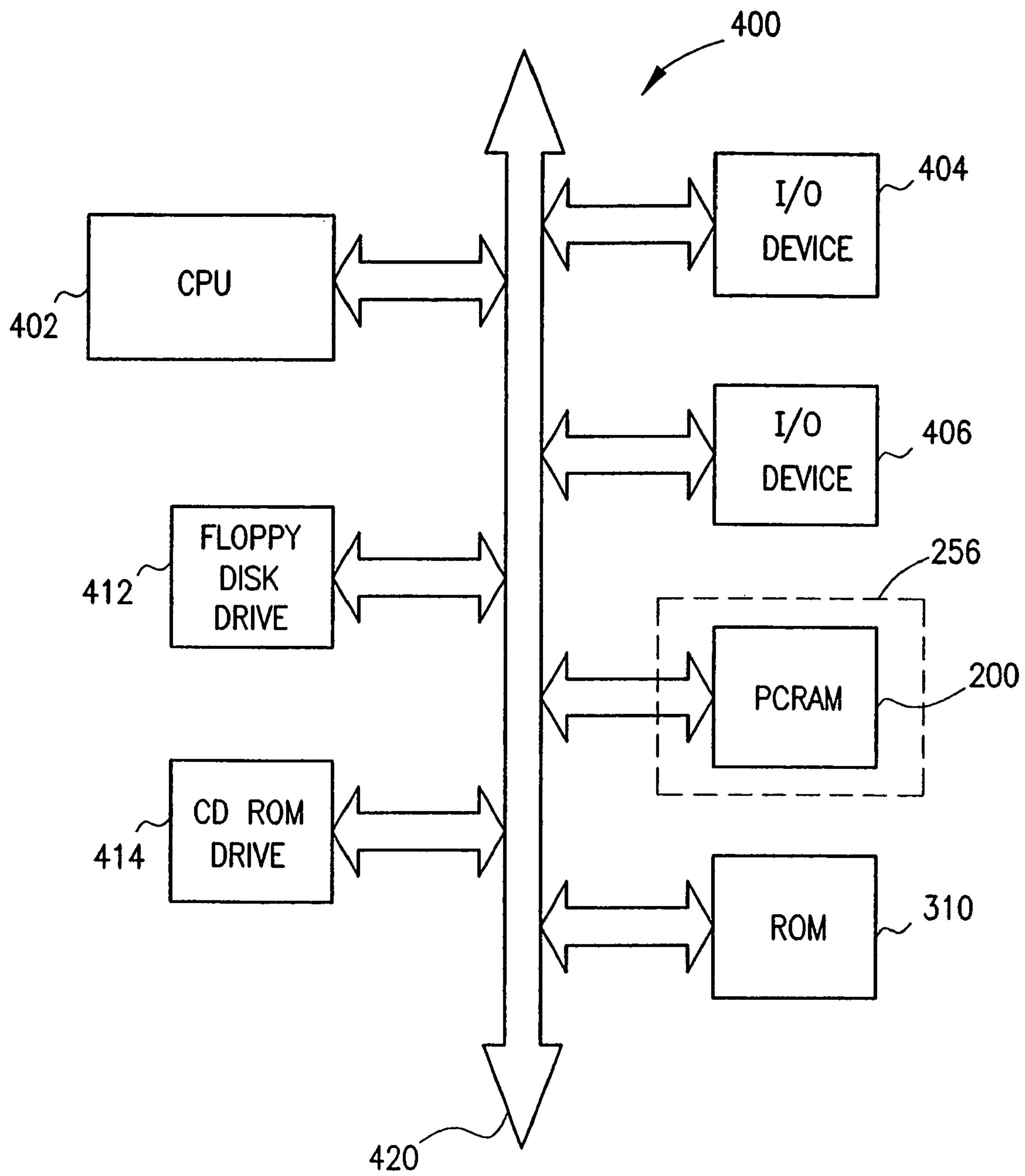


FIG. 6



METHOD OF OPERATING A COMPLEMENTARY BIT RESISTANCE MEMORY SENSOR

This application is a divisional of Application Ser. No. 10/866,091, filed Jun. 14, 2004 now U.S. Pat. No. 7,002,833, which is a continuation of application Ser. No. 09/988,627, filed Nov. 20, 2001, now U.S. Pat. No. 6,791,859, the entire disclosures of which are incorporated herein by reference.

FIELD OF THE INVENTION

The invention relates to a method and apparatus for sensing the resistance of a Programmable Conductor Random Access Memory (PCRAM) element.

BACKGROUND OF THE INVENTION

PCRAM devices store binary data as two different resistance values, one higher than the other. The resistance value represents a particular binary value of logic "0" or logic "1". When sensing the resistance value of a PCRAM device, it is common to compare the resistance of a memory cell undergoing a read operation with resistance of a reference cell to determine the resistance value of the cell being read and thus its logic state. Such an approach is disclosed in U.S. Pat. No. 5,883,827. However, this approach has some limitations.

If the reference cell is defective and a column of memory cells within an array uses a same defective reference cell, the entire column of memory cells will have erroneous resistance readings. In addition, specialized circuitry is required to write a resistance value into the reference cell, and a sense amplifier circuit for such an arrangement tends to be complex and large.

Typically, sensing schemes for PCRAM devices also tend to have a unique architecture which is different from that normally employed in typical DRAM circuits. Although PCRAM's differ from DRAM's in that they store binary values in resistive memory elements rather than as charges on capacitors, and although PCRAM's are non-volatile, where the capacitor structures employed in DRAM's are volatile, nevertheless it would be desirable if the read and write circuits for both devices were as similar as possible so that existing DRAM memory device architectures could be easily adapted to read and write PCRAM devices.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a PCRAM memory device and its method of operation which utilizes a read architecture similar to that employed in some DRAM memory devices. A pair of complementary PCRAM memory cells comprising first and second programmable conductor memory elements are employed, each connected to respective access transistors. During a write operation, the first and second memory elements are written with complementary binary values, that is: if the first memory element is written to a high resistance state, then the second memory element is written to a low resistance state; whereas if the first memory element is written to a low resistance state, the second memory element is written to a higher resistance state.

During a read operation of, for example, the first memory element, a sense amplifier is connected so that its respective inputs are coupled to receive respective precharge voltages which discharge through the first and second memory elements. A sense amplifier reads the discharging voltages through the two memory elements to determine which is the larger voltage, thus determining the resistance (high or low) and logic state (high or low) of the memory cell being read.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the invention will become more apparent from the following detailed description of exemplary embodiments of the invention which are provided in connection with the accompanying drawings in which:

FIG. **1** shows an exemplary PCRAM device;

FIG. **2** is a schematic diagram depicting one aspect of the invention;

FIG. **3** is a schematic diagram depicting an additional aspect of the invention;

FIG. **4** is a schematic diagram depicting an additional aspect of the invention;

FIG. **5** shows the discharge rate characteristics of capacitors employed in the invention;

FIG. **6** shows the invention utilized in a computer system.

DETAILED DESCRIPTION OF THE INVENTION

The present invention employs a sense amplifier architecture which is somewhat similar to that employed in some conventional DRAM devices to sense the resistance states of PCRAM memory cells. In the invention, a binary value is stored as a resistance value in a first PCRAM cell while its complement resistance value is stored in a second PCRAM cell. During readout of the first PCRAM cell, both PCRAM cells are used to discharge a precharge voltage into respective inputs of a sense amplifier which reads the discharge voltages to determine the resistance and thus the binary value stored in the first PCRAM cell undergoing a read operation.

FIG. **1** illustrates an exemplary cell arrangement provided within a portion of a PCRAM memory device constructed in accordance with the invention. A PCRAM memory element **102** is illustrated which has a chalcogenite glass body and lower **103** and upper **104** conductors. As is well known, a programmable conductor memory element has two stable resistance states: one high resistance and one low resistance. Normally, when at rest the memory has a high resistance state, but it can be programmed to a low resistance state by suitably applying bias voltages to the conductors **103** and **104**. Typically, the low resistant state of a PCRAM memory element is characterized by a dendrite growth through the chalcogenite glass body or along the surface of the chalcogenite glass body between the conductors **103** and **104**. A high resistant state is present when there is no such dendrite growth. The grown dendrite is relatively non-volatile in that it will remain in place for a relatively long time, e.g. days or weeks, after the bias voltage is removed.

As further shown in FIG. **1**, the PCRAM memory element **102** is coupled by a conductive plug **101** to an access transistor **207** which is driven by a word line **105** which forms the gate structure of transistor **207**. The access transistor is coupled through conductive plug **101** to one of the conductors **103** of the PCRAM memory element. The other conductor **104** of the PCRAM element is connected by a common cell plate **109** to a bias voltage, which is common to other PCRAM memory elements provided in the memory device.

FIG. **1** illustrates a common PCRAM architecture in which two adjacent memory cells **207**, **211** are coupled to a common digit line **118**. Thus, FIG. **1** also shows another access transistor **211** driven by a word line **107** which is connected through conductive plug **99** to another PCRAM memory element **106**, which in turn is also connected also to the common cell plate **109**. Access transistor **211** also has one terminal connected to digit line **118**.

FIG. **2** shows an electrical schematic arrangement of a memory array employing the cell architecture illustrated in FIG. **1**. Thus, the top portion of FIG. **2** illustrates the transistors **207** and **211** coupled to the respective PCRAM memory elements **102** and **106** with the access transistors **207** and **211** coupling the memory elements **102** and **106** to the digit line **118**.

As also illustrated in FIG. **2**, a complementary digit line D**1*** **120** is also provided in the memory array, to which another set of access transistors is connected which are in turn connected to other PCRAM memory elements. To simplify discussion, a single complementary pair of PCRAM cells is illustrated as **300**. It includes transistor **207** and associated PCRAM memory element **102**, which is coupled to the digit line **118** (D1), and an access transistor **209** and associated PCRAM memory element **124**, which are coupled to digit line **120** (D1*).

During a write operation, a row line **104**, which is coupled to transistor **207** and a row line **113** which is coupled to transistor **209** are activated such that if PCRAM memory element **102** is written to a high resistance state, PCRAM element **124** is written to a low resistance state, and vice versa. In this way, PCRAM memory elements **102** and **124** are accessed together and always store complementary resistance digit values. Thus assuming that PCRAM memory element **102** is the primary element which is being written to and read from, a sense amplifier **210** which is coupled to the digit lines **118** and **120** will read the value of PCRAM memory element **102** by comparing a discharging precharge voltage on digit line **118** to the discharging precharge voltage on digit line **120** during a memory read operation.

Thus, prior to a memory read, a precharge voltage is applied to complementary digit lines **118** and **120** by a precharge circuit **301**. The precharge circuit is activated by a logic circuit on a precharge line which activates transistors **305** to supply a voltage, for example, Vcc/2, to both digit lines **118** and **120**.

During a write operation, a row line **105**, which is coupled to transistor **207** and a row line **113** which is coupled to transistor **209** are activated such that if PCRAM memory element **102** is written to a high resistance state, PCRAM element **124** is written to a low resistance state, and vice versa. In this way, PCRAM memory elements **102** and **124** are accessed together and always store complementary resistance digit values. Thus assuming that PCRAM memory element **102** is the primary element which is being written to and read from, a sense amplifier **210** which is coupled to the digit lines **118** and **120** will read the value of PCRAM memory element **102** by comparing a discharging precharge voltage on digit line **120** during a memory read operation.

Parasitic capacitance for the complementary digit lines **118** and **120** are illustrated as C**1** and C**1***. The respective access transistors **207** and **209** are illustrated as connected to their respective word lines **105** and **113**. The PCRAM memory elements **102** and **124** are also illustrated. As noted, a binary value is stored, for example, in memory PCRAM memory element **102** as a resistance value. It will be either a high resistance value or a low resistance value, and the complementary resistance value will be stored in PCRAM memory element **124**.

During a read operation, the precharge voltage applied to the complementary digit lines **118** and **120** is allowed to discharge through the access transistors **207** and **209** and through the respective resistance values of the PCRAM memory elements **102** and **124**. Because the resistance values will be different, one high and one low, the voltages on the digit lines D**1** and D**1*** (**118**, **120**) will begin to diverge during a read operation. Although the voltage initially applied to the complementary digit lines **118** and **120** is a voltage of Vcc/2, during a read operation this voltage actually is slightly higher by approximately 0.3 mV due to the presence of the parasitic capacitance C**1** and C**1*** on the digit lines **118** and **120**, as well as gate-drain capacitance inherent within transistors **207** and **209**.

FIG. **5** illustrates the voltages on the complementary digit lines **118** and **120** during a read operation. The activation of the word lines **105** and **113** is illustrated as a pulse signal, and initially the voltage of Vcc/2+approximately 0.3 mV which exists on both digit lines D**1** and D**1*** begins to decay. Because one PCRAM memory element, e.g. **102**, has a higher resistance than the other, the voltage on the digit line associated with the lower resistance value, e.g. **124**, will decay faster than the voltage on the digit line coupled to the higher resistance value, e.g. D**1**. This is illustrated in FIG. **5**.

The divergence of the two voltages on the lines D**1** and D**1*** progressively increases. At a predetermined time after the word lines **105** and **113** are activated, the sense amplifier **210** is activated. The sense amplifier can have an architecture typically employed in a DRAM arrangement which is illustrated in FIG. **4**. Such a sense amplifier includes an Nsense amplifier latch **302** and a Psense amplifier latch **304**. This structure is illustrated in FIG. **4**.

Reverting back to FIG. **5**, the N sense amplifier is fired first at a time t_1. When the Nsense amplifier fires, the digit line which has the lower voltage, e.g. D**1*** in the example, is immediately pulled to ground. Thereafter, the Psense amplifier is fired at a time t_2 which drives the higher voltage line, e.g. D**1**, to Vcc. Accordingly at a time t_2, the sense amplifier **210** outputs a value of Vcc indicating the high resistant state for the PCRAM memory element **102**.

Although FIG. **5** illustrates the signal timing which occurs when PCRAM memory element **102** has a higher resistance than memory element **104**, obviously the signal levels are reversed if PCRAM memory element **102** has a low resistance state and PCRAM memory element **124** has a high resistance state. That is, the signal diagrams illustrated in the FIG. **5** would have the digit line D**1*** going towards Vcc and the digit line D**1** going towards ground.

FIG. **5** also illustrates another aspect of the invention. As shown, the voltage for row lines **105**, **113** increases from near ground level to a positive voltage near Vcc for a read operation. This voltage then returns to near ground level before the sense amplifier is enabled (before t_1). As a result, there is no rewriting of a read PCRAM memory element. If such rewriting of a PCRAM cell is desired, then the voltage on row line **105**, **113** having a memory element which is written to a low resistance state, may be at a voltage level near Vcc during operation of the sense amplifier **210**, which will automatically rewrite (refresh) the read cell to the low resistance state.

Because programmable contact memory elements are resistive rather than capacitive memory elements, it is possible they will take longer to pull the digit lines up to Vcc and to ground than a typical capacitive memory element found within a DRAM. Supposing that to be true, older DRAM sense amplifier designs that run somewhat slower than the latest generation of DRAM sense amplifiers could also be used with PCRAM memory cells. The advantage of doing so would be that these older DRAM sense amplifiers have already been shown to perform effectively, and their test infrastructure is already confirmed. Consequently, a hybrid memory consisting of PCRAM memory elements using DRAM sense amplifiers can be produced having the advantages of PCRAM technology, yet being producible quickly and inexpensively.

Although FIG. **2** shows the complementary programmable contact memory element **102** and **106** and associated access transistors and digit lines D and D* as being provided in the same memory array, the complementary memory

elements, access transistors and digit lines may also be provided in respective different memory arrays.

FIG. **6** is a block diagram of a processor-based system **400** utilizing a PCRAM memory device **200** constructed in accordance with one of the embodiments of the present invention. The processor-based system **400** may be a computer system, a process control system or any other system employing a processor and associated memory. The system **400** includes a central processing unit (CPU) **402**, e.g., a microprocessor, that communicates with the PCRAM memory device **408** and an I/O device **404** over a bus **420**. It must be noted that the bus **420** may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus **420** has been illustrated as a single bus. A second I/O device **406** is illustrated, but is not necessary to practice the invention. The processor-based system **400** also includes read-only memory (ROM) **410** and may include peripheral devices such as a floppy disk drive **412** and a compact disk (CD) ROM drive **414** that also communicates with the CPU **402** over the bus **420** as is well known in the art.

One or more memory devices **200** may be provided on a plug-in memory module **256**, e.g. SIMM, DIMM or other plug-in memory module, for easy connection with or disconnection from the bus **420**. While the invention has been described and illustrated with reference to specific exemplary embodiments, it should be understood that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of operating a programmable resistance memory device comprising:

storing a binary value as respective different higher and lower resistance states in a first and second programmable resistance memory element;

determining a binary value stored in one of said memory elements by discharging respective voltages through said memory elements and comparing the discharging voltages; and

rewriting the binary value stored only in one of the first and second programmable resistance memory elements which is storing a lower resistance state.

2. The method as in claim **1** wherein said discharging comprises:

precharging complementary digit lines, which are respectively switchably coupled to said first and second programmable resistance memory elements, to a common voltage value; and

respectively discharging the common voltage value on each of said complementary digit lines through each of said first and second programmable resistance memory elements.

3. The method as in claim **2** wherein said precharged voltage value on said complementary digit lines is discharged through said respective programmable resistance memory elements by enabling access transistors respectively associated with each of said memory elements.

4. The method as in claim **3** further comprising completing said precharge before enabling said access transistors.

5. The method as in claim **4** further comprising equilibrating said digit lines before enabling said access transistors.

6. The method as in claim **3** wherein said comparison comprises:

determining whether the discharging voltage associated with one memory element is the higher or lower of the two discharging voltages and outputting a first binary value if the discharging voltage associated with the said one memory element is the higher voltage and outputting a second binary value if the discharging voltage associated with said one memory element is the lower voltage.

7. The method as in claim **6** further comprising setting a digit line having a higher discharge voltage to a first predetermined voltage state and setting a digit line having a lower discharging voltage to a second predetermined voltage state.

8. The method as in claim **7** wherein said first predetermined voltage is higher than said second predetermined voltage.

9. The method as in claim **8** wherein said second predetermined voltage is ground voltage.

10. The method as in claim **7** further comprising disabling said access transistors before said digit lines are set to said first and second voltage states.

11. The method as in claim **7** further comprising enabling at least one of said access transistors during a time when said digit lines are set to said first and second voltage states.

12. A method of operating a programmable resistance memory device, the method comprising:

respectively storing complementary binary digit values of a data bit as different resistance values in first and second programmable resistance memory elements associated with a single memory cell; and

reading said data bit stored as a resistance value in one of said memory elements.

13. The method of claim **12** further comprising:

precharging respective digit lines switchably coupled to said first and second programmable resistance memory elements to a common precharge voltage prior to said act of reading.

14. The method of claim **13** further comprising:

discharging said precharge voltage on said digit lines through a respective resistance of said first and second programmable resistance memory elements;

determining whether said one of said memory elements is storing a high or low resistance state; and

outputing a binary value corresponding to the stored resistance state.

15. The method of claim **13**, wherein said act of precharging further comprises:

storing said precharge voltage with a parasitic capacitance associated with said digit lines.

16. The method of claim **13**, further comprising:

equilibrating said precharge voltage on said digit lines.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,242,603 B2
APPLICATION NO. : 11/236562
DATED : July 10, 2007
INVENTOR(S) : Glen Hush et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification, the following error is corrected:

Column 3, line 17, “line 104” should read --line 105--.

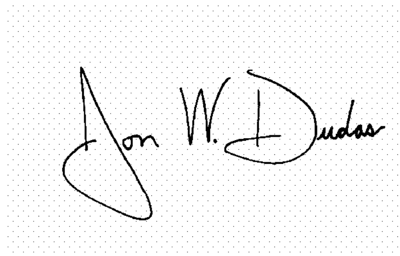
Also in Column 3, the paragraph that begins at line 38 and ends at line 50 is deleted.

The following paragraph is inserted after line 37:

--An equilibrate circuit 303 may also be provided which is activated by an equilibrate signal after the precharge circuit is activated to ensure that the voltages on lines 118 and 120 are the same. The voltages on lines 118 and 120 are held by a parasitic capacitance of the lines. After precharge and equilibrate (if present) circuits are activated, a read operation may be conducted on the complimentary cell pair 300. This read operation is illustrated in greater detail in Figure 3, which is a simplification of the sense amplifier 210 input path.--.

Signed and Sealed this

Thirtieth Day of October, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office