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(54) **COMPLEMENTARY BIT RESISTANCE MEMORY SENSOR AND METHOD OF OPERATION**

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See application file for complete search history.

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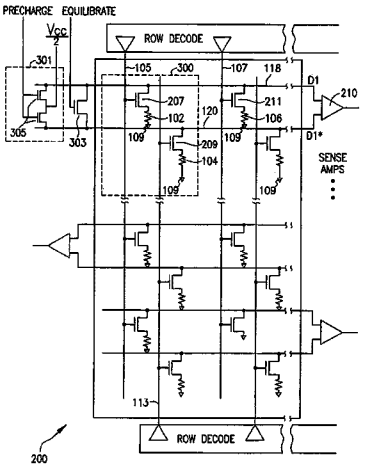
(57) **ABSTRACT**

A method and apparatus are disclosed for sensing the resistance state of a resistance-based memory element using complementary resistance-based elements, one holding the resistance state being sensed and the other holding a complementary resistance state. A sense amplifier detects voltages discharging through the high and low resistance elements to determine the resistance state of an element being read.

32 Claims, 6 Drawing Sheets



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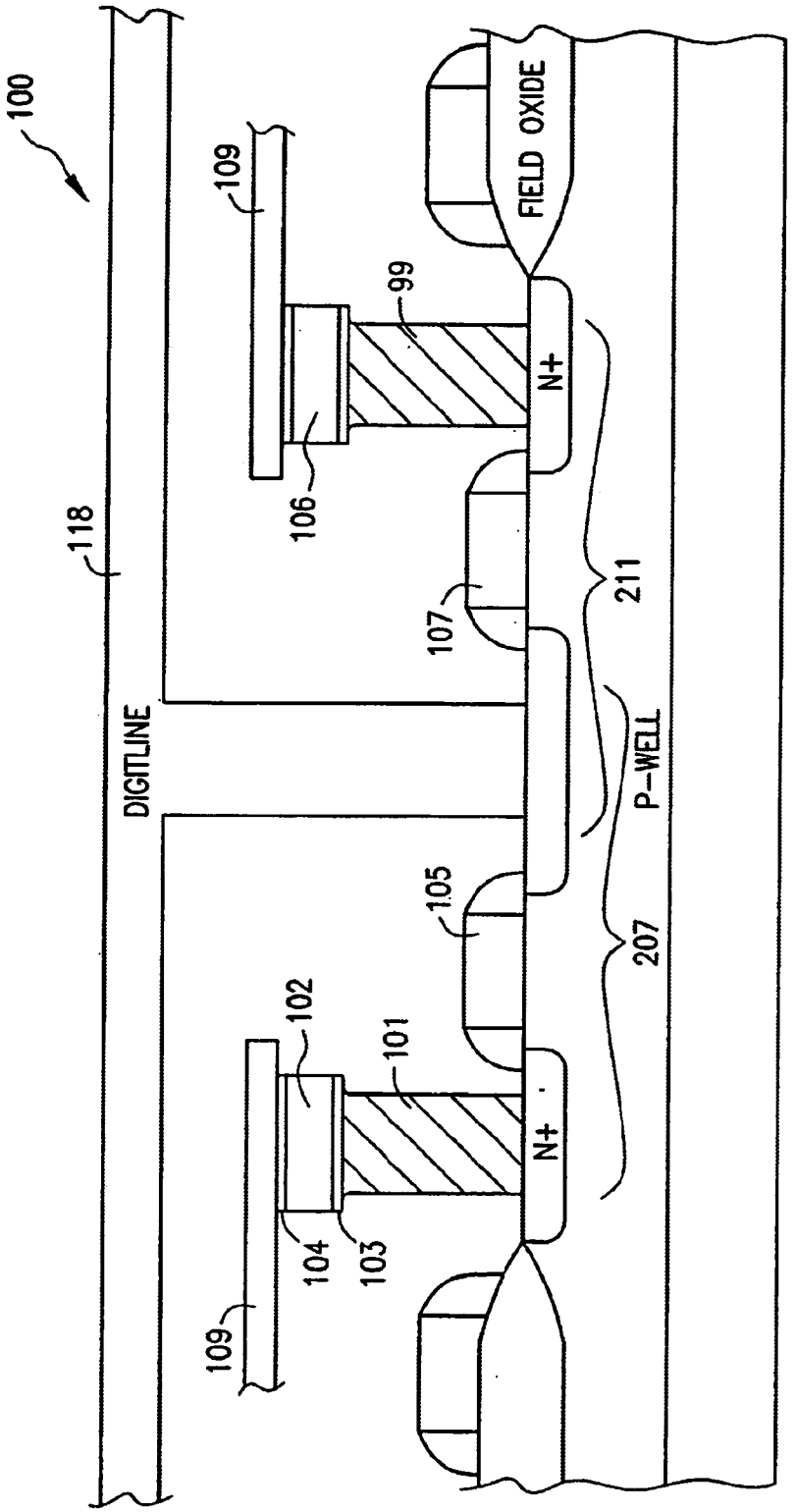
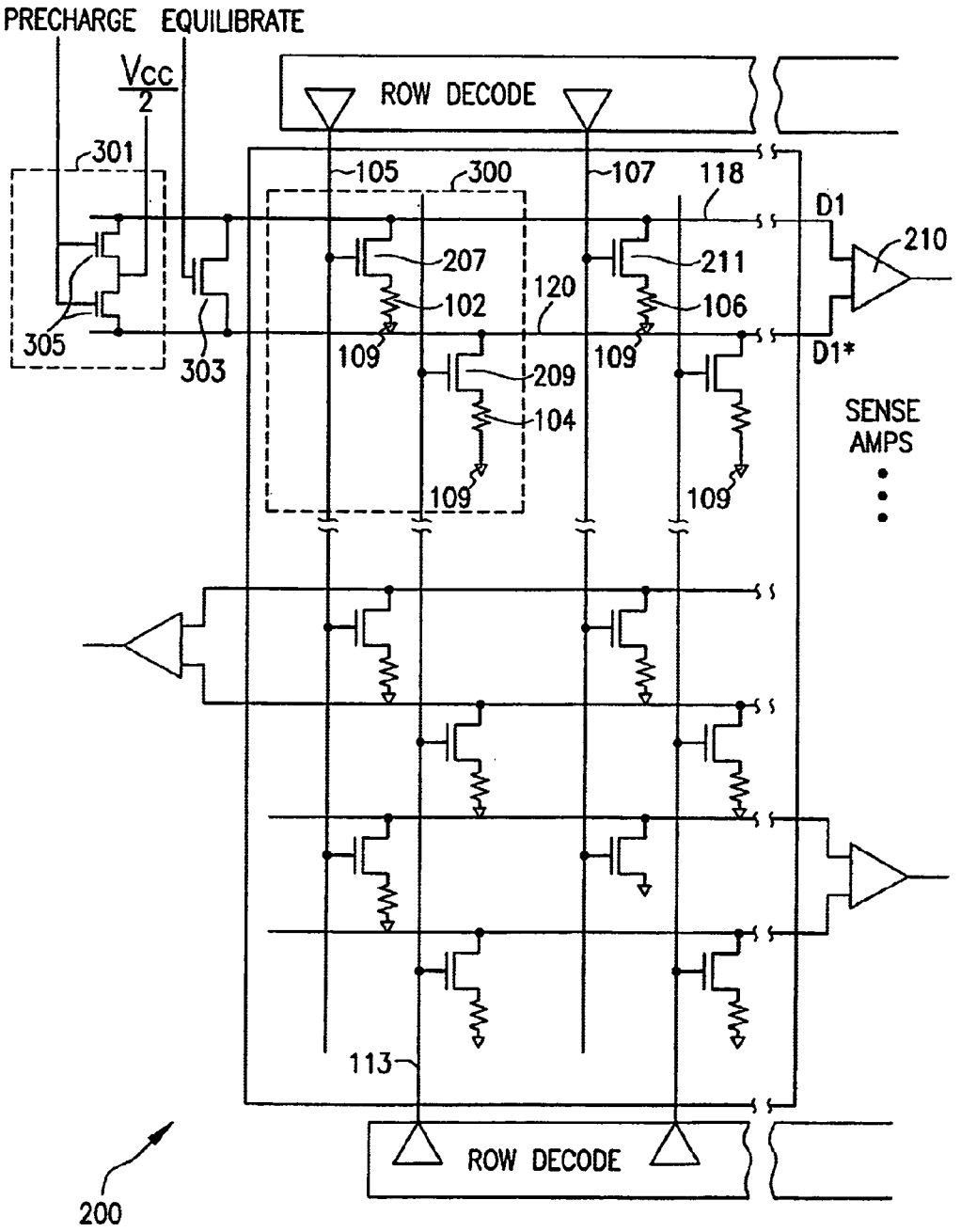

100
109
99
FIELD OXIDE
N+
106
118
107
211
DIGITLINE
P-WELL
105
207
102
101
N+
104
103
109

FIG. 1

FIG. 2


PRECHARGE
EQUILIBRATE
Vcc/2
ROW DECODE
301
105
300
107
118
D1
210
207
211
120
102
106
305
303
109
109
D1*
209
104
SENSE AMPS
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109
113
ROW DECODE
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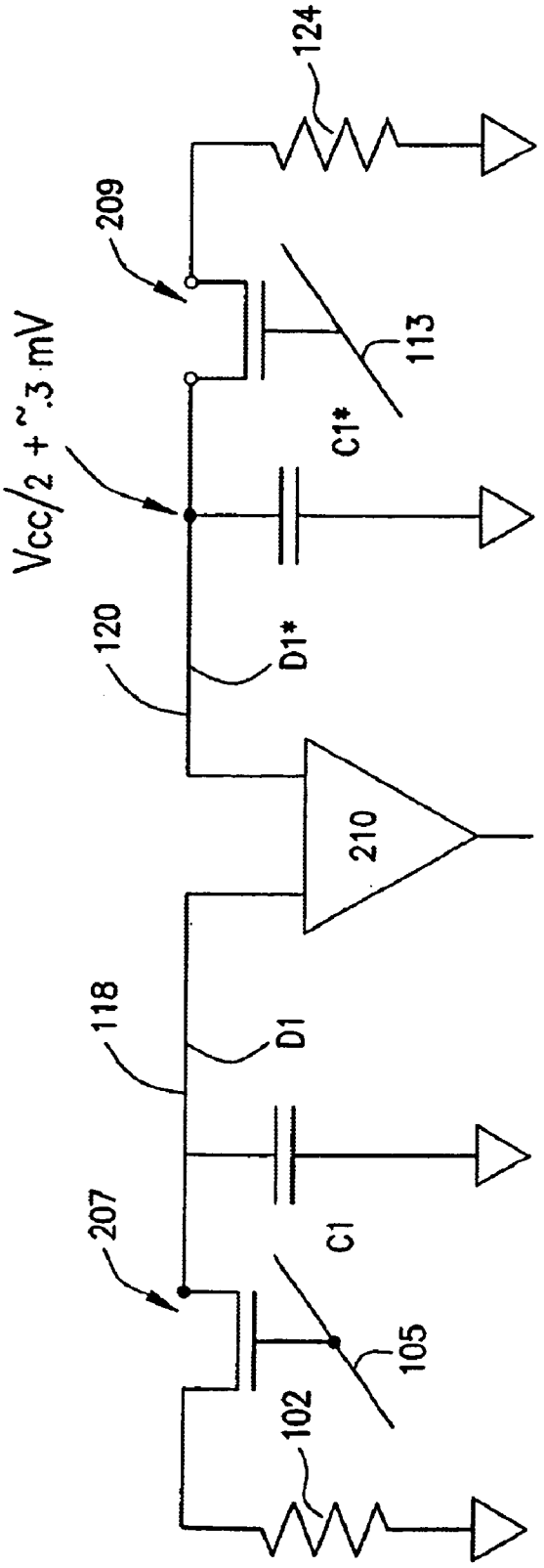


FIG. 3

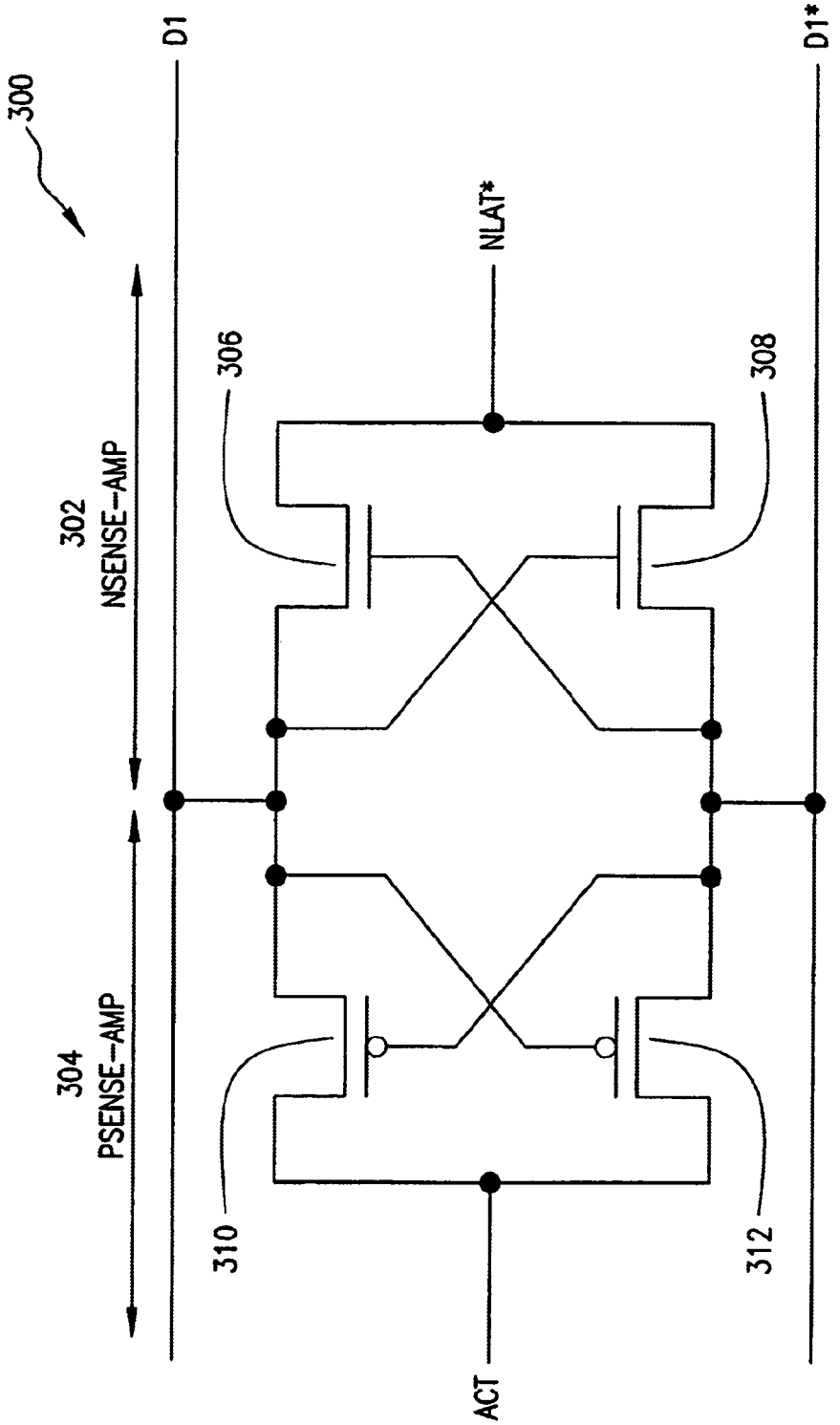

300
D1
D1*
NLAT*
306
308
302
NSENSE-AMP
304
PSENSE-AMP
310
312
ACT

FIG. 4

FIG. 5

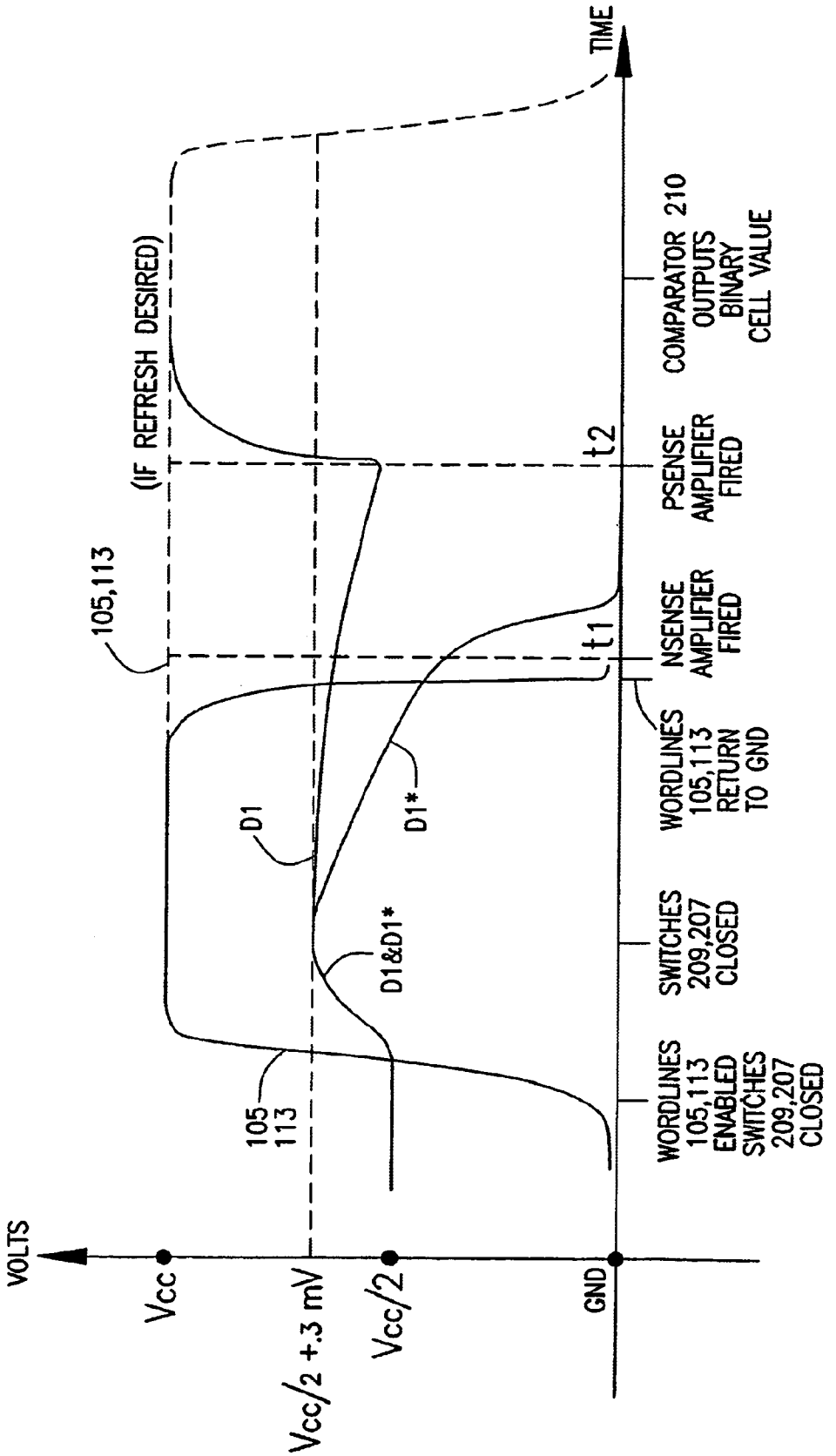
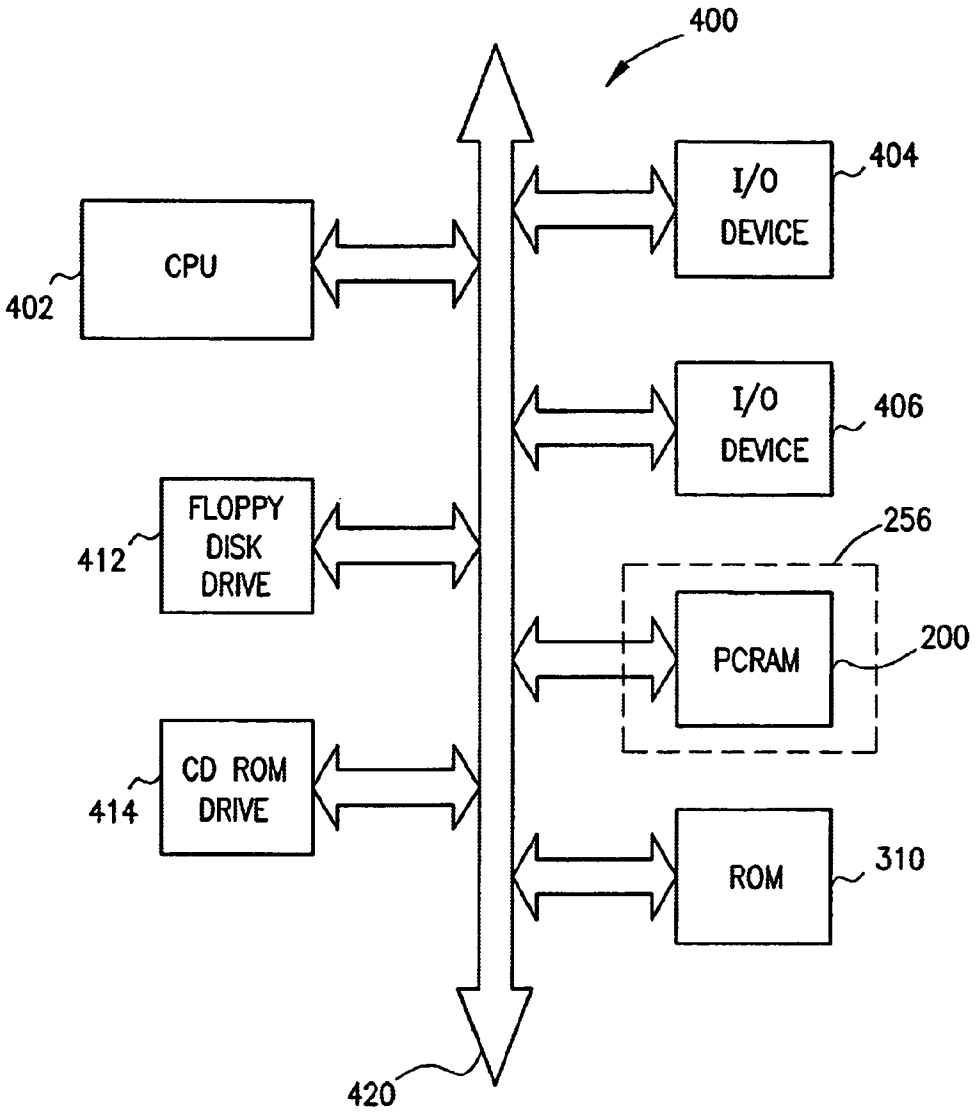

VOLTS
Vcc
Vcc/2 +.3 mV
Vcc/2
GND
105
113
D1
D1*
D1&D1*
105,113
(IF REFRESH DESIRED)
t1
t2
TIME
WORDLINES 105,113 ENABLED SWITCHES 209,207 CLOSED
SWITCHES 209,207 CLOSED
WORDLINES 105,113 RETURN TO GND
NSENSE AMPLIFIER FIRED
PSENSE AMPLIFIER FIRED
COMPARATOR 210 OUTPUTS BINARY CELL VALUE

FIG. 6


400
I/O DEVICE
404
CPU
402
I/O DEVICE
406
FLOPPY DISK DRIVE
412
256
PCRAM
200
CD ROM DRIVE
414
ROM
310
420

COMPLEMENTARY BIT RESISTANCE MEMORY SENSOR AND METHOD OF OPERATION

This application is a continuation of application Ser. No. 09/988,627, filed Nov. 20, 2001 now U.S. Pat. No. 6,791,859, the entire disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

The invention relates to a method and apparatus for sensing the resistance of a Programmable Conductor Random Access Memory (PCRAM) element.

BACKGROUND OF THE INVENTION

PCRAM devices store binary data as two different resistance values, one higher than the other. The resistance value represents a particular binary value of logic "0" or logic "1". When sensing the resistance value of a PCRAM device, it is common to compare the resistance of a memory cell undergoing a read operation with resistance of a reference cell to determine the resistance value of the cell being read and thus its logic state. Such an approach is disclosed in U.S. Pat. No. 5,883,827. However, this approach has some limitations.

If the reference cell is defective and a column of memory cells within an array uses a same defective reference cell, the entire column of memory cells will have erroneous resistance readings. In addition, specialized circuitry is required to write a resistance value into the reference cell, and a sense amplifier circuit for such an arrangement tends to be complex and large.

Typically, sensing schemes for PCRAM devices also tend to have a unique architecture which is different from that normally employed in typical DRAM circuits. Although PCRAM's differ from DRAM's in that they store binary values in resistive memory elements rather than as charges on capacitors, and although PCRAM's are non-volatile, where the capacitor structures employed in DRAM's are volatile, nevertheless it would be desirable if the read and write circuits for both devices were as similar as possible so that existing DRAM memory device architectures could be easily adapted to read and write PCRAM devices.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a PCRAM memory device and its method of operation which utilizes a read architecture similar to that employed in some DRAM memory devices. A pair of complementary PCRAM memory cells comprising first and second programmable conductor memory elements are employed, each connected to respective access transistors. During a write operation, the first and second memory elements are written with complementary binary values, that is: if the first memory element is written to a high resistance state, then the second memory element is written to a low resistance state; whereas if the first memory element is written to a low resistance state, the second memory element is written to a higher resistance state.

During a read operation of, for example, the first memory element, a sense amplifier is connected so that its respective inputs are coupled to receive respective precharge voltages which discharge through the first and second memory elements. A sense amplifier reads the discharging voltages through the two memory elements to determine which is the larger voltage, thus determining the resistance (high or low) and logic state (high or low) of the memory cell being read.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the invention will become more apparent from the following detailed description of exemplary embodiments of the invention which are provided in connection with the accompanying drawings in which:

FIG. **1** shows an exemplary PCRAM device;

FIG. **2** is a schematic diagram depicting one aspect of the invention;

FIG. **3** is a schematic diagram depicting an additional aspect of the invention;

FIG. **4** is a schematic diagram depicting an additional aspect of the invention;

FIG. **5** shows the discharge rate characteristics of capacitors employed in the invention;

FIG. **6** shows the invention utilized in a computer system.

DETAILED DESCRIPTION OF THE INVENTION

The present invention employs a sense amplifier architecture which is somewhat similar to that employed in some conventional DRAM devices to sense the resistance states of PCRAM memory cells. In the invention, a binary value is stored as a resistance value in a first PCRAM cell while its complement resistance value is stored in a second PCRAM cell. During readout of the first PCRAM cell, both PCRAM cells are used to discharge a precharge voltage into respective inputs of a sense amplifier which reads the discharge voltages to determine the resistance and thus the binary value stored in the first PCRAM cell undergoing a read operation.

FIG. **1** illustrates an exemplary cell arrangement provided within a portion of a PCRAM memory device constructed in accordance with the invention. A PCRAM memory element **102** is illustrated which has a chalcogenite glass body and lower **103** and upper **104** conductors. As is well known, a programmable conductor memory element has two stable resistance states: one high resistance and one low resistance. Normally, when at rest the memory has a high resistance state, but it can be programmed to a low resistance state by suitably applying bias voltages to the conductors **103** and **104**. Typically, the low resistant state of a PCRAM memory element is characterized by a dendrite growth through the chalcogenite glass body or along the surface of the chalcogenite glass body between the conductors **103** and **104**. A high resistant state is present when there is no such dendrite growth. The grown dendrite is relatively non-volatile in that it will remain in place for a relatively long time, e.g. days or weeks, after the bias voltage is removed.

As further shown in FIG. **1**, the PCRAM memory element **102** is coupled by a conductive plug **101** to an access transistor **207** which is driven by a word line **105** which forms the gate structure of transistor **207**. The access transistor is coupled through conductive plug **101** to one of the conductors **103** of the PCRAM memory element. The other conductor **104** of the PCRAM element is connected by a common cell plate **109** to a bias voltage, which is common to other PCRAM memory elements provided in the memory device.

FIG. **1** illustrates a common PCRAM architecture in which two adjacent memory cells **207**, **211** are coupled to a common digit line **118**. Thus,. FIG. **1** also shows another

access transistor **211** driven by a word line **107** which is connected through conductive plug **99** to another PCRAM memory element **104**, which in turn is also connected also to the common cell plate **109**. Access transistor **211** also has one terminal connected to digit line **118**.

FIG. **2** shows an electrical schematic arrangement of a memory array employing the cell architecture illustrated in FIG. **1**. Thus, the top portion of FIG. **2** illustrates the transistors **207** and **211** coupled to the respective PCRAM memory elements **102** and **106** with the access transistors **207** and **211** coupling the memory elements **102** and **106** to the digit line **118**.

As also illustrated in FIG. **2**, a complementary digit line D1 * **120** is also provided in the memory array, to which another set of access transistors is connected which are in turn connected to other PCRAM memory elements. To simplify discussion, a single complementary pair of PCRAM cells is illustrated as **300**. It includes transistor **207** and associated PCRAM memory element **102**, which is coupled to the digit line **118** (D1), and an access transistor **209** and associated PCRAM memory element **124**, which are coupled to digit line **120** (D1*).

During a write operation, a row line **104**, which is coupled to transistor **207** and a row line **113** which is coupled to transistor **209** are activated such that if PCRAM memory element **102** is written to a high resistance state, PCRAM element **124** is written to a low resistance state, and vice versa. In this way, PCRAM memory elements **102** and **124** are accessed together and always store complementary resistance digit values. Thus assuming that PCRAM memory element **102** is the primary element which is being written to and read from, a sense amplifier **210** which is coupled to the digit lines **118** and **120** will read the value of PCRAM memory element **102** by comparing a discharging precharge voltage on digit line **118** to the discharging precharge voltage on digit line **120** during a memory read operation.

Thus, prior to a memory read, a precharge voltage is applied to complementary digit lines **118** and **120** by a precharge circuit **301**. The precharge circuit is activated by a logic circuit on a precharge line which activates transistors **305** to supply a voltage, for example, Vcc/2, to both digit lines **118** and **120**.

An equilibrate circuit **303** may also be provided which is activated by an equilibrate signal after the precharge circuit is activated to ensure that the voltages on lines **118** and **120** are the same. The voltages on lines **118** and **120** are held by a parasitic capacitance of the lines. After precharge and equilibrate (if present) circuits are activated, a read operation may be conducted on the complimentary cell pair **300**. This read operation is illustrated in greater detail in FIG. **3**, which is a simplification of the sense amplifier **210** input path.

Parasitic capacitance for the complementary digit lines **118** and **120** are illustrated as C1 and C1*. The respective access transistors **207** and **209** are illustrated as connected to their respective word lines **105** and **113**. The PCRAM memory elements **102** and **124** are also illustrated. As noted, a binary value is stored, for example, in memory PCRAM memory element **102** as a resistance value. It will be either a high resistance value or a low resistance value, and the complementary resistance value will be stored in PCRAM memory element **124**.

During a read operation, the precharge voltage applied to the complementary digit lines **118** and **120** is allowed to discharge through the access transistors **207** and **209** and through the respective resistance values of the PCRAM memory elements **102** and **124**. Because the resistance values will be different, one high and one low, the voltages on the digit lines D1 and D1* (**118**, **120**) will begin to diverge during a read operation. Although the voltage initially applied to the complementary digit lines **118** and **120** is a voltage of Vcc/2, during a read operation this voltage actually is slightly higher by approximately 0.3 mV due to the presence of the parasitic capacitance C1 and C1* on the digit lines **118** and **120**, as well as gate-drain capacitance inherent within transistors **207** and **209**.

FIG. **5** illustrates the voltages on the complementary digit lines **118** and **120** during a read operation. The activation of the word lines **105** and **113** is illustrated as a pulse signal, and initially the voltage of Vcc/2+ approximately 0.3 mV which exists on both digit lines D1 and D1* begins to decay. Because one PCRAM memory element, e.g. **102**, has a higher resistance than the other, the voltage on the digit line associated with the lower resistance value, e.g. **124**, will decay faster than the voltage on the digit line coupled to the higher resistance value, e.g. D1. This is illustrated in FIG. **5**.

The divergence of the two voltages on the lines D1 and D1* progressively increases. At a predetermined time after the word lines **105** and **113** are activated, the sense amplifier **210** is activated. The sense amplifier can have an architecture typically employed in a DRAM arrangement which is illustrated in FIG. **4**. Such a sense amplifier includes an Nsense amplifier latch **302** and a Psense amplifier latch **304**. This structure is illustrated in FIG. **4**.

Reverting back to FIG. **5**, the N sense amplifier is fired first at a time t1. When the Nsense amplifier fires, the digit line which has the lower voltage, e.g. D1* in the example, is immediately pulled to ground. Thereafter, the Psense amplifier is fired at a time t_2 which drives the higher voltage line, e.g. D1, to Vcc. Accordingly at a time t_2, the sense amplifier **210** outputs a value of Vcc indicating the high resistant state for the PCRAM memory element **102**.

Although FIG. **5** illustrates the signal timing which occurs when PCRAM memory element **102** has a higher resistance than memory element **104**, obviously the signal levels are reversed if PCRAM memory element **102** has a low resistance state and PCRAM memory element **124** has a high resistance state. That is, the signal diagrams illustrated in the FIG. **5** would have the digit line D1* going towards Vcc and the digit line D1 going towards ground.

FIG. **5** also illustrates another aspect of the invention. As shown, the voltage for row lines **105**, **113** increases from near ground level to a positive voltage near Vcc for a read operation. This voltage then returns to near ground level before the sense amplifier is enabled (before t_1). As a result, there is no rewriting of a read PCRAM memory element. If such rewriting of a PCRAM cell is desired, then the voltage on row line **105**, **113** having a memory element which is written to a low resistance state, may be at a voltage level near Vcc during operation of the sense amplifier **210**, which will automatically rewrite (refresh) the read cell to the low resistance state.

Because programmable contact memory elements are resistive rather than capacitive memory elements, it is possible they will take longer to pull the digit lines up to Vcc and to ground than a typical capacitive memory element found within a DRAM. Supposing that to be true, older DRAM sense amplifier designs that run somewhat slower than the latest generation of DRAM sense amplifiers could also be used with PCRAM memory cells. The advantage of doing so would be that these older DRAM sense amplifiers have already been shown to perform effectively, and their test infrastructure is already confirmed. Consequently, a hybrid memory consisting of PCRAM memory elements

using DRAM sense amplifiers can be produced having the advantages of PCRAM technology, yet being producible quickly and inexpensively.

Although FIG. **2** shows the complementary programmable contact memory element **102** and **106** and associated access transistors and digit lines D and D* as being provided in the same memory array, the complementary memory elements, access transistors and digit lines may also be provided in respective different memory arrays.

FIG. **6** is a block diagram of a processor-based system **400** utilizing a PCRAM memory device **200** constructed in accordance with one of the embodiments of the present invention. The processor-based system **400** may be a computer system, a process control system or any other system employing a processor and associated memory. The system **400** includes a central processing unit (CPU) **402**, e.g., a microprocessor, that communicates with the PCRAM memory device **408** and an I/O device **404** over a bus **420**. It must be noted that the bus **420** may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus **420** has been illustrated as a single bus. A second I/O device **406** is illustrated, but is not necessary to practice the invention. The processor-based system **400** also includes read-only memory (ROM) **410** and may include peripheral devices such as a floppy disk drive **412** and a compact disk (CD) ROM drive **414**, that also communicates with the CPU **402** over the bus **420** as is well known in the art.

One or more memory devices **200** may be provided on a plug-in memory module **256**, e.g. SIMM, DIMM or other plug-in memory module, for easy connection with or disconnection from the bus **420**. While the invention has been described and illustrated with reference to specific exemplary embodiments, it should be understood that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A programmable resistance memory device, comprising:

a first and second digit line;

first and second programmable resistance memory elements associated with a single memory cell for respectively storing complementary binary digit values of a data bit as different resistance values;

first and second access devices for respectively coupling said first and second memory elements to said first and second digit lines; and

a sense amplifier having inputs respectively coupled to said first and second digit lines for reading said data bit stored as a resistance value in one of said memory elements.

2. The device as in claim **1** further comprising a precharge circuit for precharging said digit lines to a common precharge voltage prior to a read operation.

3. The device as in claim **1** further comprising a pair of row lines respectively coupled to said first and second access devices; and

circuitry for simultaneously activating said first and second row lines and therefore activating said first and second access devices.

4. The device as in claim **3** wherein said first and second access devices are access transistors.

5. The device as in claim **3** wherein when said access devices are activated, said precharge voltage on said digit lines discharges through a respective resistance of said first and second resistance-based memory elements, said sense amplifier determining whether said one of said memory elements is storing a high or low resistance state and outputting a binary value corresponding to the stored resistance state.

6. The device as in claim **2** wherein said digit lines have an associated parasitic capacitance which stores said precharge voltage.

7. The device as in claim **2** wherein said parasitic capacitance stores a voltage value which is larger than said precharge voltage.

8. The device as in claim **3** wherein said row lines are activated in a manner which prevents an automatic refresh of at least one of said memory elements during a read operation.

9. The device as in claim **1** wherein said first and second memory elements are in different memory arrays.

10. The device as in claim **2** further comprising an equilibrate circuit for equilibrating the voltage on said digit lines.

11. A memory device comprising:

a plurality of pairs of first and second programmable resistance memory cells, each pair of memory cells comprising:

first and second programmable resistance memory elements associated with a single memory cell for respectively storing complementary binary digit values of a data bit as different resistance values;

first and second access devices for respectively coupling said first and second memory elements to first and second digit lines; and

a sense amplifier having inputs respectively coupled to said first and second digit lines for reading said data bit stored as a resistance value in one of said memory elements.

12. The device as in claim **11** further comprising a precharge circuit for precharging said digit lines to a common precharge voltage prior to a read operation.

13. The device as in claim **11** further comprising a pair of row lines respectively coupled to said first and second access devices; and

circuitry for simultaneously activating said first and second row lines and therefore activating said first and second access devices.

14. The device as in claim **13** wherein said first and second access devices are access transistors.

15. The device as in claim **13** wherein when said access devices are activated, said precharge voltage on said digit lines discharges through a respective resistance of said first and second programmable resistance memory elements, said sense amplifier determining whether said one of said memory elements is storing a high or low resistance state and outputting a binary value corresponding to the stored resistance state.

16. The device as in claim **15** wherein said digit lines have an associated parasitic capacitance which stores said precharge voltage.

17. The device as in claim **15** wherein said parasitic capacitance stores a voltage value which is larger than said precharge voltage.

18. The device as in claim **11** wherein said first and second memory elements are in a common memory array.

19. The device as in claim **11** wherein said first and second memory elements are in different memory arrays.

20. The device as in claim **12** further comprising an equilibrate circuit for equilibrating the precharge voltage on said digit lines.

21. The device as in claim **11** wherein said memory device is provided on a memory module.

22. The device as in claim **21** wherein said memory module is a plug-in memory module.

23. A computer system comprising:

a processor;

a memory system coupled to said processor, said memory system comprising:

a first and second digit line;

first and second programmable resistance memory elements associated with a single memory cell for respectively storing complementary binary digit values of a data bit as different resistance values;

first and second access devices for respectively coupling said first and second programmable resistance memory elements to said first and second digit lines; and

a sense amplifier having inputs respectively coupled to said first and second digit lines for reading said data bit stored as a resistance value in one of said memory elements.

24. The system as in claim **23** further comprising a precharge circuit for precharging said digit lines to a common precharge voltage prior to a read operation.

25. The system as in claim **23** further comprising a pair of row lines respectively coupled to said first and second access devices; and

circuitry for simultaneously activating said first and second row lines and therefore activating said first and second access devices.

26. The system as in claim **25** wherein said first and second access devices are access transistors.

27. The system as in claim **25** wherein when said access devices are activated, said precharge voltage on said digit lines discharges through a respective resistance of said first and second memory elements, said sense amplifier determining whether said one of said memory elements is storing a high or low resistance state and outputting a binary value corresponding to the stored resistance state.

28. The system as in claim **24** wherein said digit lines have an associated parasitic capacitance which stores said precharge voltage.

29. The system as in claim **24** wherein said parasitic capacitance stores a voltage value which is larger than said precharge voltage.

30. The system as in claim **23** wherein said first and second memory elements are in a common memory array.

31. The system as in claim **23** wherein said first and second memory elements are in different memory arrays.

32. The system as in claim **24** further comprising an equilibrate circuit for equilibrating the voltage on said digit lines.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,002,833 B2
APPLICATION NO. : 10/866091
DATED : February 21, 2006
INVENTOR(S) : Glen Hush et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4, line 28, "t1" should read --t_1--.

Item (56), References Cited, Other Publications, the following errors are corrected:

"Boolchand, P., The maximum in glass transition temperature (Tg) near=1/3 ln Ge_xSe_{1-x} Glasses, Asian Journal of Physics (2000) 9, 709-72."

Should read

--Boolchand, P., The maximum in glass transition temperature (Tg) near x=1/3 ln Ge_xSe_{1-x} Glasses, Asian Journal of Physics (2000) 9, 709-72.--;

"Deamaley, G.; Stoneham, A.M.; Morgan, D.V., Electrical phenomena in amorphous oxide films, Rep. Prog. Phys. 33 (1970) 1129-1191."

Should read

--Dearnaley, G.; Stoneham, A.M.; Morgan, D.V., Electrical phenomena in amorphous oxide films, Rep. Prog. Phys. 33 (1970) 1129-1191.--;

"Kotkata, M.F.; Afif, M.A.; Labib, H.H.; Hegab, N.A.; Abdel-Aziz, M.M., Memory switching in amorphous GeSeTi chalcogenide semiconductor films, Thin Solid Films 240 (1994) 143-146."

Should read

--Kotkata, M.F.; Afifi, M.A.; Labib, H.H.; Hegab, N.A.; Abdel-Aziz, M.M., Memory switching in amorphous GeSeTi chalcogenide semiconductor films, Thin Solid Films 240 (1994) 143-146.--;

"McHardy, et al., The dissolution of metals in amorphous chalcogenides and the effects o electron and ultraviolet radiation, 20 J. Phys. C.: Solid State Phys., pp. 4055-4075 (1987)f."

Should read

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"Rose, M.J.; Snell, A.J.; Lecomber, P.G.; Hajto, J.; Fitzgerald, A.G.; Owen, A.E., Aspects of non-volatility in a –Si:H memory devices, Mat. Res. Soc. Symp. Proc. V 258, 1992, 1075-1080."

Should Read

--Rose, M.J.; Snell, A.J.; Lecomber, P.G.; Hajto, J.; Fitzgerald, A.G.; Owen, A.E., Aspects of non-volatility in metal/a –Si:H memory devices, Mat. Res. Soc. Symp. Proc. V 258, 1992, 1075-1080.--;
and

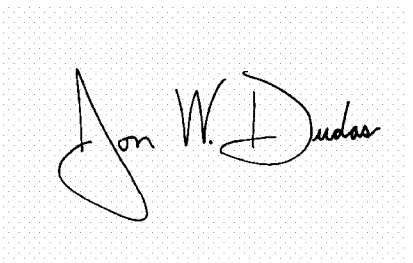
"Tranchant, S.; Peytavin, S.; Ribes, M.; Flank, A.M.; Dexpert, H.; Lagarde, J.P., Silver chalcogenide glasses Ag-Ge-Se: Ionic conduction and exafs structural investigation, Transport-structure relations in fast ion and mixed conductors Proceedings of the 6th Riso International, Symposium. Sep. 9-13, 1985."

Should Read

--Tranchant, S.; Peytavin, S.; Ribes, M.; Flank, A.M.; Dexpert, H.; Lagarde, J.P., Silver chalcogenide glasses Ag-Ge-Se: Ionic conduction and EXAFS structural investigation, Transport-structure relations in fast ion and mixed conductors, Proceedings of the 6th RISO International Symposium. Sep. 9-13, 1985.--.

Signed and Sealed this

Eighth Day of August, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office