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(54) **PHASE SPLITTER USING DIGITAL DELAY LOCKED LOOPS**

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6,011,732 A	1/2000	Harrison et al.	
6,137,325 A	10/2000	Miller, Jr.	
6,289,068 B1 *	9/2001	Hassoun et al.	375/376
6,385,126 B2 *	5/2002	Jung et al.	365/233
6,445,231 B1	9/2002	Baker et al.	
6,539,072 B1 *	3/2003	Donnelly et al.	375/371
6,777,995 B1	8/2004	Harrison	
6,839,860 B2	1/2005	Lin	

* cited by examiner

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(52) **U.S. Cl.** **375/376**

(58) **Field of Search** **375/371-376;**
327/158

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,963,069 A * 10/1999 Jefferson et al. 327/158

Primary Examiner—Stephen Chin

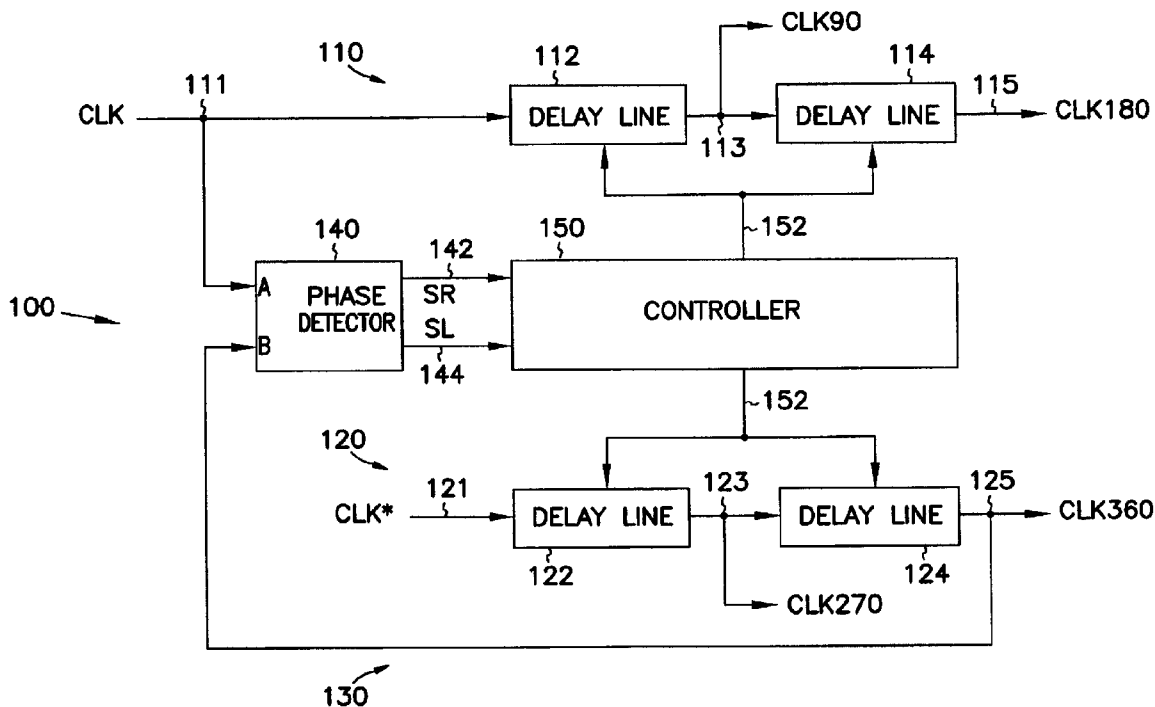
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(57) **ABSTRACT**

A phase splitter using digital delay locked loop (DLL) to receive complementary input clock signals to generate a plurality of output signals having different phase shifts. When the DLL is locked, the delay resolution of the phase splitter is equal to two delay stages of the DLL.

56 Claims, 10 Drawing Sheets



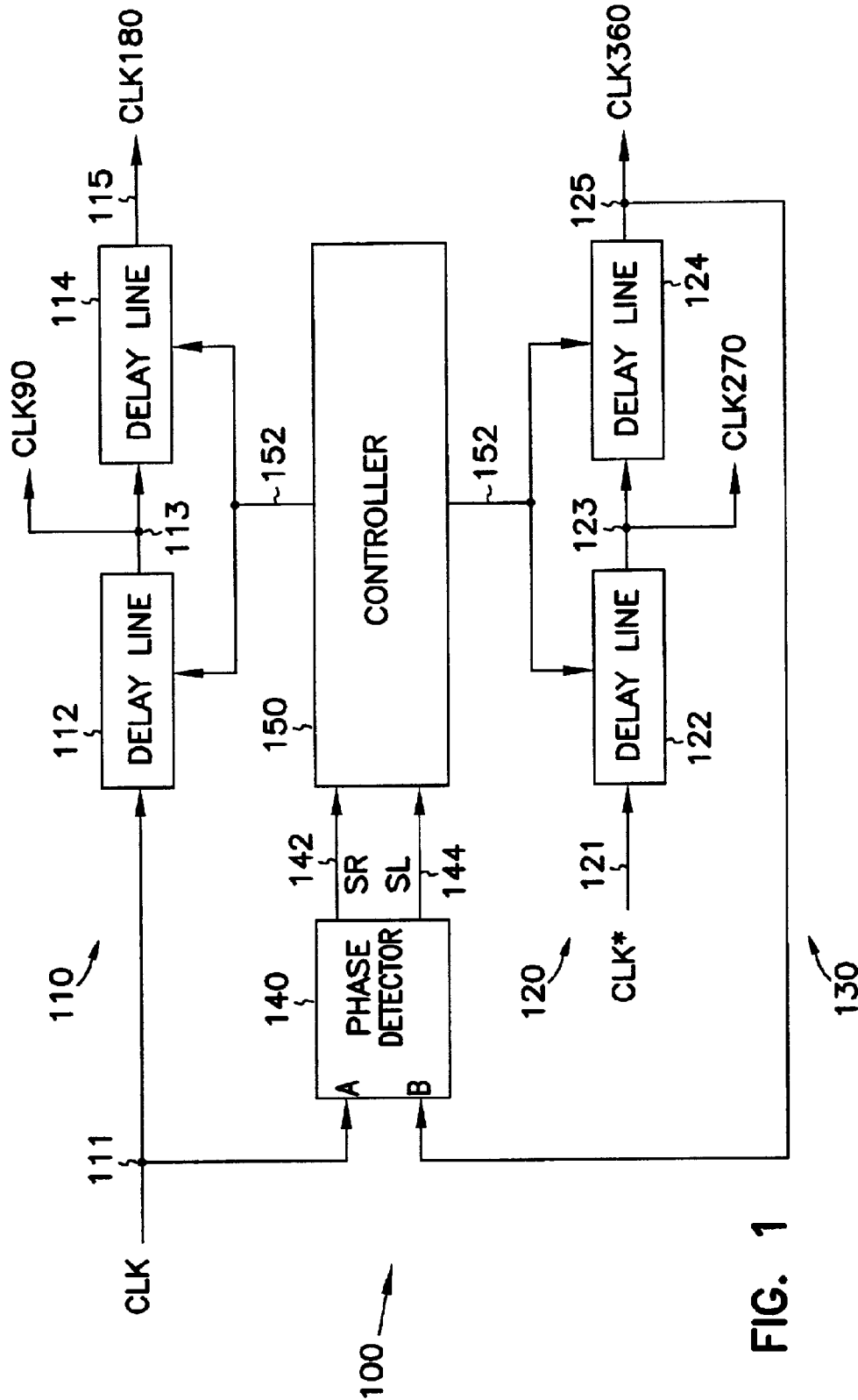


FIG. 1

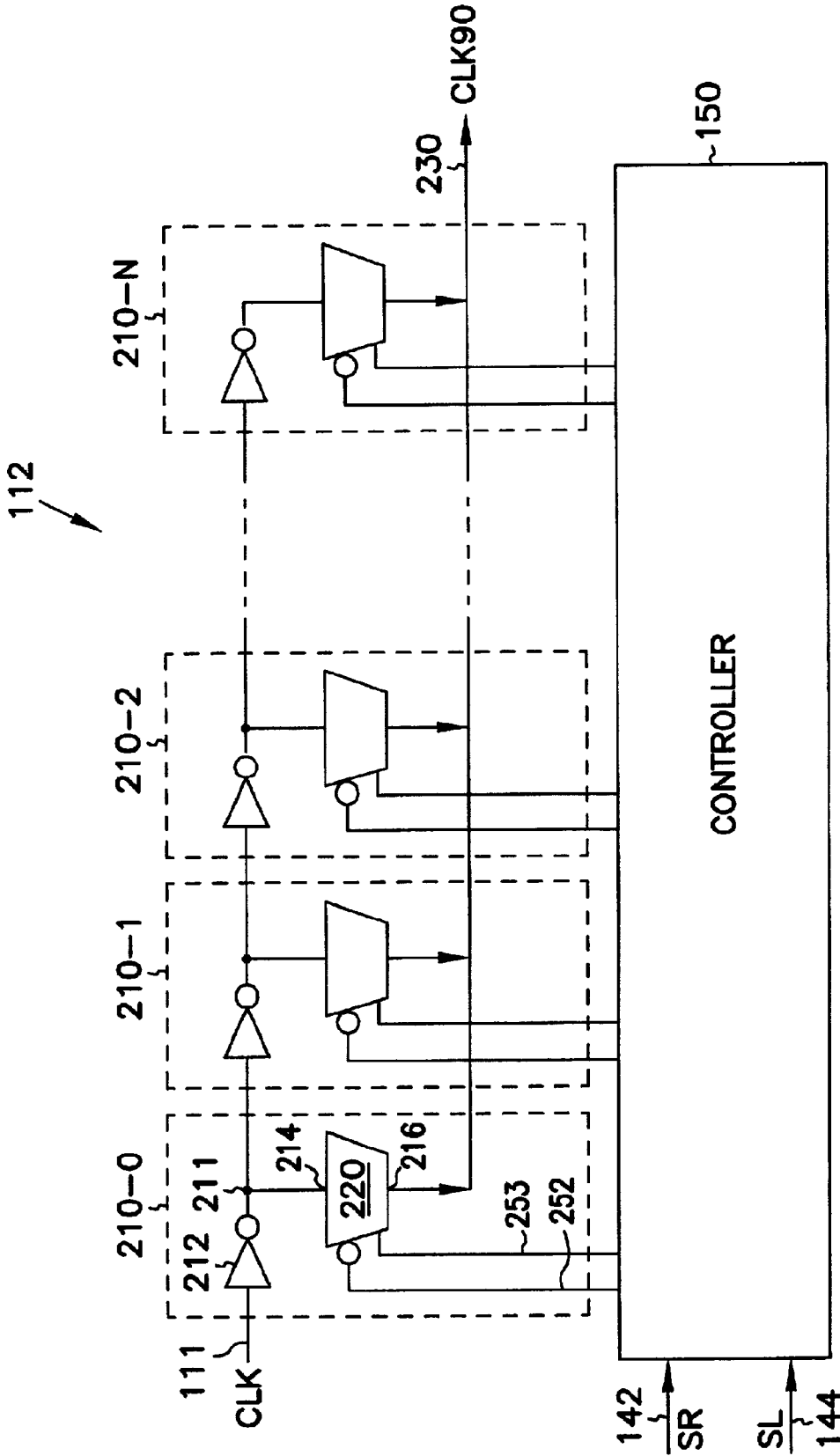


FIG. 2

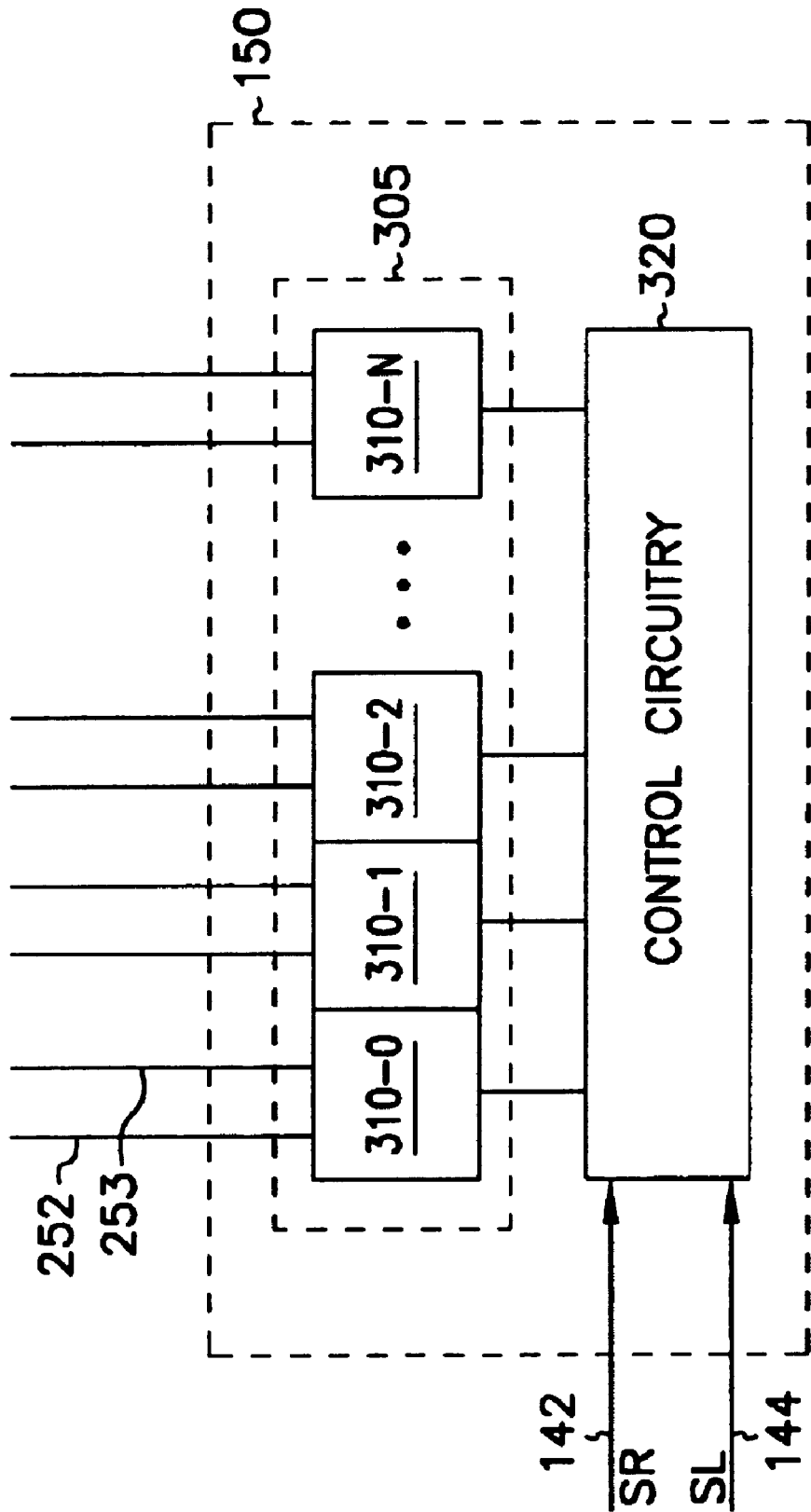


FIG. 3

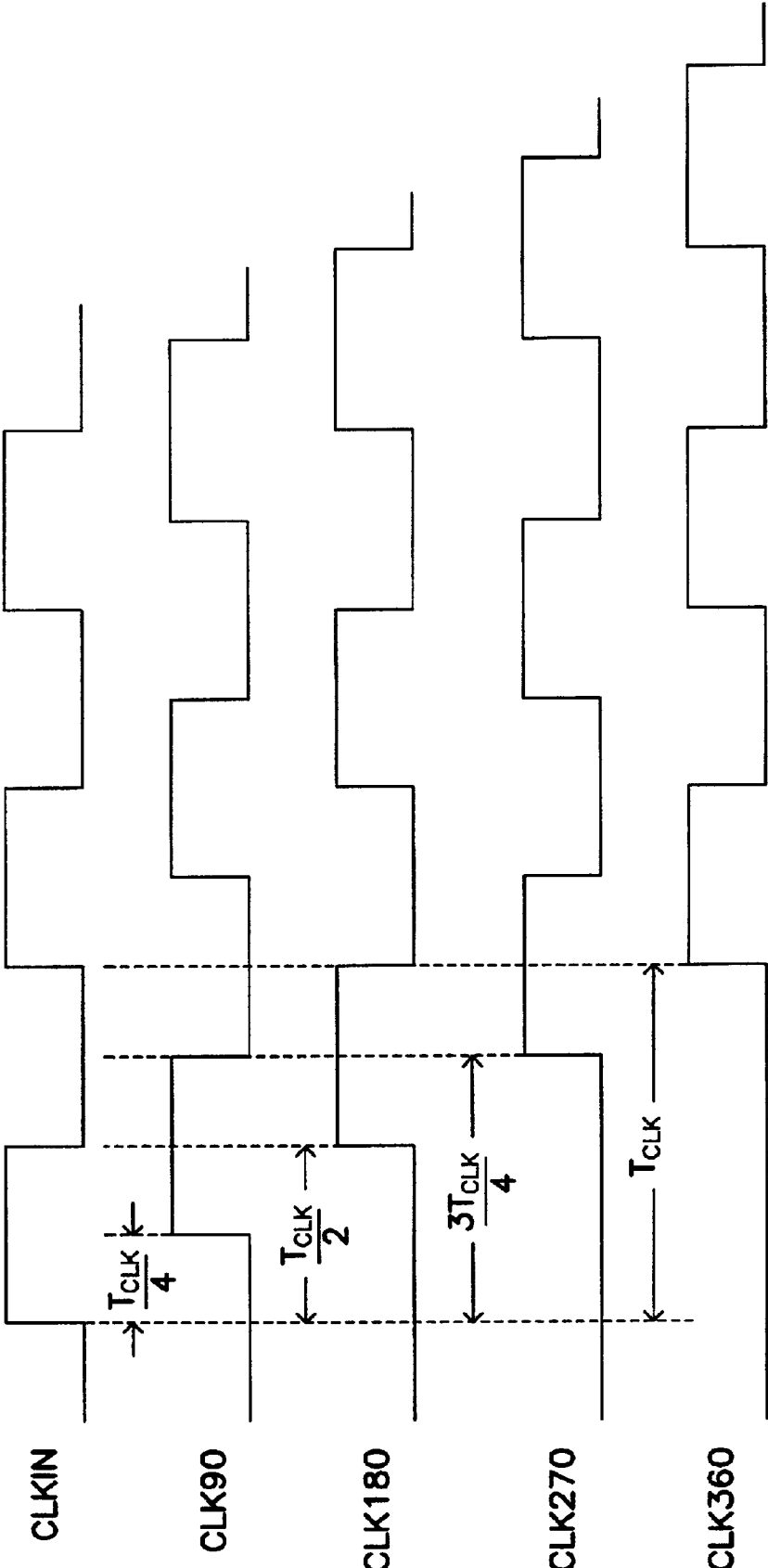


FIG. 4

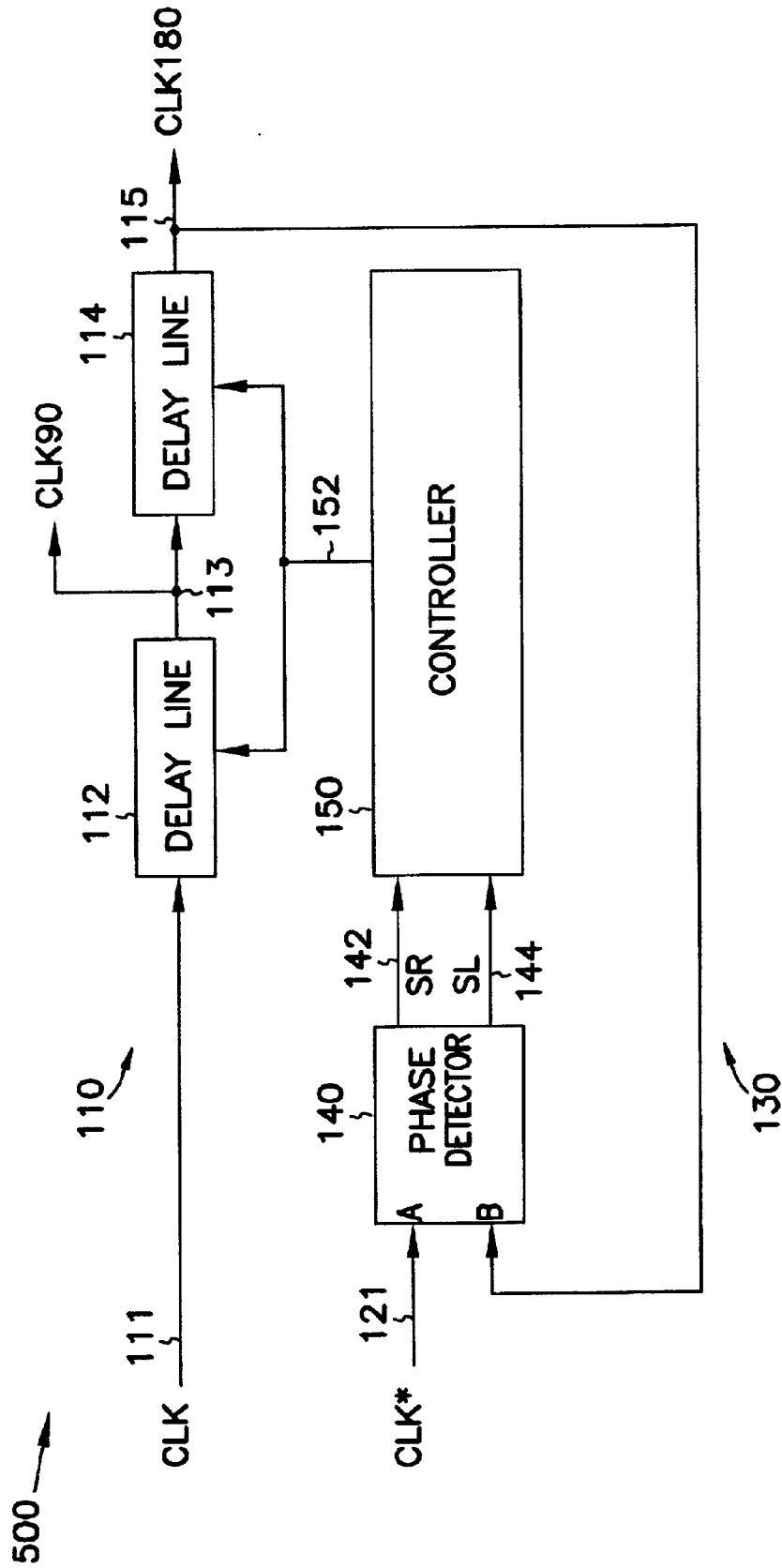


FIG. 5

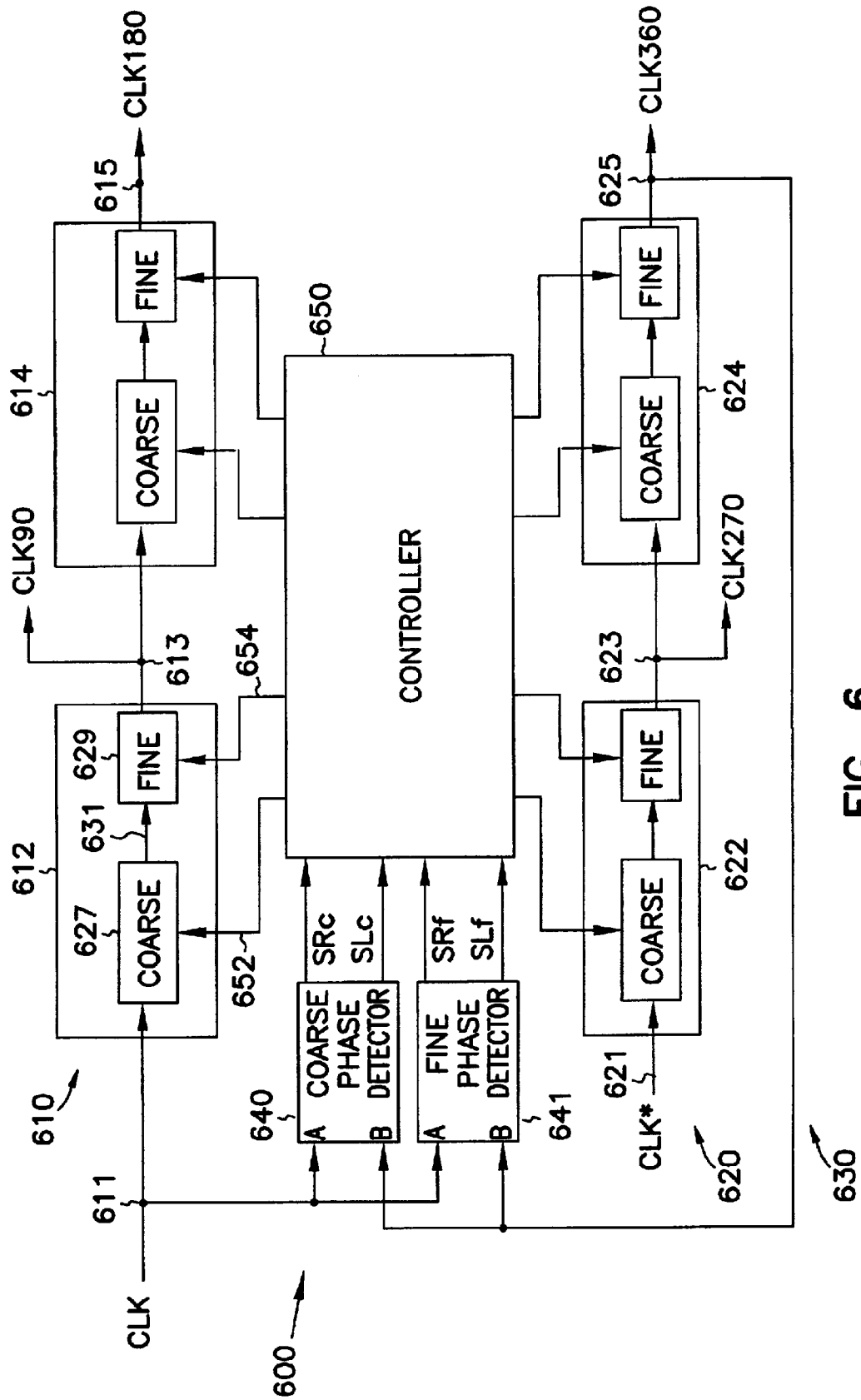


FIG. 6

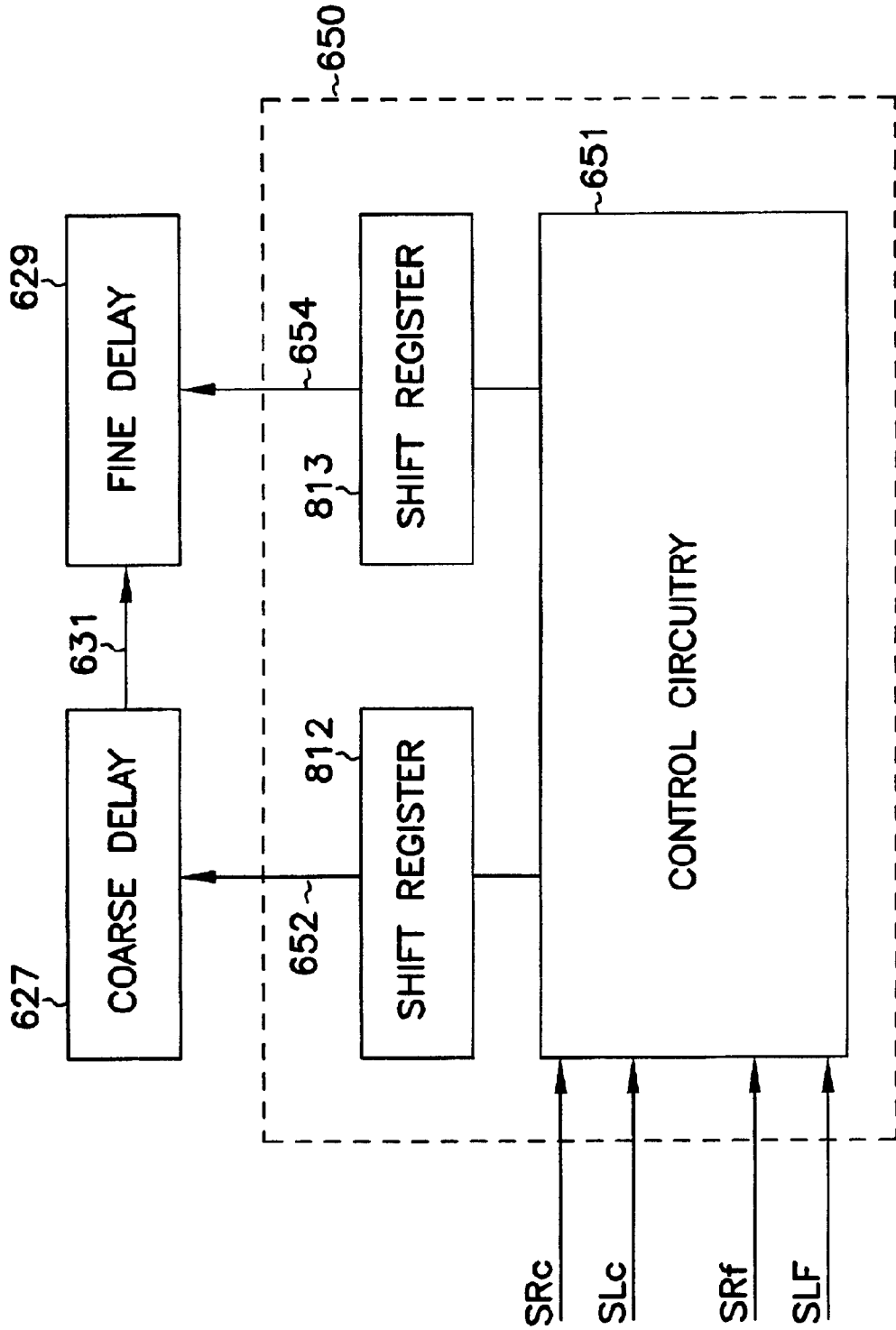


FIG. 7

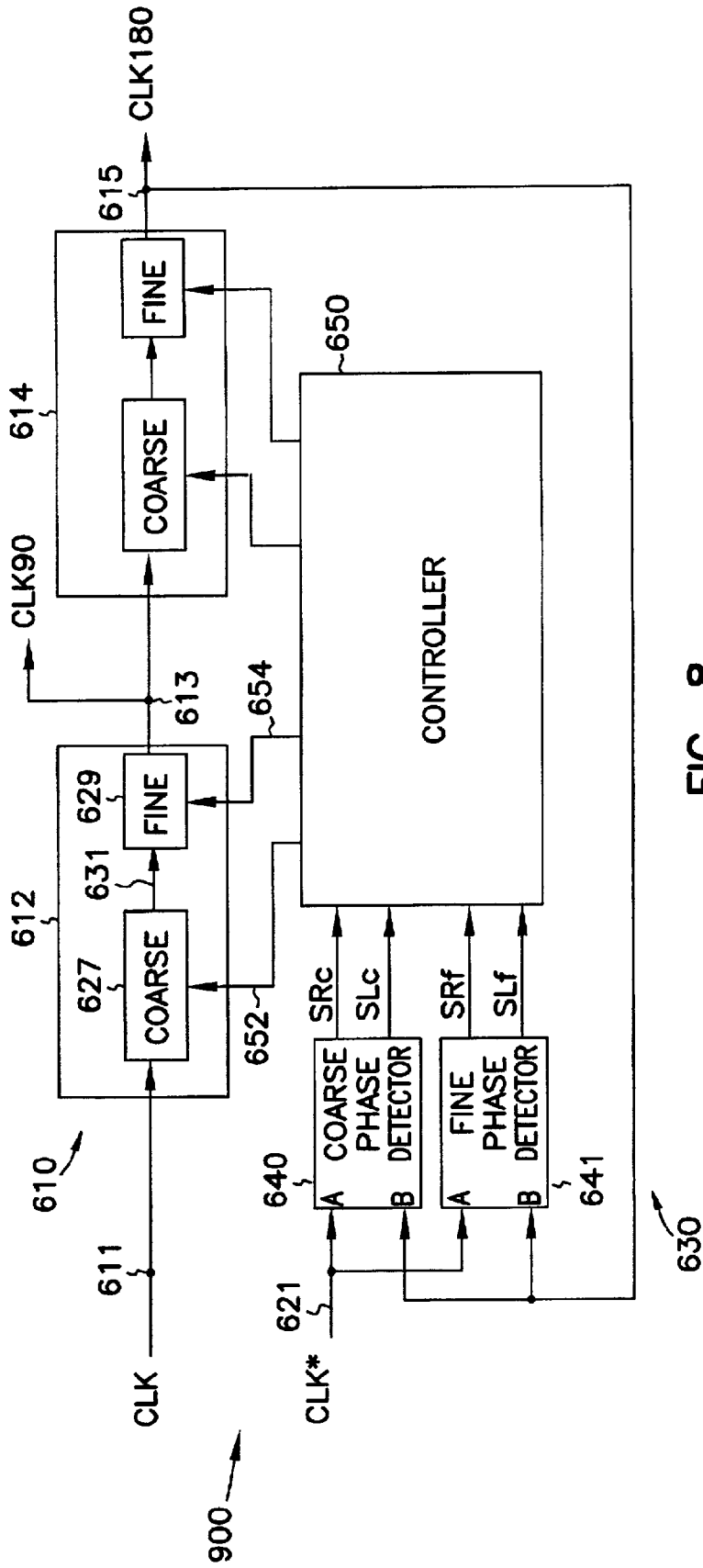


FIG. 8

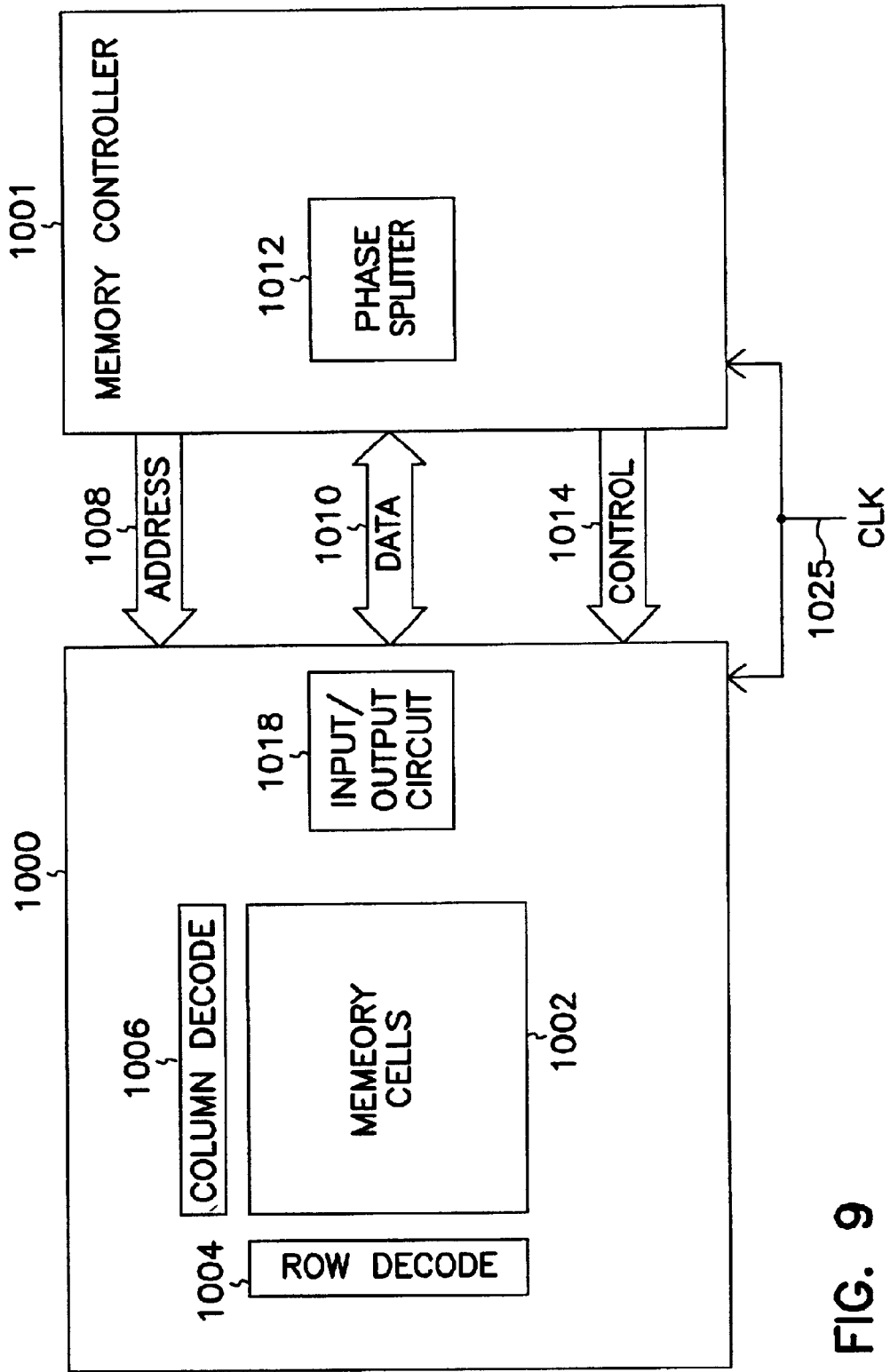


FIG. 9

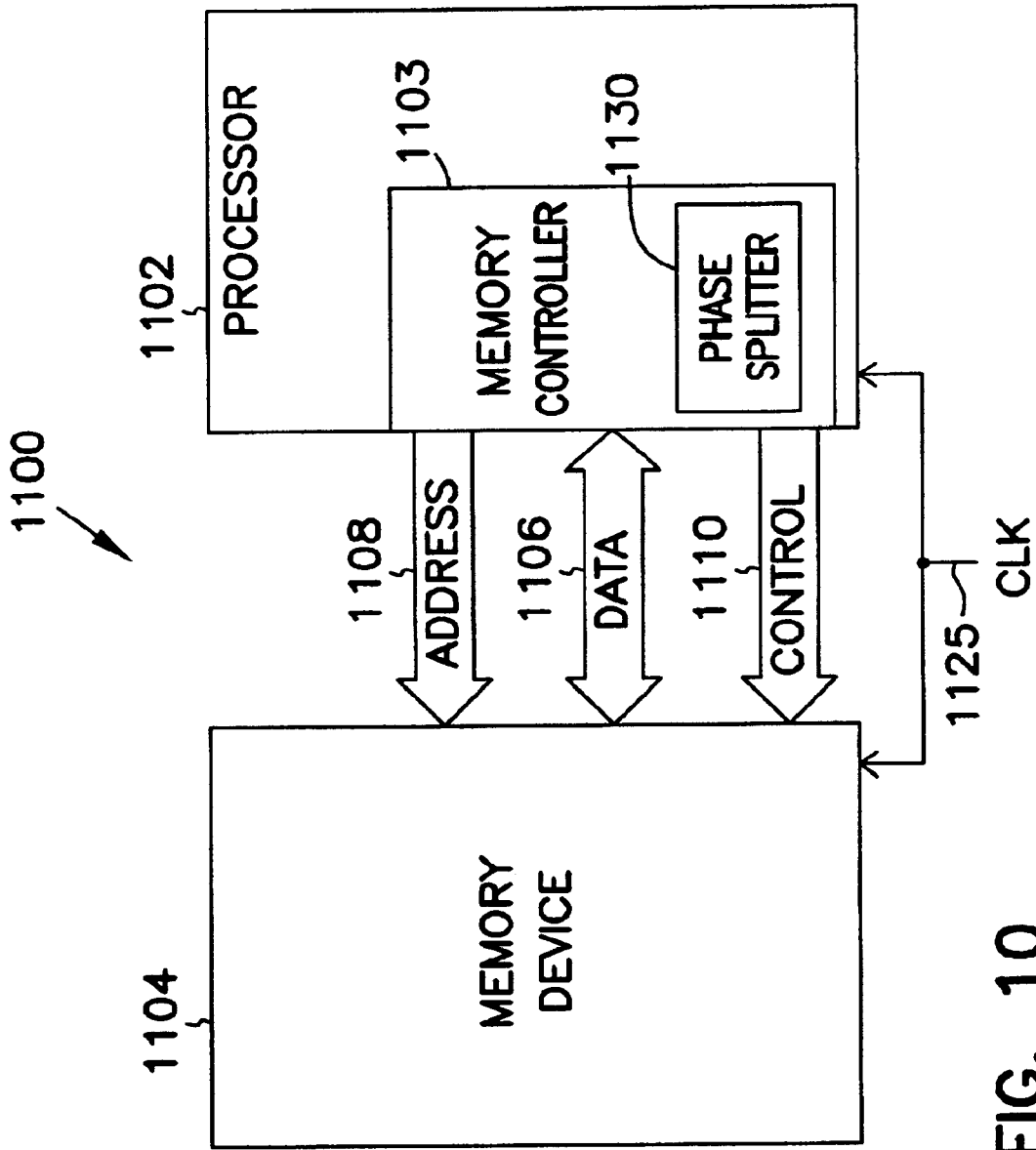


FIG. 10

PHASE SPLITTER USING DIGITAL DELAY LOCKED LOOPS

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to integrated circuits (ICs), and in particular to generating multiple clock signals for an IC.

BACKGROUND OF THE INVENTION

In an integrated circuit, a clock signal having a different phase shift with the system clock signal is sometimes required for a specific function. For instance, in one method of capturing a data signal, a clock signal 90 degrees out of phase with the system clock is needed. This clock signal is normally referred to as a quadrature clock signal.

Conventionally, the quadrature clock signal can be generated by a phase splitter using analog or digital delay locked loop (DLL). A traditional phase splitter using digital DLL has four delay segments connected in series. Each of the delay segments has a plurality of delay stages to provide a quarter of clock cycle delay to an input or system clock signal. Together, the four delay lines generate four output clock signals having 90, 180, 270 and 360 degrees out of phase with the system clock signal.

Since the traditional phase splitter using digital DLL has four delay lines connected in series, each time the DLL performs a signal synchronization to generate the output clock signals, four delay stages are used, one from each delay segment. Each delay stage includes two delay gates to avoid logic inversion. Thus, the delay resolution of the traditional digital phase splitter is equal to eight delay gates. This resolution may not provide a satisfactory level of accuracy for some devices, especially for high speed devices such as new generations of memory devices.

There is a need for improving the delay resolution of digital phase splitters for producing multiple clock signals.

SUMMARY OF THE INVENTION

The present invention includes a phase splitter using digital delay locked loop (DLL) to receive complementary input clock signals to generate a plurality of output signals having different phase shifts. When the DLL is locked, the delay resolution of the phase splitter is equal to two delay gates of the DLL.

In one aspect, the phase splitter includes a first forward path to delay a first input clock signal by an amount of delay to produce first and second output clock signals. A second forward path delays a second input clock signal by the same amount of delay to produce third and fourth output clock signals. A feedback path connects to the second forward path to produce a feedback signal. The phase splitter also includes a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals. A controller is used to adjust the amount of delay of the first and second forward paths such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal.

In another aspect, a method of generating multiple clock signals includes delaying a first clock signal with an amount of delay to generate first and second output clock signals. The same amount of delay is applied to a second clock signal to generate third and fourth output clock signals. A feedback

signal is generated from the fourth output clock signal. The method also includes generating shifting signals based on a difference between the phases of the feedback and first clock signals. Based on the shifting signals, the amount of delay of the first and second forward paths is adjusted such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a phase splitter according to one embodiment of the invention.

FIG. 2 is a schematic diagram of a delay line of the phase splitter of FIG. 1.

FIG. 3 is a block diagram of a controller of the phase splitter of FIG. 1.

FIG. 4 is a timing diagram of output clock signals generated by the phase splitter of FIG. 1.

FIG. 5 is a block diagram of a phase splitter according to another embodiment of the invention.

FIG. 6 is a block diagram of a phase splitter according to another embodiment of the invention.

FIG. 7 is a block diagram of a controller of the phase splitter of FIG. 6.

FIG. 8 is a block diagram of a phase splitter according to another embodiment of the invention.

FIG. 9 is a block diagram of a memory device including the phase splitter according to the invention.

FIG. 10 is a block diagram of a system including the phase splitter according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

The following detailed description refers to the accompanying drawings which form a part hereof, and show by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the invention is defined only by the appended claims.

FIG. 1 is a block diagram of a phase splitter according to one embodiment of the invention. Digital phase splitter **100** includes first and second forward paths **110** and **120**, and a feedback path **130**. Each of the forward paths **110** and **120** includes two delay lines.

Forward path **110** includes a delay line **112** connected to another delay line **114**. Delay line **112** has an output at node **113** to provide a first output clock signal or a quadrature signal CLK90. Delay line **114** has an output at node **115** to provide a second output clock signal CLK180.

Forward path **120** includes a delay line **122** connected to another delay line **124**. Delay line **122** has an output at node **123** to provide a third output clock signal CLK270. Delay line **124** has an output at node **125** to provide a fourth output clock signal CLK360.

Forward paths **110** has an input node **111** to receive an input signal CLK. Forward path **120** has an input node **121** to receive a second input clock signal CLK*. The CLK and

CLK* signals are complementary clock signals. In other terms, each of the clock signals CLK and CLK* is an inverse of the other.

Delay lines **112**, **114**, **122** and **124** have the same initial setting. That is each of the delays lines **112**, **114**, **122** and **124** has the same number of delay stages initially set to provide the same amount of delay. When phase splitter **100** is in a locked position, each of the delay lines **112**, **114**, **122** and **124** provides a quarter (one-fourth) of clock cycle (clock period) delay.

Phase splitter **100** also includes a phase detector **140** and a controller **150**. Controller **150** connects to the first and second forward paths **110** and **120** via a plurality of control lines **152**. Phase detector **140** has an input A connected to node **111** to receive the CLK signal, and an input B connected to node **125** to receive the feedback signal (CLK360). Phase detector **140** connects to controller **150** via lines **142** and **144** to provide shifting signals. The shifting signals include a shift right (SR) provided on line **142** and a shift left (SL) provided on line **144**.

Feedback path **130** connects between the output of delay line **124** at node **125** and input B of phase detector **140**. In the embodiment of FIG. 1, feedback path **130** receives the CLK360 signal and uses it as a feedback signal and passes this feedback signal to input B of phase detector **140**.

FIG. 2 is a schematic diagram of one embodiment a delay line of the phase splitter **100** of FIG. 1. For simplicity, FIG. 2 only shows a schematic diagram of delay line **112**; other delay lines **114**, **122** and **124** have the same construction. Delay line **112** includes a plurality of delay stages **210-0**, **210-1**, **210-2** through **210-N**. Each of the delay stages **210 0-N** includes a delay element **212**. In FIG. 2, delay element **212** is an inverter. In other embodiments, however, delay element **212** can be a NAND gate or other logic gates. The output of inverter **212** of each of the delay stages **210 0-N** connects to the input of the inverter **212** of the adjacent delay stage at node **211** such as is illustrated in delay stage **210-0**. The input of inverter **212** of first delay stage **210-0** connects to node **111** to receive the CLK signal.

Each of the delay stages **210 0-N** also includes a multiplexer (MUX) **220**. MUX **220** has an input at node **214**, an output at node **216**, and select lines **252** and **253**. MUX **220** connects to controller **150** via select lines **252** and **253**. Select lines **252** and **253** are represented in FIG. 1 by line **152**. Input **214** of each MUX **220** connects to node **211** for a respective delay stage at the output of the inverter **212** of the same delay stage. For instance, input **214** of MUX **200** of delay stage **210-0** connects to the output of inverter **212** of the same delay stage **210-0**. The output of each MUX **220** connects to a common output line **230**. Line **230** of FIG. 2 is represented in FIG. 1 as node **113** associated with delay line **112**. Each time, only one Mux of the delay line can be selected to pass the clock signal.

FIG. 3 is a block diagram of controller **150** of phase splitter **100** of FIG. 1. Controller **150** includes a shift register **305** connected to a register control circuitry **320**. Shift register **305** includes a plurality of shift register cells **310-0** to **310-N** (**310 0-N**). Each of the register cells **310 0-N** connects to one MUX **220** via lines **252** and **253** for each delay stage. The number of shift register cells **310 0-N** is equal to the number of delay stages **210 0-N**. Control circuitry **320** connects to lines **142** and **144** shown in FIG. 1, to receive the SR and SL signals.

In general, referring to FIG. 1, phase splitter **100** receives the complementary clock signals CLK and CLK* at forward paths **110** and **120**. Forward path **110** applies an appropriate

amount delay to the CLK signal to generate the CLK90 and CLK180 signals. Similarly, forward path **120** applies the same amount of delay to the CLK* signal to generate the CLK270 and CLK360 signals. In other words, the amount of delay applied to each of the delay lines **112**, **114**, **122** and **124** is the same. During the operation, phase detector **140** compares the feedback and CLK signals. In this case, the feedback signal is the CLK360 signal. Based on the phase relationship between these two signals, phase detector **140** generates either the SR or SL signal. Controller **150** receives the SR or SL signal and performs a shifting operation to adjust the amount of delay applied to the CLK and CLK* signals. When the CLK360 and CLK signals are synchronized, phase detector **140** disables or deactivates the SR and SL signals. Consequently, controller **150** stops performing the shifting operation. At this point phase splitter **100** is in a locked position.

When phase splitter **100** is locked (when the CLK360 and CLK signals are synchronized) the quadrature clock signal or the CLK90 output clock signal is one-fourth clock cycle delayed from the CLK signal; and each of the other output clock signals CLK180, CLK270 and CLK360 is a multiple of one-fourth clock cycle delayed from the CLK signal. In other words, when the CLK360 and CLK signals are synchronized, the CLK90, CLK180, CLK270 and CLK360 are 90, 180, 270 and 360 degrees out of phase with the CLK signal.

The operation of phase splitter **100** of FIG. 1 is further understood with the description of the operation of delay line **112** of FIG. 2. The operations of other delay lines **114**, **122** and **124** are the same as the operation of delay line **112**. In FIG. 2, delay line **112** receives the CLK signal at nodes **111**. The CLK signal propagates following a path starting from node **111** through a certain number of delay stages **210 0-N** and through one of the MUXs **220** before arriving at output node **230**. Since each of the delay stages **210 0-N** has one inverter **212**, the amount of delay applied to the CLK signal depends on the number, e.g., how many of the inverters **221** it has propagated through.

At the start of the operation, delay line **112** applied an initial amount of delay to the CLK signal by using an initial or a predetermined number of delay stages **210 0-N**. The predetermined number of delay stages is initially set by controller **150**. In subsequent actions of the operation, controller **150** selects a different number of delay stages to adjust, e.g., increase or decrease the amount of delay by increasing or decreasing the number of delay stages. Thus, the amount of delay is proportional to the number of the selected delay stages through which the CLK signal passes. In other terms, when the number of delay stages increases, the amount of delay applied to the CLK signal is increased. Conversely, when the number of delay stages decreases, the amount of delay is decreased.

To select a different number of delay stages, controller **150** selects a different MUX **220** by activating select lines **252** and **253** of the selected MUX. Based on the SR or SL signal provided by phase detector **140** on lines **142** and **144**, controller **150** performs a shifting operation to select a MUX to the right or left of the current MUX. Thus, only one MUX **220** is selected and is activated to pass the CLK signal from node **111** to node **230**.

As an example, in FIG. 2, assuming that MUX **220** of delay stage **210-1** is selected. This selected MUX can be an initial selected MUX at the beginning of the operation or a current selected MUX after at least one shifting operation performed by controller **150**. In this example, the CLK

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signal propagates through two delay stages **210-0** and **210-1**. If controller **150** received the SR (shift right) signal, it will perform a shift right operation to increase the amount of delay by de-selecting MUX **220** of delay stage **210-1** and selecting MUX **220** of delay stage **210-2**. As a result, the CLK signal will propagate through three delay stages **210-0-2**. Back to the initial assumption, if controller **150** received the SL (shift left) signal (instead of the SR signal), it will perform a shift left operation to decrease the amount of delay by de-selecting MUX **220** (initial selected MUX) of delay line **210-1** and selecting MUX **220** of delay stage **210-0**. As a result, the CLK signal will propagate through one delay stage **210-0**.

From the example above, for each shifting operation, the delay applied to the CLK signal is decreased or increased by one delay stage. In the embodiment of FIG. 2 in which each of the delay stages **210-0-N** includes one inverter **212**, the delay of each stage is equal to one inverter delay, which is about 100 picoseconds.

Referring to FIG. 1, delay lines **112**, **114**, **122** and **124** are constructed the same and operate in the same manner as described in FIG. 2. Thus, for each shifting operation, the amount of delay in each delay line varies by one delay stage, which in this embodiment is one inverter delay. However, since delay line **114** or **124** receives input from delay lines **112** or **122**, for each shifting operation, the amount of delay of the input clock signal CLK, CLK* varies by two delay stages or two inverter delays. In other words, for each shifting operation, the total amount of delay is equal to one inverter delay of delay line **124** plus one inverter delay caused by delay line **122**.

Since the CLK360 is provided by the output of delay line **124**, for each shifting operation, the amount of delay applied to the CLK* is varied by two inverter delays. Because the CLK360 is used as a feedback signal by phase detector **140** to provide a clock synchronization, the delay resolution of phase splitter **100** is equal to two inverter delays. In other words, the delay resolution of phase splitter **100** is equal to two delay gates, which is about 200 picoseconds (100 picoseconds for each inverter).

FIG. 4 is a timing diagram of the output clock signals generated by phase splitter **100** of FIG. 1. When phase splitter **100** is in a locked position, that is, when the CLK360 and CLK signals are synchronized, the CLK90 signal is 90 degrees or one-fourth clock cycle delayed from the CLK signal, as indicated by $T_{CLK}/4$. The CLK180 signal is 180 degrees or one-half clock cycle delayed from the CLK signal, as indicated by $T_{CLK}/2$. The CLK270 signal is 270 degrees or three-fourths clock cycle delayed from the CLK signal, as indicated by $3T_{CLK}/4$. The CLK360 signal is 360 degrees or one clock cycle delayed from the CLK signal, as indicated by T_{CLK} .

FIG. 5 is a block diagram of a phase splitter according to another embodiment of the invention. Phase splitter **500** is a variation of phase splitter **100**. For simplicity, similar elements in both phase splitters have the same reference numbers. In the embodiment of FIG. 5, phase splitter **500** includes only two delay lines **112** and **114**. Inputs A and B of phase detector **140** receive the CLK* and CLK180 signals instead of the CLK and CLK360 signals. Feedback path **130** in this variation connects between the output of delay line **114** at node **115** and input B of phase detector **140**. The quadrature clock signal (CLK90) is still provided at node **113**.

Operation of phase splitter **500** is similar to the operation of phase splitter **100**. Phase detector **140** compares the

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CLK180 and CLK* signals to provide a clock synchronization. The delay resolution of phase splitter **500** is still equal to two inverter delays because each of the delay stages still has one inverter.

FIG. 6 is a block diagram of a phase splitter according to another embodiment of the invention. Digital phase splitter **600** is arranged in a similar configuration as phase splitter **100**. Phase splitter **600** includes first and second forward paths **610** and **620**, and a feedback path **630**. Each of the forward paths **610** and **620** includes two delay lines. In this case, each delay line can include a coarse delay segment and a fine delay segment. The fine delay is less than the coarse delay.

Forward path **610** includes a delay line **612** connected to another delay line **614**. Delay line **612** has an output at node **613** to provide a first output clock signal or a quadrature signal CLK90. Delay line **614** has an output at node **615** to provide a second output clock signal CLK180.

Forward path **620** includes a delay line **622** connected to another delay line **624**. Delay line **622** has an output at node **623** to provide a third output clock signal CLK270. Delay line **624** has an output at node **625** to provide a fourth output clock signal CLK360.

Forward path **610** has an input node **611** to receive a first clock signal CLK. Forward path **620** has an input node **621** to receive a second clock signal CLK*. The CLK and CLK* signals are complementary clock signals.

Each of the delay lines **612** and **614** includes a coarse delay segment **627** and a fine delay segment **629**. An output of coarse delay segment **627** connects to an input of fine delay segment **629** at node **631**. Coarse delay segment **627** has the same construction as delay line **112** of phase splitter **100** as shown in FIG. 2. Thus, each delay stage of coarse delay segment **627** also includes one inverter such as inverter **212**. Fine delay segment **629** also includes a plurality of delay stages, where each of the delay stages of fine delay segment provides a smaller amount of delay. Similar to phase splitter **100**, each of the delay lines **612**, **614**, **622** and **624** provides a quarter (one-fourth) of clock cycle delay when phase splitter **600** is locked, which is when the CLK360 and CLK signals are synchronized.

Phase splitter **600** also includes a coarse phase detector **640**, a fine phase detector **641**, and a controller **650**. Controller **650** connects to the first and second forward paths **610** and **620** at coarse delay segment **627** and fine delay segment **629** via a plurality of control lines **652** and **654**.

Coarse phase detector **640** and fine phase detector **641** each has an input A connected to node **611** to receive the CLK signal, and an input B connected to node **625** to receive the CLK360 signal. Coarse phase detector **640** is connected to controller **650** to provide a first set of shifting signals. The shifting signals include a coarse shift right (SRc) and a coarse shift left (SLc). Fine phase detector **641** is connected to controller **650** to provide a second set of command signals or shifting signals. The shifting signals include a fine shift right (SRf) and a fine shift left (SLf).

In comparison to phase splitter **100** of FIG. 1, the interpolation of the coarse and fine delay segments **627** and **629** of phase splitter **600** further improves the delay resolution of the phase splitter. In FIG. 1, the resolution of phase splitter **100** is equal to two delay stages of the delay lines, which is equivalent to two delay stages of the coarse delay segments of phase splitter **600** of FIG. 6. In FIG. 6, however, fine loops further improve the resolution because they have a smaller delay than the delay of the coarse loops.

FIG. 7 shows a block diagram of controller **650** of phase splitter **600** of FIG. 6. Controller **650** includes a control

circuitry **651** connected to a first shift register **812** and second shift register **813**. Shift register **812** is used to control coarse delay segment **627** and shift register **813** is used to control fine delay segment **629**. In one embodiment, shift register **812** includes a plurality of register cells such as those shown as register cells **314 0–N** in FIG. **3** connected to a plurality of delay stages of coarse delay segment similar to the delay stages **210 0–N** shown in FIG. **2**. In one embodiment, shift register **813** includes a plurality of register cells similar to register cells **314 0–N** of FIG. **3**, in which each of the register cells connects to one delay stage of fine delay segment **629**.

The operation of phase splitter **600** includes a coarse delay operation and a fine delay operation. The coarse delay operation is the same as the operation of phase splitter **100**. In this operation, coarse phase detector **640** compares the CLK360 and CLK signal and provides either the SRc or SLc to control circuitry **651**. Control circuitry **651** enables shift register **812** to apply appropriate amount of delay to the CLK and CLK* signals. When the CLK360 and CLK are synchronized, phase detector **640** disables the SRc and SLc signals which causes shift register to stop shifting. At this point, phase splitter **600** provides the four output clock signals CLK90, CLK180, CLK270 and CLK360 with a delay resolution equal to two delay stages of course delay segment **627**. Since coarse delay segment **627** is the same as delay line **112**, the delay resolution of the coarse delay operation is equal to two inverter delay. That is about 200 picoseconds.

The fine delay operation further improves the delay resolution of phase splitter **600** after the coarse delay operation. Following the coarse delay operation, fine delay segment **629** receives the signal from the output of coarse delay segment **627** at node **631**. At this time, phase detector **640** is idling and phase detector **641** activates the SRf or SLf signals. Control circuitry **651** causes shift register **813** to enable fine delay segment **629** to further improve the delay resolution. After the fine delay operation is done, the delay resolution of phase splitter is equal to two delay stages of fine delay segment **629**. That is about 60 picoseconds, when the fine delay per stage is about 30 picoseconds.

FIG. **8** is a block diagram of a phase splitter according to another embodiment of the invention. Digital phase splitter **900** is a hybrid of the phase splitters **600** as shown in FIGS. **5** and **6**. For simplicity, similar elements in both phase splitters have the same reference numbers. In the embodiment of FIG. **8**, phase splitter **900** includes only two delay lines **612** and **614**. Inputs A and B of phase detector **640** and **641** receive the CLK* and CLK180 signal. In this variation, feedback path **630** connects between the output of delay line **614** at node **615** and inputs B of phase detector **640** and **641**. The quadrature clock signal (CLK90) is still provided at node **613**.

Operation of phase splitter **900** is similar to the operation of phase splitter **600**. Coarse phase detector **640** and fine phase detector **641** compare the CLK180 and CLK* signals to provide a clock synchronization. The coarse delay operation provides a delay resolution of two coarse delay stages which is about 200 picoseconds. The fine delay operation improves the delay resolution of phase splitter **900** to two fine delay stages which is about 60 picoseconds.

The embodiments of the phase splitters described above only represent some exemplary configurations of a digital phase splitter according to the invention. In another embodiment, a different configuration of the phase splitter can be used to generate multiple output signals such as the

output signals CLK90, CLK180, CLK270 but using different combination of delay lines. For example, in one embodiment, the phase splitter has a configuration that is similar to phase splitter **100** or **600** but includes only three delay lines, two delay lines in a first forward path and only one delay line in a second forward path.

In yet another embodiment, the phase splitter has similar configuration as phase splitter **500** but generates multiple output signals having phase shift other than 90 degrees. For example, the phase splitter can generate multiple output signals having 60, 120 or 180 degrees out of phase with the external clock signal. In that case, the phase splitter has three delay lines (instead of two) connected in series in one forward path.

Based on the phase splitters shown in FIGS. **1**, **5**, **6** and **8**, and other configurations of the phase splitter can be implemented. Therefore, the phase splitter according to the invention is not limited to those shown in FIGS. **1**, **5**, **6** and **8**, or to the configurations mentioned in the previous two paragraphs. Furthermore, different configurations of the phase splitter may provide different delay resolutions. Therefore, the delay resolution of the phase splitter in other embodiments may not be the same as the delay resolution of the phase splitters described in FIGS. **1**, **5**, **6** and **8**.

FIG. **9** is a block diagram of a memory system **1000** according to one embodiment the invention. Memory system includes a memory device **1000** and a memory controller **1001**. Memory device **1000** includes a plurality of memory cells **1002** generally arranged in rows and columns. Row decode circuit **1004** and column decode circuit **1006** access the rows and columns in response to an address, provided on a plurality of address lines **1008**. Data communication to and from memory device **1000** are transmitted via input/output circuit **1018** in response to command signals on control lines **1014**. Both memory device **1000** and memory controller **1001** receive an external clock signal CLK on line **1025**. Memory controller **1001** includes a phase splitter **1012**. Phase splitter **1012** represents phase splitter **100**, **500**, **600** or **900** according to the invention. Data is transferred between memory controller **1001** and memory device **1000** through data lines **1010**.

According to the invention, phase splitter **1012** receives the CLK signal on line **1025** to generate a plurality of output signals such as the CLK90, CLK180, CLK270 and CLK360 signals of FIGS. **1**, **5**, **6** and **8**. The CLK signal on line **1025** of FIG. **9** is shown as the CLK signal at node **111** or **611** of FIGS. **1** and **5**, or **6** and **8**. One of the output signals of phase splitter **1012**, such as the CLK90 signal, can be used by memory controller **1001** to generate a capture signal to capture a data signal sent from memory device **1000** during a read operation. In that read operation, the capture signal is 90 degrees out of phase with the data signal. The CLK90 signal can also be used by memory controller **1001** to generate a control or address signal, which is sent to memory device **1000** during a write operation. The control or address signal is 90 degrees out of phase with the CLK signal.

Memory device **1000** of FIG. **9** can be a dynamic random access memory (DRAM) or other types of memory circuits such as SRAM (Static Random Access Memory) or Flash memories. Furthermore, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, or DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs. Those of ordinary skill in the art will readily recognize that memory device **1000** of FIG. **9** is

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simplified to illustrate one embodiment of a memory device of the present invention and is not intended to be a detailed description of all of the features of a memory device.

FIG. 10 shows a processing system 1100 according to the invention. System 1100 includes processor 1102 connected to a memory device 1104. System 1100 can also include many other devices such as, input/output devices, and others. These other devices are omitted from FIG. 10 for ease of illustration. Processor 1102 can be a microprocessor, digital signal processor, embedded processor, microcontroller, or the like. In the embodiment of FIG. 10, processor 1102 includes a memory controller 1103. However, in other embodiments such as in the embodiment of FIG. 9, memory controller 1103 is an independent device separated from processor 1102. Processor 1102 and memory device 1104 communicate using address signals on lines 1108 control signals on lines 1110, and data signals on lines 1106. Both processor 1102 and memory device 1104 receive an external clock signal CLK on line 1125.

Memory controller 1001 includes a phase splitter 1012. Phase splitter 1012 represents phase splitter 100, 500, 600 or 900 according to the invention. Data is transferred between memory controller 1103 and memory device 1104 through data lines 1110. According to the invention, phase splitter 1130 receives the CLK signal on line 1125 to generate a plurality output signals such as the CLK90, CLK180, CLK270 and CLK360 signals of FIGS. 1, 5, 6 and 8. The output signals can be used to generate a capture signal, a control signal, or an address signal for use during a memory operation such as the read or write operation as described in FIG. 9.

CONCLUSION

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A digital phase splitter comprising:

- a first forward path to delay a first input clock signal by a first amount of delay to produce first and second output clock signals;
- a second forward path to delay a second input clock signal by a second amount of delay to produce third and fourth output clock signals, wherein the second input clock signal is unrelated to the first and second output clock signals;
- a feedback path connected to one of the forward paths to produce a feedback signal;
- a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals; and
- a controller to adjust the first amount of delay the second amount of delay such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal.

2. A digital phase splitter comprising:

- a first forward path to delay a first input clock signal by an amount of delay to produce first and second output clock signals;

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- a second forward path to delay a second input clock signal by the same amount of delay to produce third and fourth output clock signals;

- a feedback path connected one of the forward paths to produce a feedback signal;

- a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals; and

- a controller to adjust the amount of delay of the first and second forward paths such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal, wherein the first and second input clock signals are complementary signals.

3. A digital phase splitter comprising:

- a first forward path to delay first input clock signal by an amount of delay to produce first and second output clock signals;

- a second forward path to delay a second input clock signal by the same amount of delay to produce third and fourth output clock signals;

- a feedback path connected to one of the forward paths to produce a feedback signal;

- a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals; and

- a controller to adjust the amount of delay of the first and second forward paths such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal, wherein the feedback signal is the fourth output clock signal.

4. A digital phase splitter comprising:

- a first forward path to delay a first input clock signal by an amount of delay to produce first and second output clock signals;

- a second forward path to delay a second input clock signal by the same amount of delay to produce third and fourth output clock signals;

- a feedback path connected to one of the forward paths to produce a feedback signal;

- a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals; and

- a controller to adjust the amount of delay of the first and second forward paths such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal, wherein the controller includes a shift register.

5. The phase splitter of claim 1, wherein each of the first and second forward path includes first and second delay lines, each of the delay lines including a plurality of delay stages.

6. A digital phase splitter comprising:

- a first forward path to delay first input clock signal by an amount of delay to produce first and second output clock signals;

- a second forward path to delay a second input clock signal by the same amount of delay to produce third and fourth output clock signals;

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a feedback path connected to one of the forward paths to produce a feedback signal;

a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals; and

a controller to adjust the amount of delay of the first and second forward paths such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 80, 270 and 360 degrees out of phase with the first input clock signal wherein each of the first and second forward path includes first and second delay lines, each of the delay lines including a plurality of delay stages, and wherein a delay resolution of the phase splitter is equal to two delay stages when the feedback and first input clock signals are synchronized.

7. The phase splitter of claim 6, wherein each of the delay stages includes one delay element.

8. The phase splitter of claim 7, wherein the delay element is an inverter.

9. A digital phase splitter comprising:

a first delay line to apply amount of delay to a first input clock signal to produce a first output clock signal;

a second delay line connected to the first delay line to apply a second amount of delay to the first output clock signal to produce a second output clock signal;

a third delay line to apply a third amount of delay to a second input clock signal to produce a third output clock signal, wherein the second input clock signal is unrelated to the first and second output clock signals;

a fourth delay line connected to the third delay line to apply a fourth amount of delay to the third output clock signal to produce a fourth output clock signal;

a feedback path connected to one of the delay lines to produce a feedback signal;

a phase detector to provide shifting signals based on a difference between phases of the feedback and first input clock signals; and

a controller to adjust the amount of delay applied to all of the delay lines such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are one fourth, one-half, three-fourths and one clock cycle delayed from the first input clock signal.

10. A digital phase splitter comprising:

a first delay line to apply an amount of delay to a first input clock signal to produce a first output clock signal;

a second delay line connected to the first delay line to apply the same amount of delay to the first output clock signal to produce a second output clock signal;

a third delay line to apply the same amount of delay to a second input clock signal to produce a third output clock signal;

a fourth delay line connected to the third delay line to apply the same amount of delay to the third output clock signal to produce a fourth output clock signal;

a feedback path connected to one of the delay lines to produce a feedback signal;

a phase detector to provide shifting signals based on a difference between phases of the feedback and first input clock signals; and

a controller to adjust the amount of delay applied to all of the delay lines such that when the feedback and first input clock signals are synchronized the first, second,

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third and fourth output clock signals are one fourth, one-half, three-fourths and one clock cycle delayed from the first input clock signal, wherein second input clock signal is an inverse of the first clock signal.

11. The phase splitter of claim 9, wherein each of the delay lines includes a plurality of delay stages.

12. A digital phase splitter comprising:

a first delay line to apply an amount of delay to a first input clock signal to produce a first output clock signal;

a second delay line connected to the first delay line to apply the same amount of delay to the first output clock signal to produce a second output clock signal;

a third delay line to apply the same amount of delay to a second input clock signal to produce a third output clock signal;

a fourth delay line connected to the third delay line to apply the same amount of delay to the third output clock signal to produce a fourth output clock signal;

a feedback path connected to one of the delay lines to produce a feedback signal;

a phase detector to provide shifting signals based on a difference between phases of the feedback and first input clock signals; and

a controller to adjust the amount of delay applied to all of the delay lines such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are one fourth, one-half, three-fourths and one clock cycle delayed from the first input clock signal, wherein each of the delay lines includes a plurality of delay stages, and wherein a delay resolution of the phase splitter is equal to two delay stages.

13. The phase splitter of claim 12, wherein each of the delay stages includes one delay element.

14. The phase splitter of claim 13, wherein the delay element is an inverter.

15. A digital phase splitter comprising:

a forward path to delay a first input clock signal by an amount of delay to produce first and second output clock signals;

a feedback path connected the forward path to produce a feedback signal;

a phase detector to provide shifting signals based on a difference between the phases of the feedback signal and a second input clock signal; and

a controller to adjust the amount of delay of the forward paths such that when the feedback and second input clock signals are synchronized, the first and second output clock signals are 90 and 180 degrees out of phase with the first input clock signal.

16. The phase splitter of claim 15, wherein the first and second input clock signals are complementary signals.

17. The phase splitter of claim 15, wherein the feedback signal is the second output clock signal.

18. The phase splitter of claim 17, wherein a delay resolution of the phase splitter is equal to 200 picoseconds.

19. The phase splitter of claim 15, wherein the forward path includes first and second delay lines, each of the delay lines including a plurality of delay stages.

20. The phase splitter of claim 19, wherein a delay resolution of the phase splitter is equal to two delay stages.

21. The phase splitter of claim 20, wherein each of the delay stages includes one delay element.

22. The phase splitter of claim 21, wherein the delay element is an inverter.

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23. A digital phase splitter comprising:

- a first delay line to apply amount of delay to a first input clock signal to produce a first output clock signal;
- a second delay line connected to the first delay line to apply the same amount of delay to the first output clock signal to produce a second output clock signal;
- a feedback path connected to the second delay line to produce a feedback signal;
- a phase detector to provide shifting signals based on a difference between phases of the feedback signal and a second input clock signal; and
- a controller to adjust the amount of delay applied to the first and second delay lines such that when the feedback and second input clock signals are synchronized, the first and second output clock signals are one-fourth and one-half clock cycle delayed from the first input clock signal.

24. The phase splitter of claim **23**, wherein second clock signal is an inverse of the first clock signal.

25. The phase splitter of claim **24**, wherein a delay resolution of the phase splitter is equal to two delay stages.

26. The phase splitter of claim **25**, wherein each of the delay stages includes one delay element.

27. The phase splitter of claim **26**, wherein the delay element is an inverter.

28. A digital phase splitter comprising:

- a forward path to delay a first input clock signal by an amount of delay to produce first and second output clock signals;
- a feedback path connected the forward path to produce a feedback signal;
- a first phase detector to provide a first set of shifting signals based on a difference between the phases of the feedback signal and a second input clock signal;
- a second phase detector to provide a second set of shifting signals based on a difference between the phases of the feedback signal and the second input clock signal; and
- a controller to adjust the amount of delay of the forward path such that when the feedback and second input clock signals are synchronized, the first and second output clock signals are 90 and 180 degrees out of phase with the first input clock signal.

29. The phase splitter of claim **28**, wherein the first and second input clock signals are complementary signals.

30. The phase splitter of claim **28**, wherein the feedback signal is the second output clock signal.

31. The phase splitter of claim **28**, wherein the forward path includes first and second delay lines, each of the delay lines including:

- a coarse delay segment including a plurality of coarse delay stages; and
- a fine delay segment including a plurality of fine delay stages, wherein a delay of each of the fine delay stages is smaller than a delay of each of the coarse delay stages.

32. The phase splitter of claim **31**, wherein a delay resolution of the phase splitter is equal to two coarse and two fine delay stages.

33. The phase splitter of claim **32**, wherein each of the coarse delay stages includes one delay element.

34. The phase splitter of claim **33**, wherein the delay element is an inverter.

35. The phase splitter of claim **32**, wherein a delay of each of the coarse delay stages is about 100 picoseconds, and a delay of each of the fine delay stages is about 30 picoseconds.

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36. A digital phase splitter comprising:

- a first delay line to apply an amount of delay to a first input clock signal to produce a first output clock signal;
- a second delay line connected to the first delay line to apply the same amount of delay to the first output clock signal to produce a second output clock signal;
- a feedback path connected to the second delay line to produce a feedback signal;
- a first phase detector to provide a first set of shifting signals based on a difference between the phases of the feedback signal and a second input clock signal;
- a second phase detector to provide a second set of shifting signals based on a difference between the phases of the feedback signal and the second input clock signal; and
- a controller to adjust the amount of delay of the forward path such that when the feedback and second input clock signals are synchronized, the first and second output clock signals are 90 and 180 degrees out of phase with the first input clock signal.

37. The phase splitter of claim **36**, wherein the first and second input clock signals are complementary signals.

38. The phase splitter of claim **36**, wherein the feedback signal is the second output clock signal.

39. The phase splitter of claim **36**, wherein each of the first and second delay lines includes:

- a coarse delay segment including a plurality of coarse delay stages; and
- a fine delay segment including a plurality of fine delay stages, wherein a delay of each of the fine delay stages is smaller than a delay of each of the coarse delay stages.

40. The phase splitter of claim **39**, wherein a delay resolution of the phase splitter is equal to two coarse and two fine delay stages.

41. The phase splitter of claim **40**, wherein each of the coarse delay stages includes one delay element.

42. The phase splitter of claim **41**, wherein the delay element is an inverter.

43. The phase splitter of claim **40**, wherein a delay of each of the coarse delay stages is about 100 picoseconds and a delay of each of the fine delay stages is about 30 picoseconds.

44. A memory device comprising:

- memory cells;
- a capture circuit; and
- a phase splitter connected to provide a clock signal to the capture circuit to capture a data signal from the memory cells, the phase splitter comprising:
 - a first forward path delay a first input clock signal by a first amount of delay to produce first and second output clock signals;
 - a second forward path to delay a second input clock signal by a second amount of delay to produce third and fourth output clock signals, wherein the second input clock signal is unrelated to the first and second output clock signals;
 - a feedback path connected to one of the forward paths to produce a feedback signal;
 - a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals; and
 - a controller to adjust the first amount of delay and the second amount of delay such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal.

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45. A system comprising:
 a processor;
 a memory device; and
 a controller connected between the processor and the memory device, the controller having a phase splitter to generate multiple signals, the phase splitter comprising:
 a first forward path delay a first input clock signal by a first amount of delay to produce first and second output clock signals;
 a second forward path to delay a second input clock signal by a second amount of delay to produce third and fourth output clock signals, wherein the second input clock signal is unrelated to the first and second output clock signals;
 a feedback path connected to one of the forward paths to produce a feedback signal;
 a phase detector to provide shifting signals based on a difference between the phases of the feedback and first input clock signals; and
 a controller to adjust the first amount of delay and the second amount of delay such that when the feedback and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal.

46. A method of generating multiple clock signals, the method comprising:

delaying a first clock signal with a first amount of delay to generate first and second output clock signals;

delaying a second clock signal with a second amount of delay to generate third and fourth output clock signals, wherein the second clock signal is unrelated to the first and second output clock signals;

generating a feedback signal from the fourth output clock signal;

generating shifting signals based on a difference between the phases of the feedback and first clock signals; and
 adjusting the amount of delay of the first and second forward paths such that when the feedback and first clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first clock signal.

47. The method of claim 46, wherein delaying the first clock signal includes:

propagating the first clock signal through a first delay line to generate the first output clock signal; and

propagating the first output clock signal through a second delay line to generate the second output clock signal.

48. The method of claim 47, wherein propagating each of the first clock signal and the first output clock signal includes propagating each signal through a plurality of delay stages, herein each of the delay stages includes one delay element.

49. The method of claim 46, wherein delaying the second clock signal includes:

propagating the second input clock signal through a first delay line to generate the third output clock signal; and

propagating the third output clock signal through a second delay line to generate the fourth output clock signal.

50. The method of claim 49, wherein propagating each of the second clock signal and the third output clock signal includes propagating each signal through a plurality of delay stages herein each of the delay stages includes one delay element.

51. A method of generating multiple clock signals, the method comprising:

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receiving first and second input clock signals;
 propagating the first input clock signal through a number of delay stages of a first delay line to generate a first output clock signal;

propagating the first output clock signal through the same number of delay stages of a second delay line to generate a second output clock signal;

propagating the second input clock signal through the same number of delay stages of a third delay line to generate a third output clock signal;

propagating the third output clock signal through the same number of delay stages of a fourth delay line to generate a fourth output clock signal;

comparing a phase difference between the fourth output clock and first input clock signals to determine to provide shifting signals; and

adjusting the amount of delay based on the shifting signals such that when the fourth output clock and first input clock signals are synchronized, the first, second, third and fourth output clock signals are 90, 180, 270 and 360 degrees out of phase with the first input clock signal.

52. A method of generating multiple clock signals, the method comprising:

delaying a first input clock signal to generate a first output clock signal;

delaying the first output clock signal to generate a second output clock signal;

generating a feedback signal from the second output clock signal; and

synchronizing the feedback signal and a second input clock signal such that the first and second output clock signals are one-fourth and one-half clock cycle delayed from the first input clock signal.

53. The method of claim 52, wherein delaying a first input and delaying the first output clock signals includes propagating the signals through a plurality of delay stages of a coarse delay segment and a plurality of delay stages of a fine delay segment, wherein a delay of each of the fine delay stages is smaller than a delay of each of the coarse delay stages.

54. A method of generating multiple clock signals, the method comprising:

delaying a first input clock signal to generate a first output clock signal;

delaying the first output clock signal to generate a second output clock signal;

delaying a second input clock signal to generate a third output clock signal;

delaying the third output clock signal to generate a fourth output clock signal;

generating a feedback signal from the fourth output clock signal; and

synchronizing the feedback signal and the second input clock signals such that the first, second, third and fourth output clock signals are one-fourth, one-half three-fourths and one clock cycle delayed from the first input clock signal.

55. The method of claim 54, wherein delaying a first input and delaying the first output clock signals includes propagating the signals through a plurality of delay stages of a coarse delay segment and a plurality of delay stages of a fine delay segment, wherein a delay of each of the fine delay stages is smaller than a delay of each of the coarse delay stages.

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56. The method of claim **55**, wherein delaying a second input and the third output clock signals includes propagating the signals through a plurality of delay stages of a coarse delay segment and a plurality of delay stages of fine delay

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segment, wherein a delay of each of the fine delay stages is smaller than a delay of each of the coarse delay stages.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,950,487 B2
DATED : September 27, 2005
INVENTOR(S) : Lin et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Drawings.

Sheet 9 of 10, in Fig (9), box 1002, delete "MEMEORY" and insert -- MEMORY --.

Column 3,

Line 53, delete "Mux" and insert -- MUX --.

Line 62, delete "o" and insert -- to --.

Column 9,

Line 17, after "1108" insert -- , --.

Line 58, after "delay" insert -- and --.

Column 10,

Line 4, after "connected" insert -- to --.

Lines 12, 33 and 53, delete "80" and insert -- 180 --.

Lines 18 and 62, after "delay" insert -- a --.

Column 11,

Line 9, delete "80" and insert -- 180 --.

Line 23, after "apply" insert -- an --.

Lines 27 and 34, delete "sign" and insert -- signal --.

Line 67, after "synchronized" insert -- , --.

Column 12,

Line 43, after "connected" insert -- to --.

Column 13,

Line 2, after "apply" insert -- an --.

Line 31, after "connected" insert -- to --.

Column 14,

Line 31, delete "th" and insert -- than --.

Line 40, after "picoseconds" insert -- , --.

Line 49, after "path" insert -- to --.

Column 15,

Line 7, after "path" insert -- to --.

Line 21, after "amount" delete "o" and insert -- of --.

Line 54, delete "herein" and insert -- wherein --.

Line 57, after "second" delete "input".

Line 64, delete "herein" and insert -- wherein --.

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,950,487 B2
DATED : September 27, 2005
INVENTOR(S) : Lin et al.

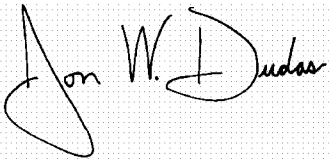
Page 2 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 16,
Line 58, after "one-half" insert -- , --.

Signed and Sealed this

Seventh Day of February, 2006

A handwritten signature in black ink on a light gray dotted background. The signature reads "Jon W. Dudas" in a cursive style. The "J" is large and loops around the "on". The "W" and "D" are also prominent.

JON W. DUDAS
Director of the United States Patent and Trademark Office