SENSING METHOD AND APPARATUS FOR RESISTANCE MEMORY DEVICE

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Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

Appl. No.: 10/790,242
Filed: Mar. 2, 2004

Prior Publication Data

Related U.S. Application Data
Continuation of application No. 10/422,849, filed on Apr. 25, 2003, now Pat. No. 6,741,490, which is a continuation of application No. 09/939,655, filed on Aug. 28, 2001, now Pat. No. 6,577,525.

Int. Cl. .......................... G11C 11/00
U.S. Cl .......................... 365/148, 365/158
Field of Search .................. 365/148, 158, 365/171, 173, 209

ABSTRACT

An MRAM memory integrated circuit is disclosed. Resistance, and hence logic state, is determined by discharging a first charged capacitor through an unknown cell resistive element to be sensed at a fixed voltage, and a pair of reference capacitors. The rate at which the parallel combination of capacitors discharge is between the discharge rate associated with a binary '1' and '0' value, and thus offers a reference for comparison.

21 Claims, 7 Drawing Sheets
FIG. 2

[Diagram of a circuit with OP AMP, VA, VA, 220, 222, 240, 246, 224, 225, 109, 204, 120, 200, Isense connections.]
FIG. 6
SENSING METHOD AND APPARATUS FOR RESISTANCE MEMORY DEVICE

FIELD OF THE INVENTION

The present invention relates to the field of resistor-based memory circuits. More particularly, it relates to a method for precisely sensing the resistance value of a resistor-based memory cell, for example, a Magnetic Random Access Memory (MRAM) magnetic memory cell.

BACKGROUND OF THE INVENTION

A resistor-based memory such as a magnetic random access memory (MRAM) typically includes an array of resistor-based magnetic memory cells. The logic state of such a magnetic memory cell is indicated by its resistance. One resistance value, e.g., the higher value, may be used to signify a logic high while another resistance value, e.g., the lower value, may be used to signify a logic low. The value stored in each memory cell can be determined by measuring the resistance value of the cell to determine whether the cell corresponds to a logic high or low. Such direct measurements are often difficult to simply and easily implement and require a number of comparators which increases the cost and size of the memory circuit. A simplified, more reliable method of sensing the resistance value of a resistor-based memory cell is desired.

SUMMARY OF THE INVENTION

The present invention provides a simple and reliable method and apparatus for sensing the logic state of a resistor-based memory cell. Resistance is measured by first charging the first capacitor to a predetermined voltage, discharging the first capacitor through a resistance to be measured while discharging a second capacitor through an associated reference resistance of known value and comparing the discharge characteristics e.g., the discharge voltage of two capacitors to determine a value of resistance to be measured relative to the reference resistance.

In one exemplary embodiment, a pair of second capacitors are used, each discharging through an associated reference resistance, one having a value corresponding to one possible resistance value of the resistance to be measured and the other having a value corresponding to another possible resistance value of the resistance to be measured. The combined discharge characteristics of the pair of second capacitors, e.g., an average of the discharge capacitor voltage, is compared with the discharge characteristics e.g., the discharge voltage of the first capacitor to determine a value of the resistance to be measured relative to an average value of the two reference resistances.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features and advantages of the invention will become more apparent from the detailed description of the exemplary embodiments of the invention given below with reference to the accompanying drawings in which:

FIG. 1 shows the invention employed in an exemplary MRAM device;

FIG. 2 shows a schematic diagram of one aspect of the invention;

FIG. 3 shows a schematic diagram of an additional aspect of the invention;

FIG. 4 shows the discharge rate characteristics of capacitors employed in the invention;

FIG. 5 shows a schematic diagram of an additional aspect of the invention;

FIG. 6 shows a schematic diagram of an additional aspect of the invention; and

FIG. 7 shows the invention utilized in a computer system.

DETAILED DESCRIPTION OF THE INVENTION

A portion of a MRAM array 100 with which the present invention may be used is shown in FIG. 1. The logical state of an MRAM memory element e.g., 204 is represented by the resistance of that element. In the present invention, resistance is determined by holding a voltage constant across a cell’s resistive element and comparing a voltage produced by the current that flows through that resistive element with a voltage produced by the current flow through a known reference resistance. To read the binary state of a memory cell element, the absolute magnitude of resistance need not be known; only whether the resistance is above or below a value that is intermediate to the logic high and logic low values. Accordingly, to provide a reference current flow for comparison purposes the resistive elements within rightmost column 108 of array 100 are preprogrammed to hold all ‘0’ values, while those within column 110 immediately to the left are preprogrammed to hold all ‘1’ values. The current flowing through these two columns when a particular row line of the array 100 is selected by grounding a rowline, e.g., rowline 120, will herefore be designated as I₀ and I₁, as shown in FIG. 1.

During the reading process, all column and row lines are driven with the same voltage Vᵣ, except for the one row line, e.g., 120 that is desired to be read. That row line 120 is driven to ground. When row 120 is grounded, a resistive element of a selected column, e.g., column 109, can be read by a sensing circuit 300 described below. As shown in FIG. 1, both ends of all resistive elements not being measured are maintained at the same potential, Vᵣ. Thus, unwanted current flow through these resistive elements due to “sneak” resistance is negligible. A current I inout flows through the grounded resistive element of a selected column within the row 120 for allowing measurement of the resistance by the sensing circuit 300 (not shown in FIG. 1).

FIG. 2 shows a circuit 200 for regulating current through and voltage across a resistive element 204 being measured. An operational amplifier 220 has one terminal 222 connected to Vᵣ, while the other terminal 224 is connected to the column line 109 for the resistance element 204 which is being sensed. The gate 242 of NMOS transistor 240 is connected to the output of operational amplifier 220. The source 246 of transistor 240 is connected to one terminal of the resistive element 204 being read, while the other terminal of resistive element 204 is driven to ground by the grounding of wordline 120 described earlier. Operational amplifier 220 and transistor 240 act in concert to keep one terminal of resistive element 204 stable at Vᵣ despite the fact that the other terminal is grounded. In this way, I inout can flow through transistor 240 and resistive element 204, while current lost through sneak resistor 225 is minimized.

To sense the amount of resistance of resistance element 204, the current flow through resistance element 204 must be
determined, since the voltage across resistance element 204 is held constant at $V_A$. FIG. 3 shows how the current regulating circuit 200 combined with a voltage comparator 304, and a reference voltage generating circuit 115 provide a method and apparatus for determining current flow through sensed resistance element 204. As shown in FIG. 3, the active wordline 120 is also connected to reference resistors R0 and R1 associated with column lines 108 and 110, which are pre-set to ‘0’ and ‘1’ resistance values respectively. Each column line of array 110 which has resistance elements which may be written to or read has its own sensing circuit and comparator which are active when the column is addressed to select with the grounded rowline, whose resistive memory element within a given row is being read. Thus, connection line 320 shows how the reference voltage generating circuit 115 is connected to other columns of array 100. As noted, each column line (e.g. 109 shown in FIG. 3) has a voltage having a reference input 113 and sensed voltage input 116.

The reference voltage generating circuit 115 includes a first 202 and second 244 regulating circuit each associated with a respective reference resistance element 108, 110. These regulating circuits respectively hold the voltage across reference resistors elements 108 and 110 at $V_A$ in the manner described above with reference to FIG. 2. The reference resistors R0, R1 have respective known resistance values corresponding to one of the logic states of a memory element and the other corresponding to the other possible logic state. The reference voltage generating circuit 115 also includes capacitors $C_1$ and $C_0$ respectively associated with the reference resistance elements $R_0$ and $R_1$. Each of the capacitors $C_1$ and $C_0$ has one lower terminal grounded and the other upper terminal connectable to a common voltage line 132 through a respective switch element 134, 136. The switch elements 134, 136 are configured to connect the upper terminals of the capacitors $C_1$, $C_0$ to either a source of voltage $V_A$ or to the common voltage line 132. The common voltage line 132 is connected to the reference voltage input 113 of comparator 304.

As noted, the comparator 304 also has a voltage input 116. This is connected through another switch element 206 to an upper terminal of a sensing capacitor $C_{sense}$, the lower terminal of which is grounded. Switch element 206 is adapted to connect the upper terminal of comparator $C_{sense}$ to either a source of voltage $V_A$ or to the input 116 of comparator 304. The input 116 is also connected to the upper (drain) terminal of transistor 240 which has its source terminal connected to the resistance element 204, the resistance of which is to be measured.

All of the switch elements 134, 136 and 206 switch together to either connect the upper terminals of capacitors $C_{sense}$, $C_1,$ or $C_0$ to the voltage $V_A$, or to connect the upper terminal of capacitor $C_{sense}$ to input 116 and the upper terminals of capacitors $C_1$ and $C_0$ to common voltage line 132. When the switch elements are in the latter condition the capacitors $C_{sense}$, $C_1$, and $C_0$ are connected in a way which provides the current flows 10, 11 and $I_{sense}$ through respective resistance elements R0, R1 and 204.

The circuit of FIG. 3 operates as follows. Capacitors $C_{sense}$, $C_1$, and $C_0$ are first fully charged to $V_A$ by switch elements 134, 136, 206 simultaneously connecting their upper terminals to a $V_A$ voltage source. After the capacitors $C_{sense}$, $C_1$, and $C_0$ are charged the switch elements 134, 136, and 206 are simultaneously operated to connect the upper terminal of capacitor $C_{sense}$ to input 116 and the upper terminal of capacitors $C_1$ and $C_0$ to the common voltage line 132. As a result all three capacitors begin discharging in unison in the direction symbolized by current flow arrows $I_{sense}$, $I_1$, and $I_0$. The rate at which the capacitors $C_1$ and $C_0$ discharge is determined by the resistance of the path through which they discharge.

The capacitor $C_{sense}$ will also discharge through resistance element 204 and the decaying voltage on capacitor 204 is applied to sense voltage input 116 of comparator 304. The discharge of both capacitors simultaneously will provide a reference voltage on voltage line 132 which is the average voltage instantaneously on capacitors $C_1$, $C_0$. Thus, as capacitors $C_1$ and $C_0$ discharge, this average voltage will decay. This average voltage is applied to the reference voltage input of comparator 304. The capacitor $C_{sense}$ will discharge significantly faster if resistance element 204 has a resistance representing a ‘0’ value (e.g. 950 kΩ) than a resistance representing a ‘1’ value (e.g. 1 MΩ). Consequently, the voltage on $V_{sense}$ will discharge either more slowly or more quickly than the average voltage discharge of $C_1$ and $C_0$; hereafter noted as $V_{avg}$. The combined average voltage across capacitors $C_1$ and $C_0$ as seen by comparator 304 decays with time as shown by $V_{avg}$ in FIG. 4. $V_{avg}$ falls between the decaying voltage on capacitor $C_{sense}$ when a logical ‘1’ and a ‘0’ resistance is set in resistance element 204. Because the resistive memory element 204 being sensed will either store a 1 or a 0, its discharge voltage $V_{sense}$ will (intentionally) never be equal to $V_{avg}$ instead $V_{sense}$ will always be measurably higher or lower than $V_{avg}$. Accordingly, the difference between the sensed and reference discharge voltages ($V_{sense}$ and $V_{avg}$) will be compared by the comparator 304 at sense time $t_{sense}$ which will provide an electrical ‘1’ or ‘0’ output representing the stored logic value of resistance element 204. Thus, determining whether a resistive memory element holds a ‘1’ or a ‘0’ does not require quantitatively measuring $V_{sense}$ instead, it is only necessary to compare $V_{sense}$ with $V_{avg}$ using a comparator 304. A circuit for comparing $V_{sense}$ to $V_{avg}$ can be achieved with less components than a circuit for quantitatively measuring $V_{sense}$. The frequency with which the voltages $V_{sense}$ and $V_{avg}$ can be compared is limited only by the capacitance values of $C_0$, $C_1$, and $C_{sense}$ which must also produce an integrating effect across their respective resistance elements.

FIG. 5 shows an alternative embodiment in which only a single capacitor $C_{av}$, is used in the reference voltage across 115/z. In such an embodiment, the desired $V_{av}$ could be obtained by discharging capacitor $C_{av}$ across a single resistor $R_{median}$, of known value which lies between resistance values corresponding to a logical ‘0’ and ‘1’ value. For example, if 950 kΩ corresponds to a typical MRAM resistance for a binary ‘0’, and 1 MΩ corresponds to the typical MRAM resistance for a binary ‘1’, then a median resistance value is set for example at 975 kΩ. By discharging capacitor $C_{av}$ across such a median resistance, a value for $V_{av}$ for comparison with $V_{sense}$ can be provided. In this embodiment, the $R_{median}$ resistance can be provided by using a single column, e.g. 108, of reference resistance elements in array 100 having this value, or dispensing with reference resistance element in the array in favor of an out-of-array reference resistance element which has the $R_{median}$ value.

FIG. 6 illustrates how the current regulating circuit 200 and sensing circuit 300 of the invention are arranged with a memory array 100. In FIG. 6, the columns which connect with storage resistive elements are labeled 107, 109, while the reference columns remain shown in 108, 110. The sensing circuit 300 of the present invention compares two discharge voltages $V_{sense}$ and $V_{av}$ and immediately
makes a determination which logical value to output on bit-out line 330. Thus, a method and apparatus for quickly measuring MRAM values while minimizing the number of necessary components is achieved.

FIG. 7 is a block diagram of a processor-based system 350 utilizing a MRAM array 100 constructed in accordance with one of the embodiments of the present invention. The processor-based system 350 may be a computer system, a process control system or any other system employing a processor and associated memory. The system 350 includes a central processing unit (CPU) 352, e.g., a microprocessor, that communicates with the MRAM array 100 and an I/O device 354 over a bus 356. It must be noted that the bus 356 may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus 356 has been illustrated as a single bus. A second I/O device 306 is illustrated, but is not necessary to practice the invention. The processor-based system 350 also includes read-only memory (ROM) 360 and may include peripheral devices such as a floppy disk drive 362 and a compact disk (CD) ROM drive 364 that also communicates with the CPU 352 over the bus 356 as is well known in the art.

While the invention has been described and illustrated with reference to specific exemplary embodiments, it should be understood that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.

What is claimed is:

1. A sensing circuit for sensing a resistance value of a first resistive element in a memory device, the circuit comprising:
   a first capacitor and at least one reference capacitor;
   a charging circuit for charging said first and said at least one reference capacitors to a predetermined voltage value;
   at least one reference resistive element;
   a first discharge circuit for discharging said first capacitor through the first resistive element, said first discharge circuit having a first discharge characteristic;
   a second discharge circuit for discharging said at least one reference capacitor through said reference resistive element, said second discharge circuit having a second discharge characteristic;
   and a comparison circuit for comparing said first discharge characteristic to said second discharge characteristic.

2. The sensing circuit of claim 1 wherein said first and second discharge characteristics are voltage levels.

3. The sensing circuit of claim 2 wherein said at least one reference capacitor comprises first and second reference capacitors and said at least one reference resistive element comprises first and second resistive elements respectively associated with said first and second reference capacitors, wherein said first reference capacitor discharges through said first reference resistive element and said second reference capacitor discharges through said second reference resistive element.

4. The sensing circuit of claim 3 wherein said first and second reference resistive elements respectively have resistance values corresponding to a binary “1” value and a binary “0” value.

5. The sensing circuit of claim 1 further comprising a regulation circuit for maintaining a predetermined voltage across said selected resistive element during discharge of said capacitors.

6. The sensing circuit of claim 5 wherein said regulation circuit comprises a voltage source and a switch for selectively connecting said voltage circuit to said capacitors.

7. A resistive memory sensing apparatus comprising:
   a method and apparatus for maintaining a predetermined voltage across said selected resistive element during discharge of said capacitors.
   first discharge means for discharging a first stored electrical charge through a first resistive element according to a first, measurable discharge characteristic, said first resistive element having one of a first or a second programmed resistance;
   second discharge means for discharging a second stored electrical charge through a reference resistive element, said second discharge means discharging according to a second, predictable discharge characteristic; and
   means for comparing said first and said second discharge characteristics and for outputting a result based on said comparison.

8. The resistive memory sensing apparatus of claim 7 wherein the first and second discharge characteristics comprise a rate of decaying voltage on said first and second discharge means respectively.

9. The resistive memory sensing apparatus of claim 7 wherein said first and second programmed resistances are resistive values corresponding to a binary logic value of “1” and a logic value of “0” respectively.

10. The resistive memory sensing apparatus of claim 9 wherein said reference resistive element has a reference resistance value of between a value corresponding to a logical “1” and a value corresponding to a logical “0.”

11. The resistive memory sensing apparatus of claim 7 wherein said second discharge means comprises first and second reference capacitive structures, and said reference resistive element comprises first and second reference resistive elements corresponding to and associated with a respective one of said first and second reference capacitive structures.

12. The resistive memory sensing apparatus of claim 11 wherein said first reference resistance element has a resistance value approximately equal to a value corresponding to a logical “1” value and wherein said second reference resistance element has a resistance value approximately equal to a value corresponding to a logical “0” value.

13. The resistive memory sensing apparatus of claim 7 further comprising a switch means for selectively connecting said applying means to selective ones of said plurality of storing means.

14. A method for converting a resistance into a logic state signal, said method comprising:
   charging a first capacitor and at least one reference capacitor;
   discharging the first capacitor through a first resistance element;
   discharging the at least one reference capacitor through at least one reference resistance element;
   sensing a first discharge characteristic of said first capacitor and a second discharge characteristic of said at least one reference capacitor;
   comparing said first and second discharge characteristics; and
   outputting a logic signal based on said comparison.

15. The method of claim 14 wherein said charging steps comprise connecting each capacitor to a common voltage source having a predetermined voltage level.

16. The method of claim 14 wherein said step of sensing a first and second discharge characteristic comprises taking a quantitative measurement of at least one of voltage and current.
17. The method of claim 14 wherein said sensing said second discharge characteristic of said at least one reference capacitor comprises sensing a discharge characteristic of a first reference capacitor and sensing a discharge characteristic of a second reference capacitor and averaging said discharge characteristics.

18. A method of reading a logic state from a resistance memory device comprising:

- quantitatively measuring a discharge characteristic from each capacitive element;
- comparing said quantitative measurements from said first and said at least one second capacitive elements; and
- outputting a value representing said comparison.

19. The method of claim 18 wherein said step of charging said first and at least one second capacitive elements comprises applying a reference voltage to each capacitive element.

20. The method of claim 18 wherein said step of quantitatively measuring a discharge characteristic comprises measuring a rate of voltage decay at each of said first and at least one second capacitive elements.

21. The method of claim 18 wherein said step of comparing said quantitative measurements from said first and said at least one second capacitive elements comprises inputting an output of said first resistance element and an output of said reference circuit into a comparator.
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,
Line 8, “Pat. No. 6,741,490 which” should read -- Pat. No. 6,741,490, issued on May 25, 2004, which --.

Signed and Sealed this

Twenty-ninth Day of November, 2005

[Signature]

JON W. DUDAS
Director of the United States Patent and Trademark Office