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Baker

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(54) **HIGH SPEED LOW POWER INPUT BUFFER**

(75) Inventor: **R. Jacob Baker**, Meridian, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

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(52) **U.S. Cl.** **327/55**; 327/56
(58) **Field of Search** 327/52, 53, 54, 327/55, 56, 57, 112, 74, 65, 77, 563; 330/252, 253, 255, 261; 365/184.09

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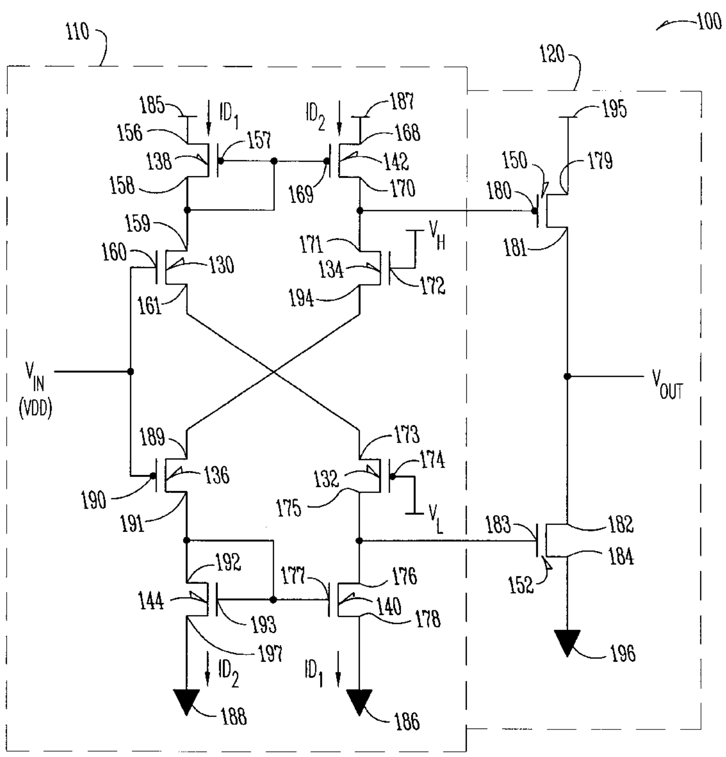
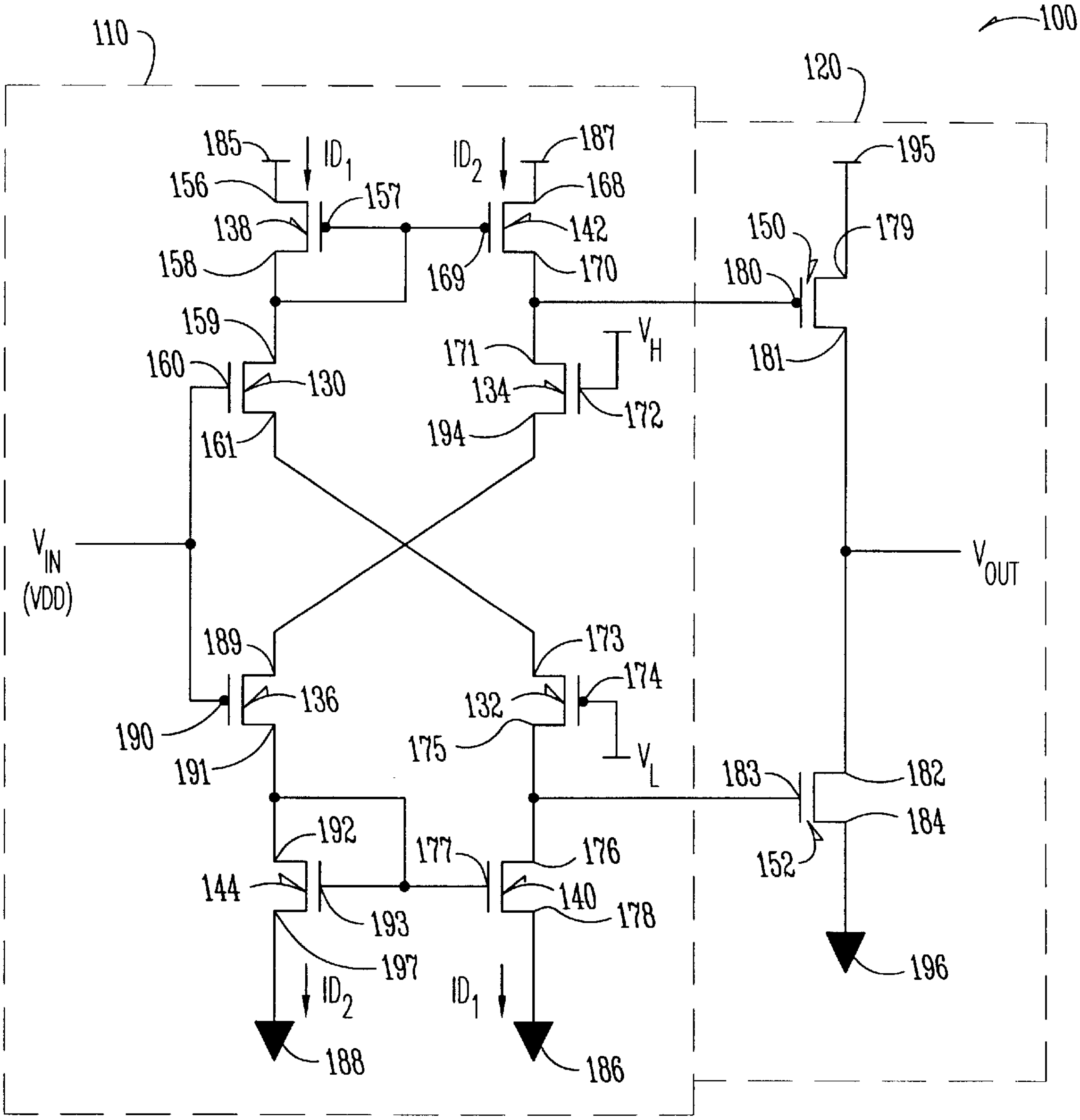
Primary Examiner—Matthew Smith
Assistant Examiner—Paul Dinh
(74) *Attorney, Agent, or Firm*—Schwegman, Lundberg, Woessner & Kluth, P.A.

(57) **ABSTRACT**

The input buffer circuit includes an input stage providing a switching point voltage based on a predetermined switching point set between a first and second reference voltages that maximizes the high and low noise margins of the input buffer. The input buffer circuit further includes an output stage. The output stage is coupled to the input stage. The output stage receives the switching point voltage from the input stage and amplifies the switching point voltage to a full logic level voltage.

76 Claims, 8 Drawing Sheets

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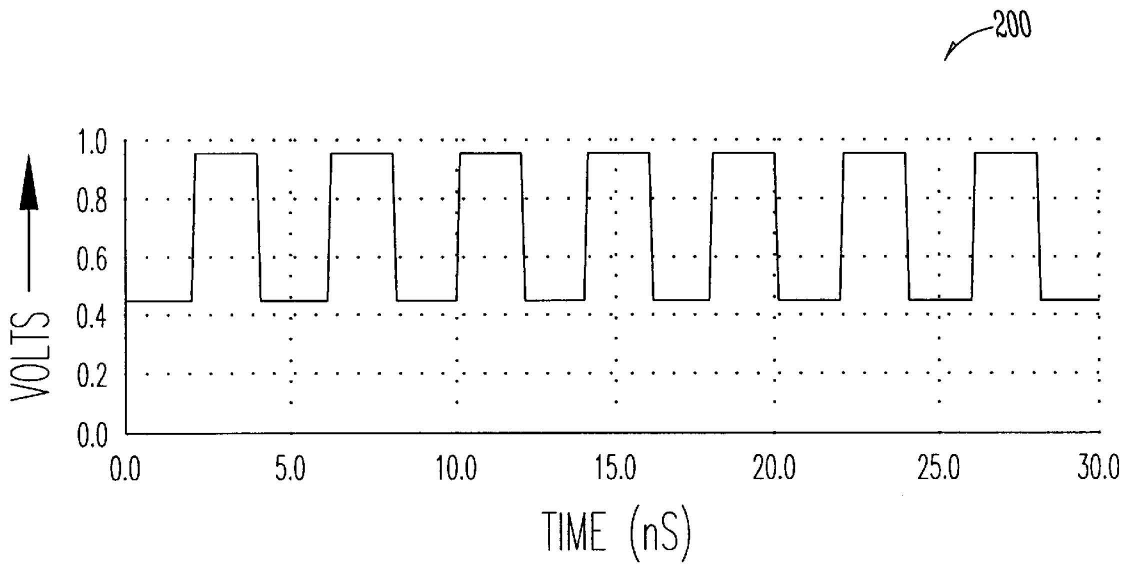
194
172
VH
195
150
179
180
181
VIN
(VDD)
VOUT
189
136
190
191
173
174
132
175
VL
183
182
184
152
192
144
193
197
ID2
177
176
140
178
ID1
188
186
196

Fig. 1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0.6
0.4
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10.0
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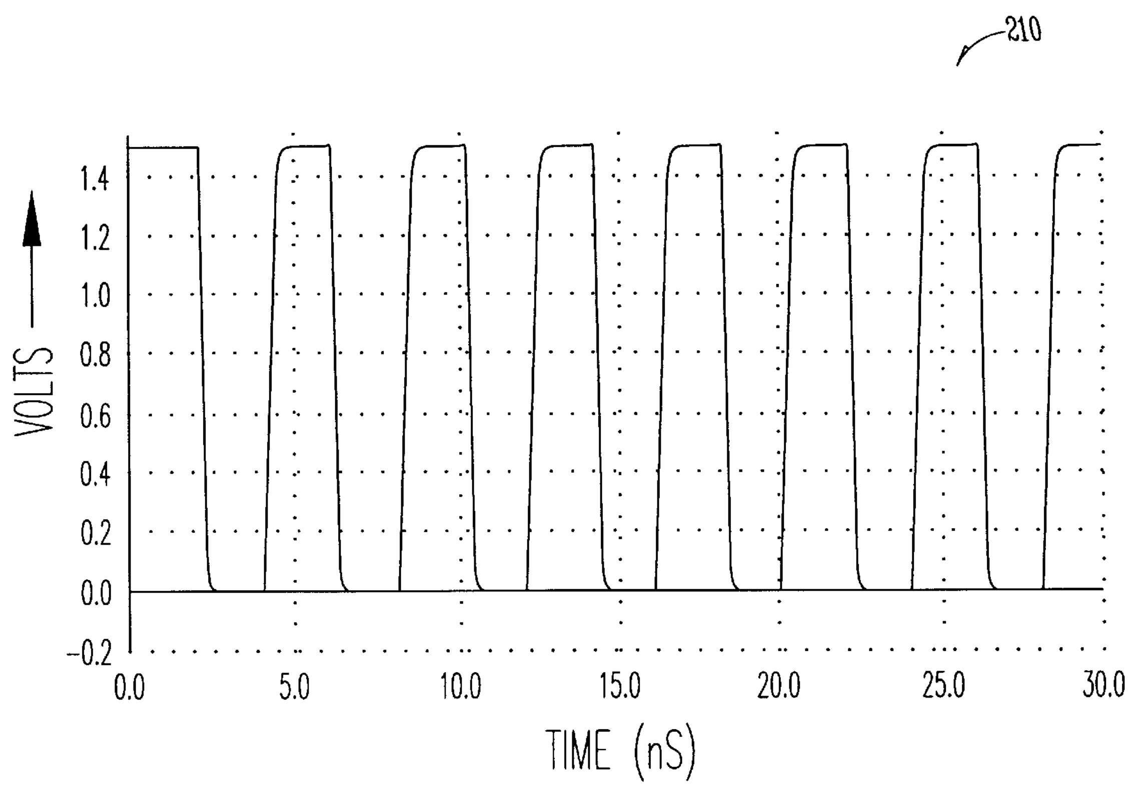
25.0
30.0
TIME (nS)

Fig.2A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1.4
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0.2
0.0
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VOLTS
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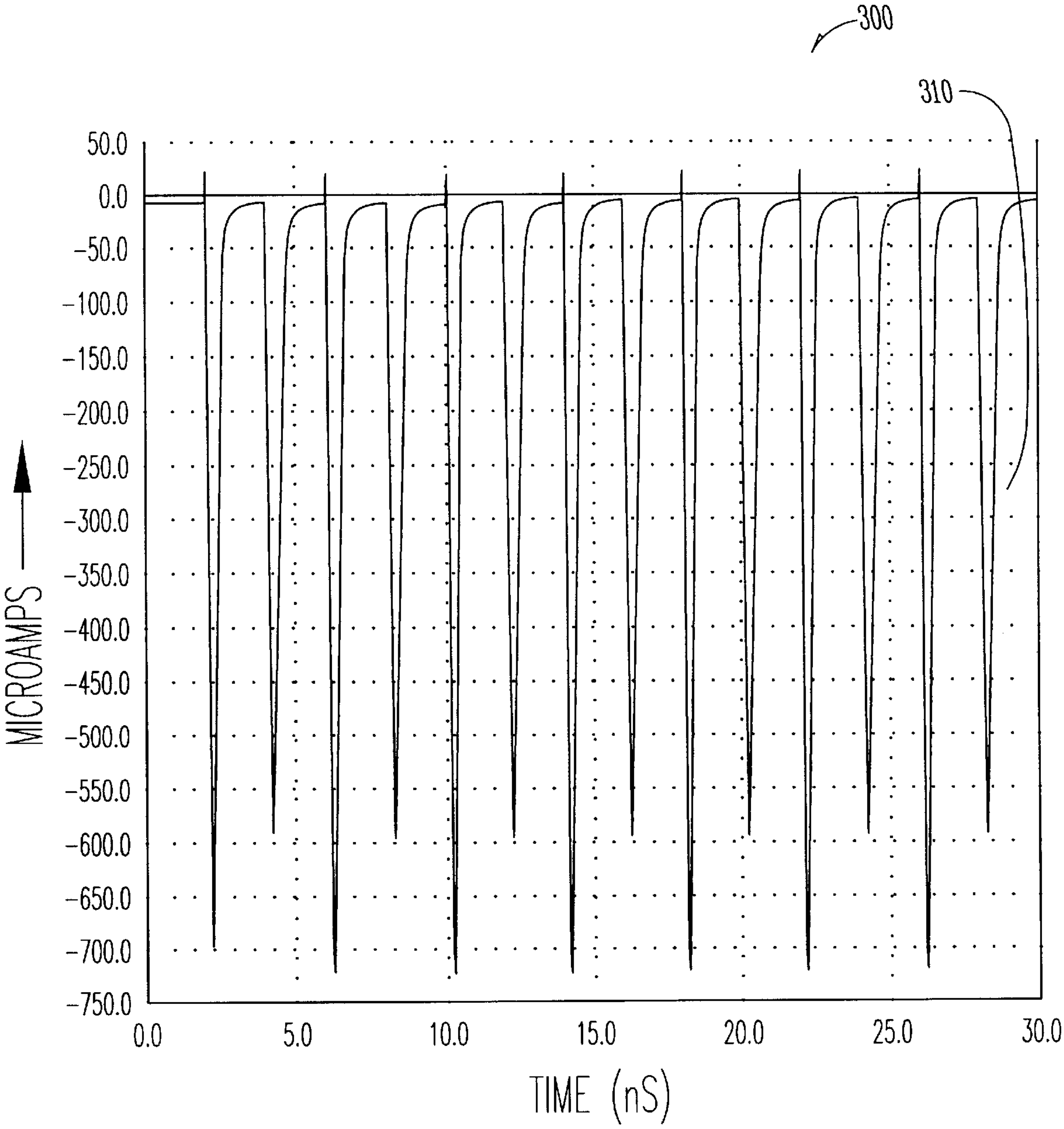
TIME (nS)

Fig.2B


300
310
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-50.0
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-500.0
-550.0
-600.0
-650.0
-700.0
-750.0
MICROAMPS
0.0
5.0
10.0
15.0
20.0
25.0
30.0
TIME (nS)

Fig. 3

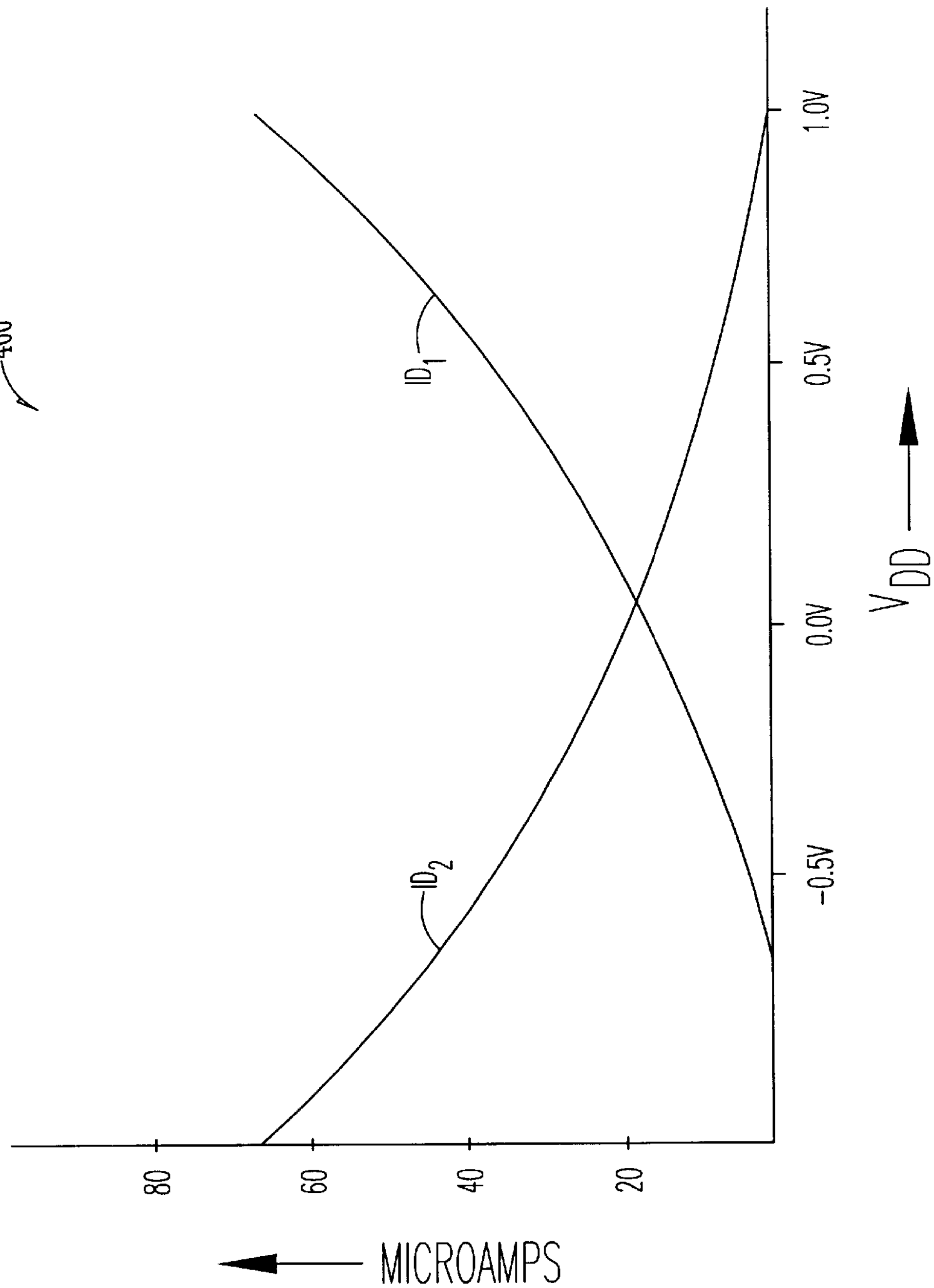


Fig. 4

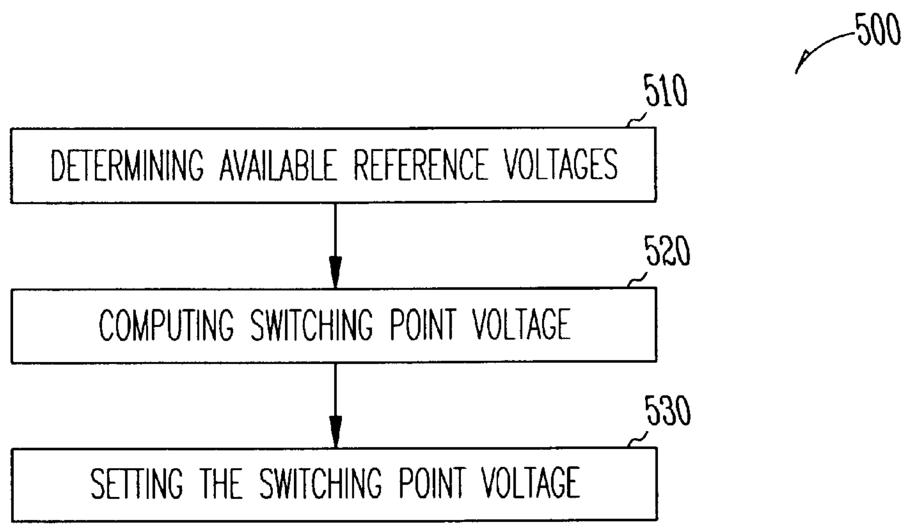

500
510
DETERMINING AVAILABLE REFERENCE VOLTAGES
520
COMPUTING SWITCHING POINT VOLTAGE
530
SETTING THE SWITCHING POINT VOLTAGE

Fig. 5

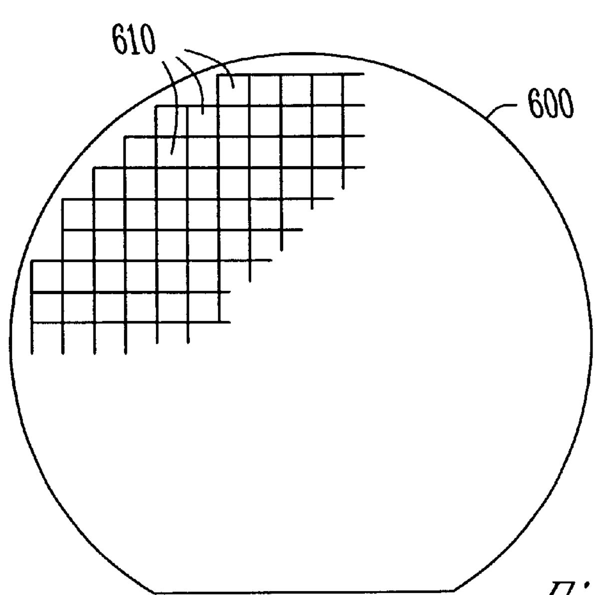

610
600

Fig. 6

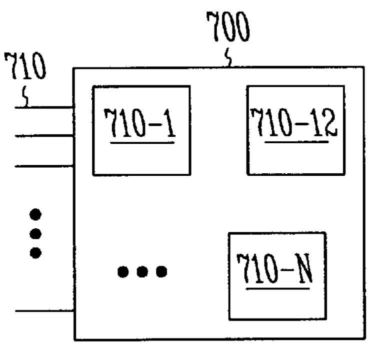


Fig. 7

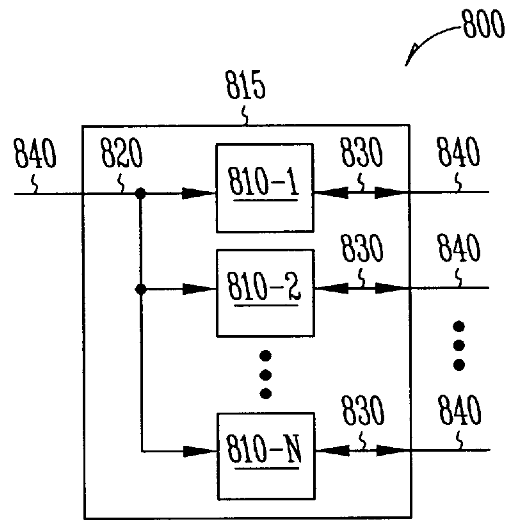


Fig. 8

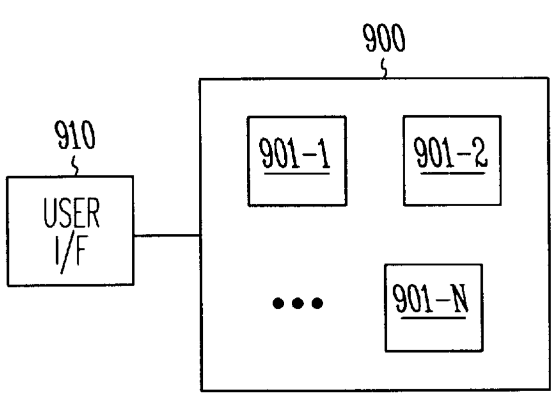
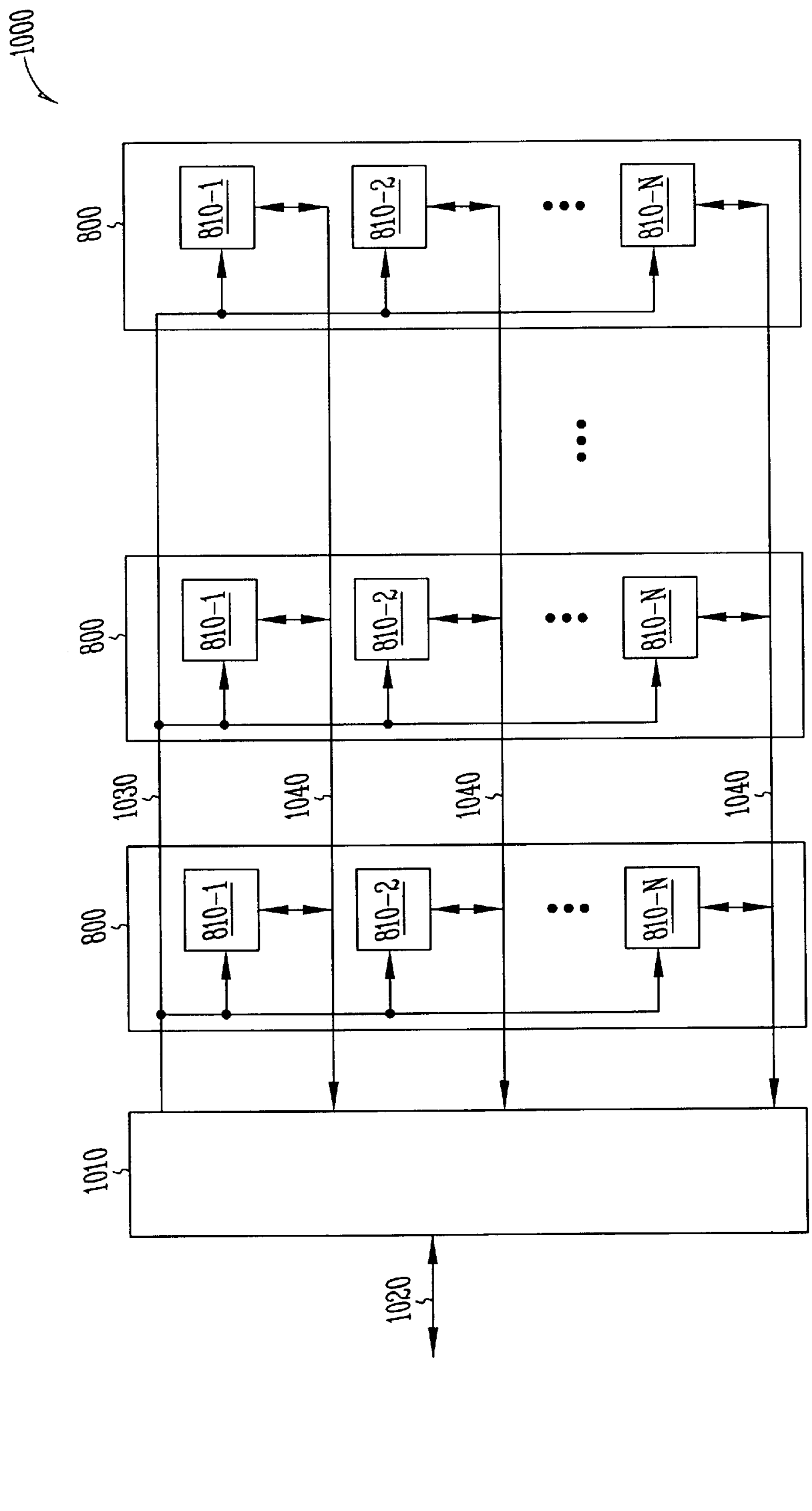


Fig. 9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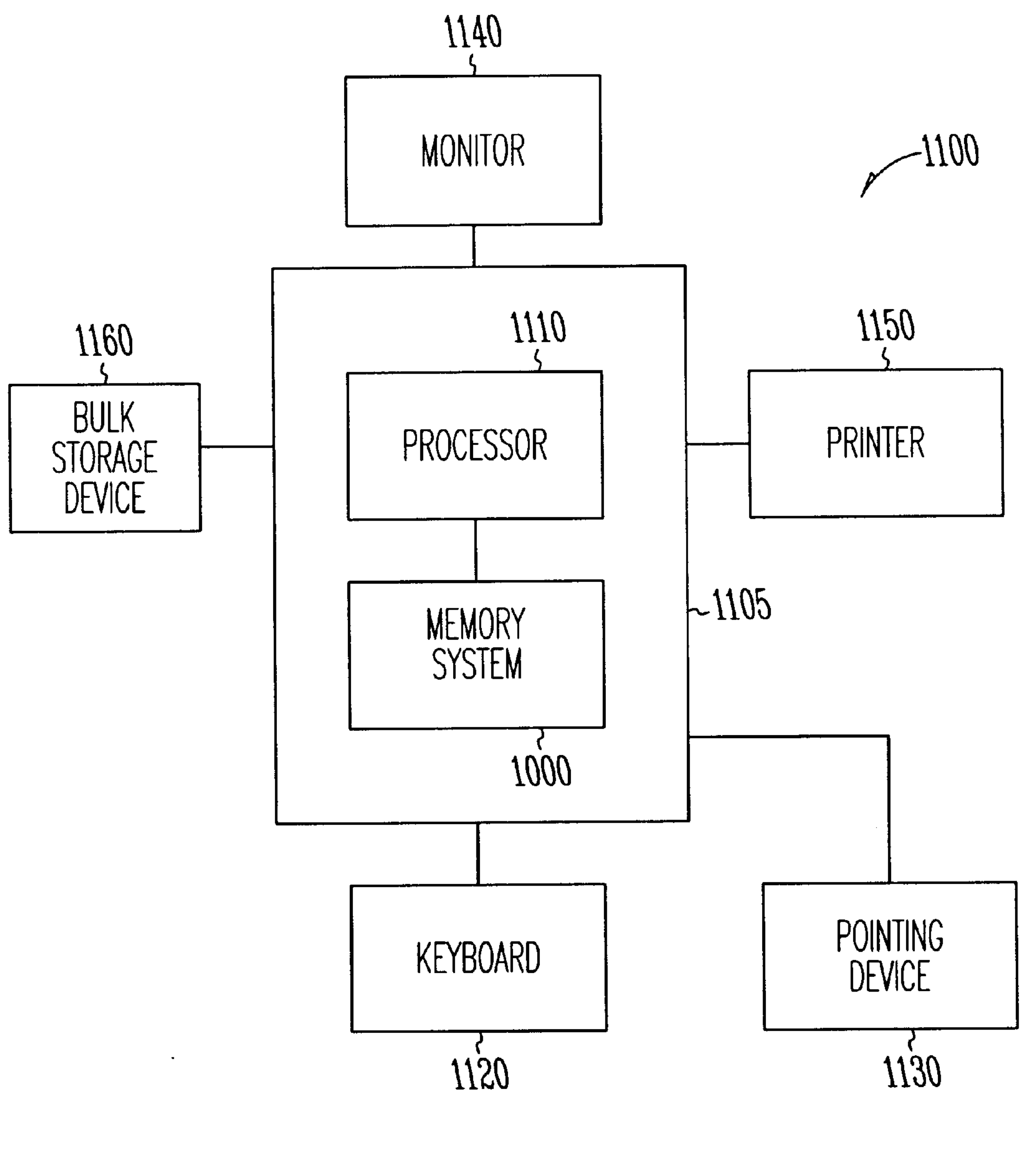
810-2
810-N
800
810-1
810-2
810-N
1030
1040
1040
1040
800
810-1
810-2
810-N
1010
1020

Fig. 10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1100
1160
BULK STORAGE DEVICE
1110
PROCESSOR
1150
PRINTER
MEMORY SYSTEM
1105
1000
KEYBOARD
POINTING DEVICE
1120
1130

Fig. 11

HIGH SPEED LOW POWER INPUT BUFFER

FIELD OF THE INVENTION

The present invention relates generally to integrated circuits. More particularly, it pertains to differential amplifiers including input buffers.

BACKGROUND OF THE INVENTION

Differential amplifiers are commonly used in memory devices as input buffers to couple data signals between a memory array and data terminals of the memory devices. Generally, one common problem with these input buffers is the setting of a switching point voltage to maximize the switching response of the input buffers. Switching point voltage refers to the point at which the input and output voltages are transitioning from a high state-to-low state or a low state-to-high state. If the switching point voltage goes too high, the bits of data coming out of the input buffer will have a good low noise margin, but will not have a high noise margin similarly, if the switching point voltage goes too low, the bits of data will have a good high noise margin, but will not have a good low noise margin. If the switching point voltage is too high or too low, the bits of data coming out of the input buffer can be distorted. For example, if we were to input a voltage in a digital wave form having a sloping rise and fall times like a triangular wave, and if the switching point voltage is too high or too low, the bits of data coming out of the input buffer can be of varying widths and can cause timing problems in the input buffer.

Thus, there is a need for an input buffer that can automatically establish a switching point voltage that maximizes the high and low noise margins of an integrated circuit. There is also a need for input buffers used in memories of computers to transfer data at a faster rate using low power. Therefore, there is also a need for a low power high-speed input buffer that is capable of operating at high speeds, while using low power.

SUMMARY OF THE INVENTION

The input buffer of the present invention provides, among other things, provides a mechanism to accurately establish a switching point voltage that maximizes the high and low noise margins of an integrated circuit, while using a low power. Also the input buffer is capable of operating at high speeds. According to one embodiment, the input buffer has an input stage providing a switching point voltage based on a predetermined switching point set between first and second reference voltages that maximizes the high and low noise margins of the input buffer. The input buffer further includes an output stage. The output stage is coupled to the input stage. The output stage receives the switching point voltage from the input stage and amplifies the switching point voltage to a full logic level voltage.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims and their equivalents. Other aspects of the invention will be apparent on reading the following detailed description of the invention and viewing the drawings that form a part thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram illustrating generally one embodiment of an input buffer of the present invention.

FIG. **2**A is a timing diagram illustrating one embodiment of application of supply voltage to the input buffer circuit of the present invention.

FIG. **2**B is a timing diagram illustrating one embodiment of output voltage obtained from the input buffer circuit of the present invention when the supply voltage to the input buffer circuit is as shown in FIG. **2**A.

FIG. **3** is a timing diagram illustrating one embodiment of a current drawn by the input buffer of the present invention, when operating at 250 Mega Hertz.

FIG. **4** is a graph illustrating one embodiment of current transfer characteristics of the input buffer of the present invention.

FIG. **5** is a flow diagram illustrating a method of providing a switching point voltage from the input buffer of the present invention.

FIG. **6** is an elevation view of one embodiment of a substrate containing semiconductor dies including the input buffer of the present invention.

FIG. **7** is a block diagram of one embodiment of a circuit module including the input buffer of the present invention.

FIG. **8** is a block diagram of one embodiment of a memory module including the input buffer of the present invention.

FIG. **9** is a block diagram of one embodiment of an electronic system formed according to the teachings of the present invention.

FIG. **10** is a block diagram of one embodiment of a memory system including the input buffer of the present invention.

FIG. **11** is a block diagram of one embodiment of a computer system including the input buffer of the present invention.

DESCRIPTION OF THE EMBODIMENTS

In the following detailed description of the invention, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. Moreover, it is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described in one embodiment may be included within other embodiments. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is designed only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The transistors described herein are N-channel metal-oxide-semiconductor (NMOS) and P-channel metal-oxide-semiconductor (PMOS). A metal-oxide-semiconductor (MOS) transistor includes a gate, a first node (drain) and a second node (source). Since a MOS transistor is typically a symmetrical device, the true designation of “source” and “drain” is only possible once voltage is impressed on the terminals. The designations of source and drain herein should be interpreted, therefore, in the broadest sense.

The embodiments of the present invention provide a mechanism to set a predetermined switching point for a switching point voltage which maximizes the high and low noise margins of an integrated circuit. Also the input buffer circuit of the present invention uses low power. This is because the differential amplifier of the present invention behaves like an inverter by drawing current only during switching. The present invention is capable of operating at high speeds to meet the needs of today's computers and computing circuitry which requires a memory that transfers data at a faster rate using low power. High operating speeds are achieved by not having the current source in series with the differential amplifier. Having current source in series with the differential amplifier, causes a slew rate limitation. To overcome the problem of slew rate limitation, the differential amplifier requires a large current source to charge-up quickly the input capacitance of a next stage, which is generally not desirable.

FIG. **1** is a schematic diagram of one embodiment of an integrated circuit according to the teachings of the present invention. In particular, FIG. **1** illustrates an input buffer circuit **100**. The input buffer circuit **100** shown in FIG. **1** includes an input stage **110** and an output stage **120**. The input stage **110** includes a first pair of NMOS and PMOS transistors **130** and **132**, a second pair of NMOS and PMOS transistors **134** and **136**, a third pair of PMOS and NMOS transistors **138** and **140**, and a fourth pair of PMOS and NMOS transistors **142** and **144**. The output stage **120** includes a fifth pair of PMOS and NMOS transistors **150** and **152**, respectively.

Description of Connectivity of the Input Buffer Circuit:

The first pair of NMOS and PMOS transistors **130** and **132** are coupled between a first current source node and a first current sink node **185** and **186**, respectively, in which a drain **159** of the NMOS transistor **130** is coupled to the first current source node **185**, a drain **175** of the PMOS transistor **132** is coupled to the first current sink node **186**. A **161** source of the NMOS transistor **130** is coupled to a source **173** of the PMOS transistor **132**, and a gate **174** of the PMOS transistor **132** is coupled to receive a second reference voltage (V_L).

The second pair of NMOS and PMOS transistors **134** and **136** are coupled between a second current source node **187** and a second current sink node **188**, in which a drain **171** of the NMOS transistor **134** is couple to the second current source node **187**, a drain **191** of the PMOS transistor **136** is coupled to the second current sink node **188**, a source **194** of the NMOS transistor **134** is coupled to a source **189** of the PMOS transistor **136**, a gate **172** of the NMOS transistor **134** is coupled to receive a first reference voltage (V_H), and the gates **160** and **190** of the first pair NMOS transistor **130** and the second pair PMOS transistor **136** are coupled to each other and to a input terminal (V_{DD}) to receive the supply voltage from a power source. V_L and V_H are effectively utilized in the present invention to maximize the switching point voltage.

The third pair of PMOS and NMOS transistors **138** and **140** are coupled between the first current source node **185** and the first current sink node **186**, in which a source **156** of the PMOS transistor **138** is coupled to the first current source node **185**, a drain **158** of the PMOS transistor **138** is coupled to the drain **159** of the first pair NMOS transistor **130**, a drain **176** of the NMOS transistor **140** is coupled to the drain **175** of the first pair PMOS transistor **132**, and a source **178** of the NMOS transistor **140** is coupled to the first current sink node **186**.

The fourth pair of PMOS and NMOS transistors **142** and **144** are coupled between the second current source node **187** and the second current sink node **188**, in which a source **168** of the PMOS transistor **142** is coupled to a second current source node **187**, a drain **170** of the PMOS transistor **142** is coupled to the drain **171** of the second pair NMOS transistor **134**, a gate **169** of the PMOS transistor **142** is coupled to the gate **157** of the third pair PMOS transistor **138** and further the gates **157** and **169** of the third and fourth PMOS transistors **138** and **142** are coupled to the drain **159** of the first pair NMOS transistor **130**, a drain **192** of the NMOS transistor **144** is coupled to the drain **191** of the second pair PMOS transistor **136**, a source **197** of the NMOS transistor **144** is coupled to the second current sink node **188**, a gate **193** of the NMOS transistor **144** is coupled to the gate **177** of the third pair NMOS transistor **140**, the gate **177** of the third PMOS transistor **140** and a gate **193** of the PMOS transistor **144** are coupled to the drain **191** of the second pair PMOS transistor **136**.

The fifth pair of PMOS and NMOS transistors **150** and **152** are coupled between a third current source node **195** and a third current sink node **196**, wherein a source **179** of the PMOS transistor **150** is coupled to the third current source node **195**, a gate **180** of the PMOS transistor **150** is coupled to the drain **171** of the second pair NMOS transistor **134** and further coupled to the drain **170** of the fourth pair PMOS transistor **142**. Further a drain **182** of the NMOS transistor **152** is coupled to a drain **181** of the PMOS transistor **150** and the drain **182** of the NMOS transistor **152** and the drain **181** of the PMOS transistor **150** are coupled to a output terminal (V_{OUT}) to supply and to amplify the switching point voltage to a full logic level voltage, and a gate **183** of the NMOS transistor **152** is coupled to the drain **175** of the first pair PMOS transistor **132** and further coupled to the drain **176** of third pair NMOS transistor **140**.

Description of Operation of the Input Buffer Circuit:

In this example embodiment, the input buffer circuit **100** including the NMOS transistors **130** and **134**, and the PMOS transistors **136** and **132** are switched from a normal CMOS configuration, such that n-channels are on the top and p-channels are on the bottom. In FIG. **1** an input voltage is applied across two gate to source voltages. This input buffer circuit **100** of the present invention is unlike a normal inverter. That is the input buffer circuit **100** of the present invention is different in that an input voltage is applied parallel across the gate to source voltages. Applying the voltages across the gate to source voltages of the transistors provides an immunity from power supply voltage variations.

When the input voltage V_{IN}) to the input buffer circuit **100** goes high (i.e., above the switching point voltage), the gate to source voltage of NMOS transistor **130** increases and source to gate voltage of PMOS transistor **132** increases, this in-turn causes the current to increase in PMOS transistor **138**, NMOS transistor **130**, PMOS transistor **132**, and NMOS transistor **140**. This causes the voltage across the gate of NMOS transistor **152** to increase and the output to go low. Also when the input voltage is high, the source to gate voltage of PMOS transistor **136** and gate to source voltage of NMOS transistor **134** decreases. This causes the current in PMOS transistor **142** and NMOS transistor **144** to go to zero. This will cause the current to go through PMOS transistor **138**, NMOS transistor **130**, and PMOS transistor **132**. This will in-turn cause the current decrease through NMOS transistor **140** and charge-up the gate of NMOS transistor **152**. One of ordinary skill in the art will understand that the opposite occurs when the V_{IN} goes low (i.e., goes below the switching point voltage). Essentially, in operation, the input buffer circuit **100** takes a low level input voltage (such as 100 millivolts peak to peak) and amplifies the input voltage to a full logic level output voltage (V_{OUT}). Also the input buffer circuit **100** of the present invention effectively utilizes the V_L and V_H to maximize the switching point voltage

FIGS. **2**A and **2**B show timing diagrams **200** and **210** illustrating one embodiment of switching point voltage output obtained from the input buffer circuit **100** shown in FIG. **1**. The timing diagram **200** in FIG. **2**A, shows the application of the supply voltage (V_{DD}) to the input buffer circuit **100**. In the embodiment shown in FIG. **2**A, the V_{DD} switches from 0.5 to 1.0 volts, and has a switching point voltage of around 0.75 volts. The timing diagram **210** shown in FIG. **2**B, shows the output voltage V_{OUT}) obtained from the output stage **120** of the input buffer circuit **100** when applying the V_{DD} as shown in the timing diagram **200** of FIG. **2**A. Timing diagrams **200** and **210** clearly show that the input stage and the output stage of the novel input buffer circuit **100** amplifies the V_{DD} and the switching point voltage to a full logic level voltage.

FIG. **3** is a timing diagram **300** illustrating one embodiment of current draw by the input buffer circuit **100** of the present invention **300** when operating at 250 Mega Hertz. The timing diagram **300** shows that the input buffer circuit **100** essentially draws current only during switching. FIG. **3** shows current drawn as spikes **310** during switching and then drawing no current the rest of the time to conserve power. This timing diagram **300** shows that the input buffer circuit **100** of FIG. **1** uses low power by behaving like a conventional inverter and drawing current only during switching. However the novel input buffer circuit **100** of this present invention offers better noise immunity by having a more accurate/effective switching point voltage.

FIG. **4** is a graph **400** illustrating one embodiment of current versus voltage behavior of the input buffer according to the teachings of the present invention. One of ordinary skill in the art will understand that when V_{DD} is applied to the input buffer circuit **100,** the voltage across the first pair of transistors **130** and **132** increases. When the voltage across the first pair of transistors **130** and **132** increases, NMOS transistor **130** and PMOS transistor **132** are turned-on, and PMOS transistor **136** and NMOS transistor **134** are turned-off. This in-turn causes the current ID_1 (represents current drawn across first and third pair of transistors **130, 132** and **138,140** respectively as shown in FIG. **1**) to increase exponentially and current ID_2 (represents current drawn across second and fourth pair of transistors **134, 136** and **142, 144** respectively as shown in FIG. **1**) to decrease exponentially, as shown in FIG. **4**. One of ordinary skill in the art will understand that the opposite occurs when the voltage across the first pair of transistors decreases and the voltage across the second pair of transistors **134** and **136** increases. One of ordinary skill in the art will also understand that in a normal differential amplifier the ID_1 will not increase more than the input current. Where as the input buffer circuit **100** of the present invention operates like a self-biased class AB input, where neither of the output currents ID_1 and ID_2 is zero as long as their magnitude remains less than the current through the fifth pair of PMOS and NMOS transistors **150** and **152**.

FIG. **5** shows a method of providing a switching point voltage using the input buffer circuit **100** of the present invention. Method **500** begins with step **510** by determining available first and second reference voltages (V_H and V_L) to the input buffer circuit **100**. After determining the available V_H and V_L voltages, the next step **520** in the process includes computing a switching point voltage based on the available V_H and V_L voltages to maximize high and low noise margins of the input buffer circuit **100**. In one embodiment, the switching point voltage is computed based on the average of the first and second reference voltages $((V_H+V_L)/2)$. The next step **530** in the process includes setting the switching point voltage by sizing the transistors in the input buffer circuit **100**, to provide the computed switching point voltage. In one embodiment, sizing the transistors in the input buffer circuit **100** includes selecting appropriate reference voltages based on using standard size transistors. In another embodiment, sizing the transistors in the input buffer circuit **100** includes using standard reference voltages V_{DD} and ground. In one embodiment, the first reference voltage is set to V_{DD}. In one embodiment, the second reference voltage is set to zero by coupling the gate of the PMOS transistor **132** of the input stage **110** to ground. In another embodiment, providing a first reference voltage includes using a standard supply voltage V_{DD} and sizing the transistors in the input buffer circuit **100** to obtain a desired switching point voltage.

With reference to FIG. **6**, in one embodiment, a semiconductor die **610** is produced from a silicon wafer **600**. A die is an individual pattern, typically rectangular, on a substrate that contains circuitry to perform a specific function. A semiconductor wafer will typically contain a repeated pattern of such dies containing the same functionality. According to the teaching of the present invention, die **610** contains circuitry for the inventive input buffer, as discussed above. Die **610** may further contain additional circuitry to extend to such complex devices as a monolithic processor with multiple functionality. Die **610** is typically packaged in a protective casing (not shown) with leads extending therefrom (not shown) providing access to the circuitry of the die for unilateral or bilateral communication and control.

As shown in FIG. **7**, two or more dies **710** may be combined, with or without protective casing, into a circuit module **700** to enhance or extend the functionality of an individual die **710-1**. According to the teachings of the present invention at least one of the dies **710-1**, **710-2**, . . . , **710**-N shown in FIG. **7**, includes buffer circuit of the present invention. Circuit module **700** may be a combination of dies **710-1** representing a variety of functions, or a combination of dies **710-1** containing the same functionality. Some examples of a circuit module include input buffer, memory modules, device drivers, power modules, communication modems, processor modules and application-specific modules and may include multi-layer, multi-chip modules. Circuit module **700** may be a sub-component of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft and others. Circuit module **700** will have a variety of leads **710** extending therefrom providing unilateral or bilateral communication and control.

FIG. **8** shows one embodiment of a circuit module as memory module **800**. Memory module **800** generally depicts a Single In-line Memory Module (SIMM) or Dual In-line Memory Module (DIMM). A SIMM or DIMM is generally a printed circuit board (PCB) or other support containing a series of memory devices including input buffer circuit according to the teaching of the present invention. While a SIMM will have a single in-line set of contacts or leads, a DIMM will have a set of leads on each side of the support with each set representing separate I/O signals. Memory module **800** contains multiple memory devices **810-1, 810-2**, . . . , **810**-N contained on support **815**, the number depending upon the desired bus width and the desire for parity. According to the teachings of the present invention, memory module **800** include input buffer circuit of the present invention in a memory device **810-1**, **810-2**, . . . , **810**-N on both sides of support **815**. Memory module **800** accepts a command signal from an external controller (not shown) on a command link **820** and provides for data input and data output on data links **830**. The command link **820** and data links **830** are connected to leads **840** extending from the support **815**. Leads **840** are shown for conceptual purposes and are not limited to the positions shown in FIG. **7**.

FIG. **9** shows an electronic system **900** includes one or more circuit modules **800** as described in FIG. **8**. Electronic system **900** generally contains a user interface **910**. User interface **910** provides a user of the electronic system **900** with some form of control or observation of the results of the electronic system **900**. Some examples of user interface **910** include the keyboard, pointing device, monitor and printer of a personal computer; the tuning dial, display and speakers of a radio; the ignition switch and gas pedal of an automobile; and the card reader, keypad, display and currency dispenser of an automated teller machine. User interface **910** may further describe access ports **901-1**, **901-2**, . . . , **901**-N provided to electronic system **900**. Access ports **901-1**, **901-2**, . . . , **901**-N are used to connect an electronic system **900** to the more tangible user interface components previously exemplified. One or more of the circuit modules **800** includes the input buffer circuit according to the teachings of the present invention. One or more of the circuit modules may be a processor providing some form of manipulation, control or direction of inputs from or outputs to user interface **910**, or of other information either preprogrammed into, or otherwise provided to, electronic system **900**. As will be apparent from the lists of examples previously given, electronic system **900** will often contain certain mechanical components (not shown) in addition to circuit modules **800** including an input buffer circuit according to the teachings of the present invention and user interface **910**. It will be appreciated that the one or more circuit modules **800** in electronic system **900** can be replaced by a single integrated circuit. Furthermore, electronic system **900** may be a subcomponent of a larger electronic system.

FIG. **10** shows one embodiment of an electronic system as memory system **1000**. Memory system **1000** contains one or more memory modules **800** such as memory modules described in connection with FIG. **8**. One or more memory modules **800** includes an input buffer circuit according to the teachings of the present invention and a memory controller **910**. Memory controller **1010** provides and controls a bidirectional interface between memory system **1000** and an external system bus **1020**. Memory system **1000** accepts a command signal from the external bus **1020** and relays it to the one or more memory modules **800** on a command link **1030**. Memory system **1000** provides for data input and data output between the one or more memory modules **800** and external system bus **1020** on data links **1040**.

FIG. **11** shows a further embodiment of an electronic system as a computer system **1100**. Computer system **1100** contains a processor **1110** and a memory system **1000** housed in a computer unit **1105**. Computer system **1100** is but one example of an electronic system containing another electronic system, i.e. memory system **1000**, as a subcomponent. Computer system **1100** optionally contains user interface components. Depicted in FIG. **11** are a keyboard **1120**, a pointing device **1130**, a monitor **1140**, a printer **1150** and a bulk storage device **1160**. It will be appreciated that other components are often associated with computer system **1100** such as modems, device driver cards, additional storage devices, etc. It will further be appreciated that the processor **1110** and memory system **1000** can include the input buffer circuit according to the teachings of the present invention. Computer system **1100** can be incorporated on a single integrated circuit. Such single package processing units reduce the communication time between the processor and the memory circuit.

CONCLUSION

An input buffer circuit is described which conveniently allows setting any predetermined switching point voltage to provide a switching point voltage that maximizes high and low noise margins of an integrated circuit. The input buffer of the present invention is capable of operating at high speeds while using low power. The input buffer circuit is self-biasing and automatically adjusts to process variations. In one embodiment, the input buffer has an input stage providing a switching point voltage based on a predetermined switching point set between a first and second reference voltages that maximizes the high and low noise margins of the input buffer. The input stage is further coupled to an output stage. The output stage receives the switching point voltage from the input stage and amplifies the switching point voltage to a full logic level voltage.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. An integrated circuit, comprising:

a power source, to provide a supply voltage;

a first voltage source, to provide a first reference voltage;

a second voltage source, to provide a second reference voltage; and

an input stage, coupled to receive the supply voltage, and the first and second reference voltages and including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages.

2. The integrated circuit of claim **1**, further comprising an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, and to amplify the switching point voltage to a full logic level voltage.

3. The integrated circuit of claim **2**, wherein the predetermined switching point set between the first and second reference voltages, comprises a switching point that maximizes high and low noise margins of the integrated circuit.

4. The integrated circuit of claim **2**, wherein the predetermined switching point voltage is computed using the first and second reference voltages.

5. The integrated circuit of claim **2**, wherein the input stage is an input differential amplifier.

6. An integrated circuit, comprising:

a power source, to provide a supply voltage;

a first voltage source, to provide a first reference voltage;

a second voltage source, to provide a second reference voltage;

an input stage, coupled to receive the, and the first and second reference voltages, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages;

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, and to amplify the switching point voltage to a full logic level voltage;

wherein the input stage comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

7. The integrated circuit of claim **6**, wherein the output stage acts as an inverter.

8. The integrated circuit of claim **7**, wherein the first reference voltage is equal to the supply voltage.

9. The integrated circuit of claim **7**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

10. The integrated circuit of claim **7**, wherein the drain of the first pair PMOS transistor is coupled to ground.

11. An integrated circuit, comprising:

a power source, to provide a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the supply voltage, and the first and second reference voltages including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage between the first and second reference voltages that maximizes high and low noise margins of the integrated circuit; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage and to amplify the switching point voltage to a full logic level voltage.

12. The integrated circuit of claim **11**, wherein the switching point voltage is based on an average of the first and second reference voltages.

13. An integrated circuit, comprising:

a power source, to provide a supply voltage;

a first voltage source wherein the first voltage source provides a first reference voltage;

a second voltage source wherein the second voltage source provides a second reference voltage;

an input stage to provide a switching point voltage between the first and second reference voltages that maximizes high and low noise margins of the integrated circuit;

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage and to amplify the switching point voltage to a full logic level voltage,

wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

14. The integrated circuit of claim **13**, wherein the output stage is an inverter.

15. The integrated circuit of claim **13**, wherein the first reference voltage is equal to the supply voltage.

16. The integrated circuit of claim **13**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

17. The integrated circuit of claim **13**, wherein the drain of the first pair PMOS transistor is coupled to ground.

18. An input buffer circuit, comprising:

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the first and second reference voltages including cross-coupled pairs of transistors coupled to a supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage between a first and second reference voltages that maximizes high and low noise margins of the input buffer circuit; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage and to amplify the switching point voltage to a full logic level voltage.

19. The input buffer circuit of claim **18**, wherein the switching point voltage is based on an average of the first and second reference voltages.

20. An input buffer circuit, comprising:

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the first and second reference voltages, to provide a switching point voltage between the first and second reference voltages that maximizes high and low noise margins of the input buffer circuit; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage and to amplify the switching point voltage to a full logic level voltage,

wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

21. The integrated circuit of claim **20**, wherein the output stage is an inverter.

22. The integrated circuit of claim **20**, wherein the first reference voltage is equal to the supply voltage.

23. The integrated circuit of claim **20**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

24. The integrated circuit of claim **20**, wherein the drain of the first pair PMOS transistor is coupled to ground.

25. A cross-coupled differential input buffer, comprising:

first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input differential amplifier, coupled to receive the first and second reference voltages including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage between the first and second reference voltages that maximizes high and low noise margins of the cross-coupled differential input buffer; and

an inverter, coupled to the input stage, to receive the switching point voltage from the input stage and to amplify the switching point voltage to a full logic level voltage.

26. The cross-coupled differential input buffer of claim **25**, wherein the switching point voltage is based on an average of the first and second reference voltages.

27. A cross-coupled differential input buffer, comprising:

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input differential amplifier, coupled to receive the first and second reference voltages, to provide a switching point voltage between the first and second reference voltages that maximizes high and low noise margins of the cross-coupled differential input buffer; and

an inverter, coupled to the input stage, to receive the switching point voltage from the input stage and to amplify the switching point voltage to a full logic level voltage,

wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

28. The cross-coupled differential input buffer of claim **27**, wherein the output stage acts as an inverter.

29. The cross-coupled differential input buffer of claim **27**, wherein the first reference voltage is equal to the supply voltage.

30. The cross-coupled differential input buffer of claim **27**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

31. The cross-coupled differential input buffer of claim **27**, wherein the drain of the first pair PMOS transistor is coupled to ground.

32. A memory device including an input buffer, wherein the input buffer comprising:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the supply voltage, and the first and second reference voltages including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory device; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, to amplify the switching point voltage to a full logic level voltage.

33. The memory device of claim **32**, wherein the switching point voltage is based on an average of the first and second reference voltages.

34. A memory device including an input buffer, wherein the input buffer comprising:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the supply voltage, and the first and second reference voltages, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory device; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, to amplify the switching point voltage to a full logic level voltage, wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

35. The memory device of claim **34**, wherein the output stage is an inverter.

36. The memory device of claim **34**, wherein the first reference voltage is equal to the supply voltage.

37. The memory device of claim **34**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

38. The memory device of claim **34**, wherein the drain of the first pair PMOS transistor is coupled to ground.

39. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device includes an input buffer, and wherein the input buffer comprises:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the supply voltage, and the first and second reference voltages, including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory device; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, to amplify the switching point voltage to a full logic level voltage.

40. The semiconductor die of claim **39**, wherein the switching point voltage is based on an average of the first and second reference voltages.

41. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device includes an input buffer, and wherein the input buffer comprises:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the, and the first and second reference voltages, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory device; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, to amplify the switching point voltage to a full logic level voltage,

wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

42. The semiconductor die of claim **41**, wherein the output stage is an inverter.

43. The semiconductor die of claim **41**, wherein the first reference voltage is equal to the supply voltage.

44. The semiconductor die of claim **41**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

45. The integrated circuit of claim **41**, wherein the drain of the first pair PMOS transistor is coupled to ground.

46. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link includes an input buffer, and wherein the input buffer comprises:

a first voltage source, wherein the first voltage source provides a first reference voltage; a second voltage source, wherein the second voltage source provides a second reference voltage; and

an input stage, coupled to receive the supply voltage, and the first and second reference voltages including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory system.

47. The memory system of claim 46, further comprising an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, and to amplify the switching point voltage to a full logic level voltage.

48. The memory system of claim 47, wherein the predetermined switching point set between the first and second reference voltages, comprises a switching point that maximizes high and low noise margins of the integrated circuit.

49. The memory system of claim 47, wherein the predetermined switching point voltage is computed based on an average of the first and second reference voltages.

50. The memory system of claim 47, wherein the input stage is an input differential amplifier.

51. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link includes an input buffer, and wherein the input buffer comprises:

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the, and the first and second reference voltages, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory system; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, and to amplify the switching point voltage to a full logic level voltage,

wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

52. The memory system of claim 51, wherein the output stage is an inverter.

53. The memory system of claim 51, wherein the first reference voltage is equal to the supply voltage.

54. The memory system of claim 51, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

55. The integrated circuit of claim 51, wherein the drain of the first pair PMOS transistor is coupled to ground.

56. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link includes an input buffer, and wherein the input buffer comprises:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the supply voltage, and the first and second reference voltages , and including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory system; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, to amplify the switching point voltage to a full logic level voltage.

57. The memory system of claim **56**, wherein the predetermined switching point set between the first and second reference voltages, comprises a switching point that maximizes high and low noise margins of the integrated circuit.

58. The memory system of claim **56**, wherein the predetermined switching point voltage is computed based on an average of the first and second reference voltages.

59. The memory system of claim **56**, wherein the input stage is an input differential amplifier.

60. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link includes an input buffer, and wherein the input buffer comprises:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the supply voltage, and the first and second reference voltages, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the memory system; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, to amplify the switching point voltage to a full logic level voltage,

wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

61. The memory system of claim **60**, wherein the output stage is an inverter.

62. The memory system of claim **60**, wherein the first reference voltage is equal to the supply voltage.

63. The memory system of claim **60**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

64. The memory system of claim **60**, wherein the drain of the first pair PMOS transistor is coupled to ground.

65. An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device includes an input buffer, and wherein the input buffer comprises:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage; and

an input stage, coupled to receive the supply voltage, and the first and second reference voltages and including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages to maximize high and low noise margins of the electronic system.

66. The electronic system of claim **65**, further comprising an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, and to amplify the switching point voltage to a full logic level voltage.

67. The electronic system of claim **66**, wherein the predetermined switching point set between the first and second reference voltages, comprises a switching point that maximizes high and low noise margins of the integrated circuit.

68. The electronic system of claim **66**, wherein the predetermined switching point voltage is computed based on an average of the first and second reference voltages.

69. The electronic system of claim **66**, wherein the input stage is an input differential amplifier.

70. An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device includes an input buffer, and wherein the input buffer comprises:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage; and

an input stage, coupled to receive the supply voltage, and the first and second reference voltages, to provide a switching point voltage based on a predetermined

switching point set between the first and second reference voltages to maximize high and

low noise margins of the electronic system; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, and to amplify the switching point voltage to a full logic level voltage,

wherein the input stage further comprises a first pair of NMOS and PMOS transistors coupled between a first current source node and a first current sink node, in which a drain of the NMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the first current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, and a gate of the PMOS transistor is coupled to receive the second reference voltage;

a second pair of NMOS and PMOS transistors coupled between a second current source node and a second current sink node, in which a drain of the NMOS transistor is couple to the second current source node, a drain of the PMOS transistor coupled to the second current sink node, a source of the NMOS transistor coupled to a source of the PMOS transistor, a gate of the NMOS transistor coupled to receive the first reference voltage, and the gates of the first pair NMOS transistor and the second pair PMOS transistor are coupled to each other and to a input terminal to receive the supply voltage from the power source;

a third pair of PMOS and NMOS transistors coupled between the first current source node and the first current sink node, in which a source of the PMOS transistor is coupled to the first current source node, a drain of the PMOS transistor coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the first pair PMOS transistor, and a source of the NMOS transistor coupled to the first current sink node; and

a fourth pair of PMOS and NMOS transistors coupled between the second current source node and the second current sink node, in which a source of the PMOS transistor is coupled to a second current source node, a drain of the PMOS transistor coupled to the drain of the second pair NMOS transistor, a gate of the PMOS transistor coupled to the gate of the third pair PMOS transistor and further the gates of the third and fourth PMOS transistors coupled to the drain of the first pair NMOS transistor, a drain of the NMOS transistor coupled to the drain of the second pair PMOS transistor, a source of the NMOS transistor coupled to the second current sink node, a gate of the NMOS transistor is coupled to the gate of the third pair NMOS transistor, the gate of the third PMOS transistor and a gate of the PMOS transistor are coupled to the drain of the second pair PMOS transistor.

71. The electronic system of claim **70**, wherein the output stage is an inverter.

72. The electronic system of claim **70**, wherein the first reference voltage is equal to the supply voltage.

73. The electronic system of claim **70**, wherein the output stage further comprises:

a fifth pair of PMOS and NMOS transistors coupled between a third current source node and a third current sink node, wherein a source of the PMOS transistor is coupled to the third current source node, a gate of the PMOS transistor coupled to the drain of the second pair NMOS transistor and further coupled to the drain of the fourth pair PMOS transistor, a drain of the NMOS transistor coupled to a drain of the PMOS transistor and further the drain of the NMOS transistor and the drain of the PMOS transistor coupled to a output terminal, wherein the output stage amplifies the switching point voltage to a full logic level voltage, and a gate of the NMOS transistor coupled to the drain of the first pair NMOS transistor and further coupled to the drain of third pair NMOS transistor.

74. The electronic system of claim **70**, wherein the drain of the first pair PMOS transistor is coupled to ground.

75. An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory includes an input buffer, and wherein the input buffer comprises:

a power source, wherein the power source provides a supply voltage;

a first voltage source, wherein the first voltage source provides a first reference voltage;

a second voltage source, wherein the second voltage source provides a second reference voltage;

an input stage, coupled to receive the supply voltage, and the first and second reference voltages and including cross-coupled pairs of transistors coupled to the supply voltage, and the first and second reference voltages such that the supply voltage is applied across the gate to source voltages of the pairs of transistors, to provide a switching point voltage based on a predetermined switching point set between the first and second reference voltages that maximizes high and low noise margins of the electronic system; and

an output stage, coupled to the input stage, to receive the switching point voltage from the input stage, to amplify the switching point voltage to a full logic level voltage.

76. The electronic system of claim **75**, wherein the predetermined switching point set between the first and second reference voltages, comprises a switching point that maximizes high and low noise margins of the integrated circuit.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,407,588 B1 Page 1 of 1
DATED : June 18, 2002
INVENTOR(S) : Baker

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

<u>Column 4,</u>
Line 49, delete "V_{IN})" and insert -- (V_{IN}) --, therefor.

<u>Column 5,</u>
Line 6, after "voltage" insert -- . --.
Line 15, delete "V_{OUT})" and insert -- (V_{OUT}) --, therefor.

<u>Column 13,</u>
Line 33, before "first" insert -- a --.

<u>Column 16,</u>
Line 49, delete "a" and insert -- an --, therefor.

<u>Column 18,</u>
Line 39, delete "a" and insert -- an --, therefor.

<u>Column 24,</u>
Line 27, delete "a" and insert -- an --, therefor.
Line 61, delete "76. The electronic system of claim 75, wherein the predetermined switching point set between the first and second reference voltages, comprises a switching point that maximizes high and low noise margins of the integrated circuit.".

Signed and Sealed this

Eighteenth Day of March, 2003

JAMES E. ROGAN
Director of the United States Patent and Trademark Office