US006069506A

United States Patent [19]

Miller, Jr. et al.

[11] **Patent Number:** **6,069,506**

[45] **Date of Patent:** **May 30, 2000**

[54] **METHOD AND APPARATUS FOR IMPROVING THE PERFORMANCE OF DIGITAL DELAY LOCKED LOOP CIRCUITS**

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[21] Appl. No.: **09/081,774**

[22] Filed: **May 20, 1998**

[51] **Int. Cl.⁷** .... $H03L\ 7/06$

[52] **U.S. Cl.** **327/156**; 327/158; 327/276; 327/284; 377/54

[58] **Field of Search** 327/263, 269, 327/270, 272, 276, 277, 278, 284, 147, 149, 150, 156, 158, 159; 377/54, 56, 76

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[57] **ABSTRACT**

A method and apparatus for improving the performance and accuracy of a digital delay locked loop (DDLL) by using a unique correction latch and novel reset mechanism circuit for eliminating DDLL minimum and maximum delay states of inoperability. The accuracy of a DDLL is further improved by the use of a three-NAND gate logic delay element design. A DDLL according to the present invention provides symmetrical rising and falling edges of the signal at the output of each delay line element. A DDLL according to the present invention further ensures insensitivity to random values upon initialization. In addition, a DDLL according to the present invention has increased accuracy due to ensuring a comparison between the actual, not divided-down, input signal and an output signal during a phase detect operation.
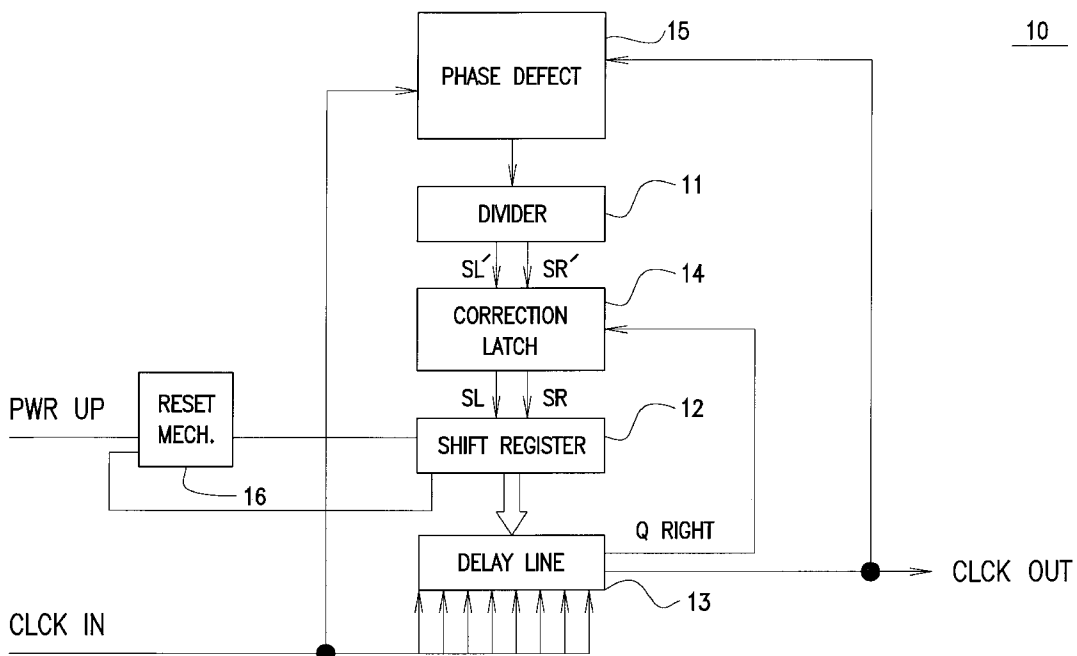
50 Claims, 7 Drawing Sheets
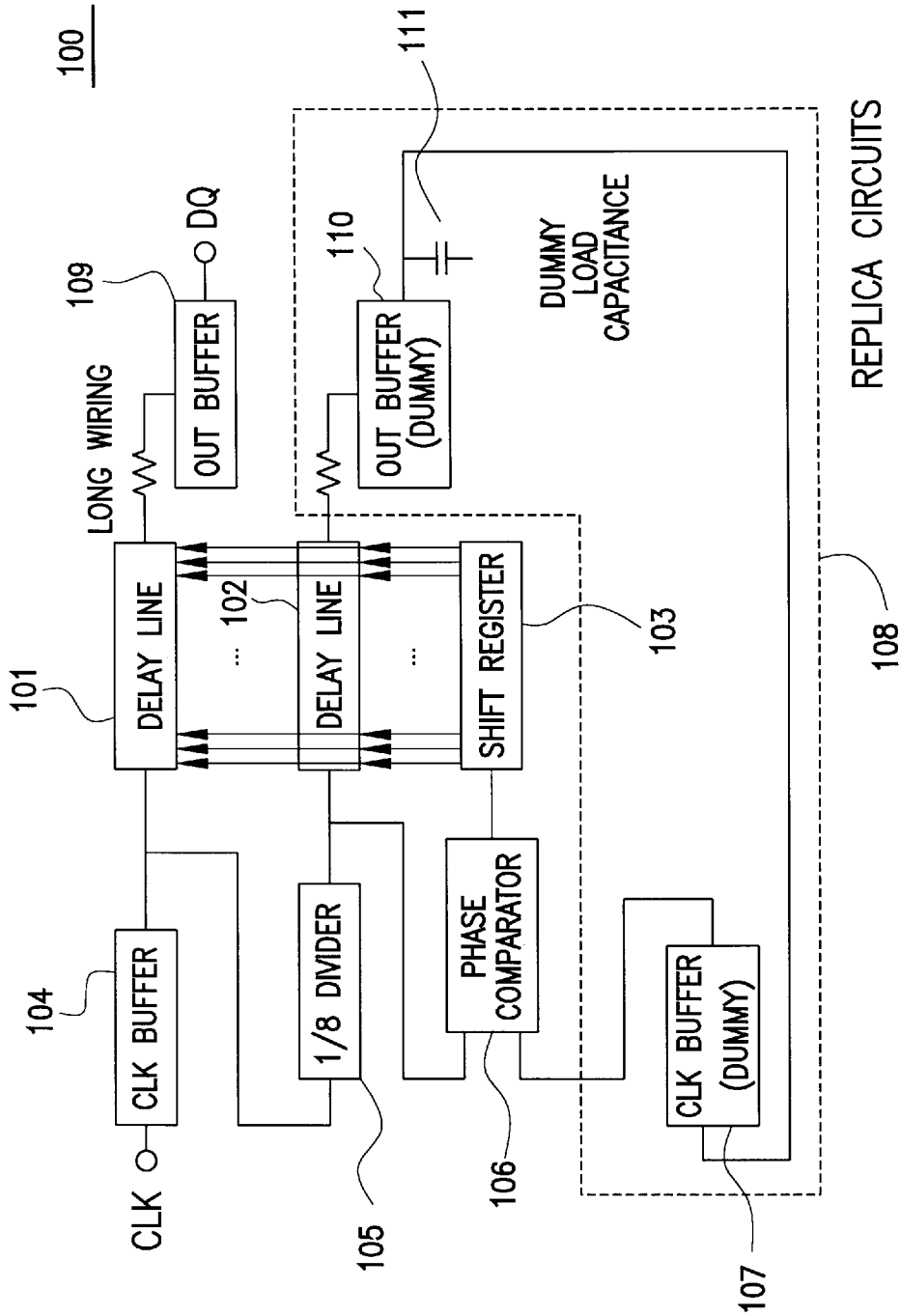
FIG. 1

PRIOR ART

FIG. 2A
PRIOR ART
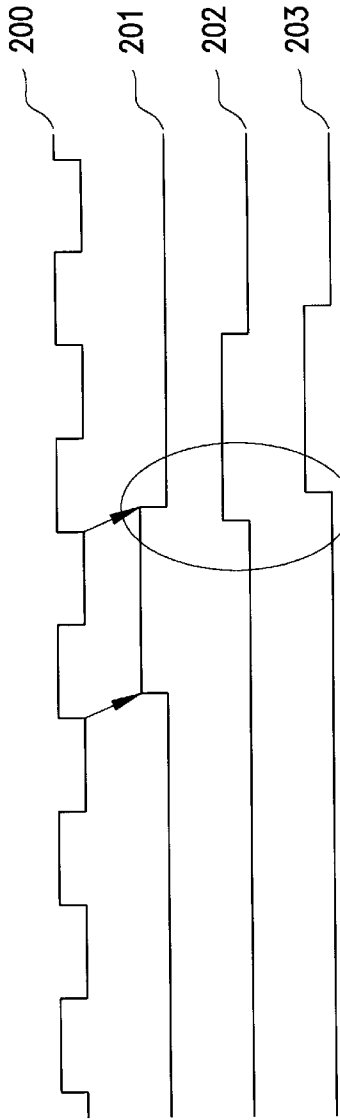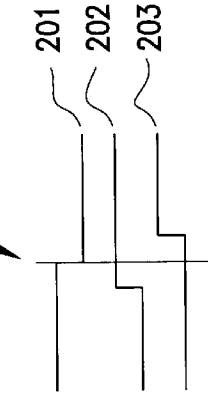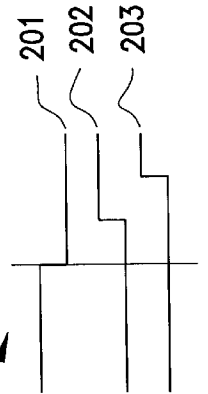
FIG. 2B
PRIOR ART

FAST, SHIFT LEFT

FIG. 2C
PRIOR ART

ADJUSTED

FIG. 2D
PRIOR ART

SLOW, SHIFT RIGHT

FIG. 3

FIG. 4

(a)

FIG. 5

n

DELAY ELEMENT

13

PRECEDING
DELAY ELEMENT
OUTPUT

32

31

33

OUTPUT

CLCK IN

n−3 n−2 n−1   Q   Q̄   n+1 n+2 n+3 n+4

| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 12 |

SHIFT REGISTER

n−3 n−2 n−1   n   n+1 n+2 n+3 n+4
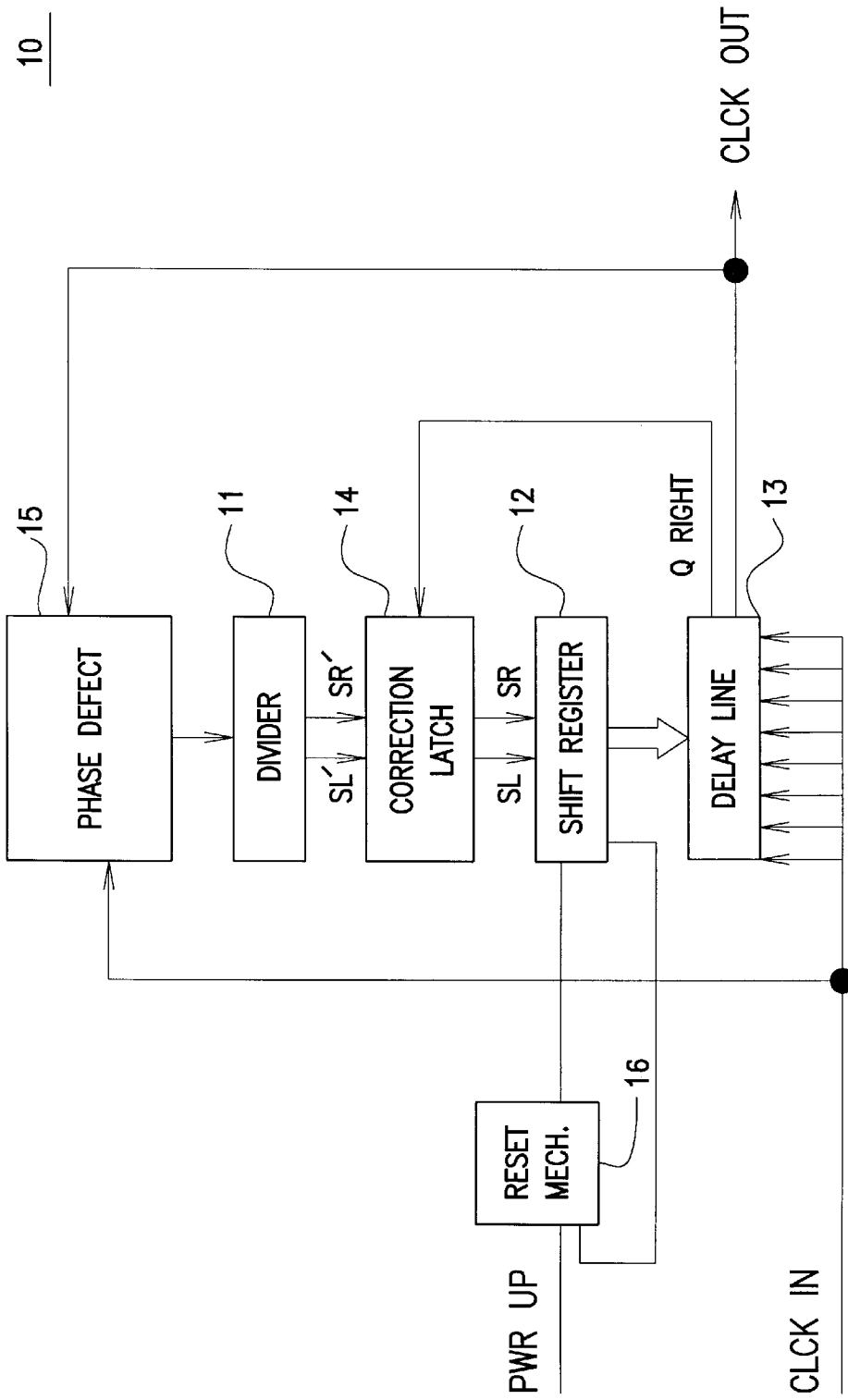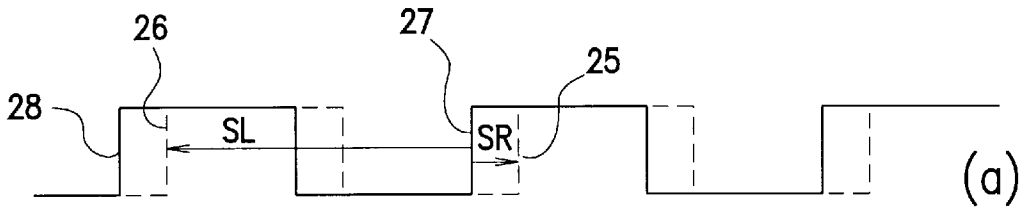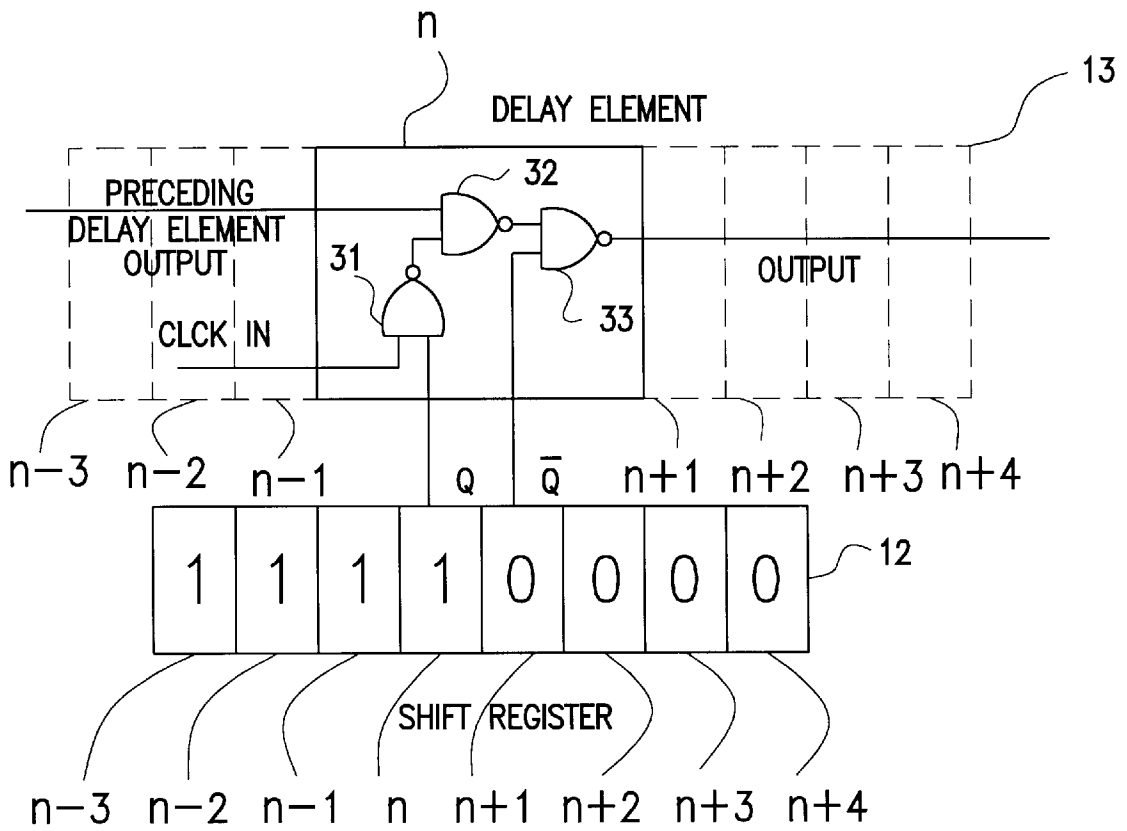
FIG. 6
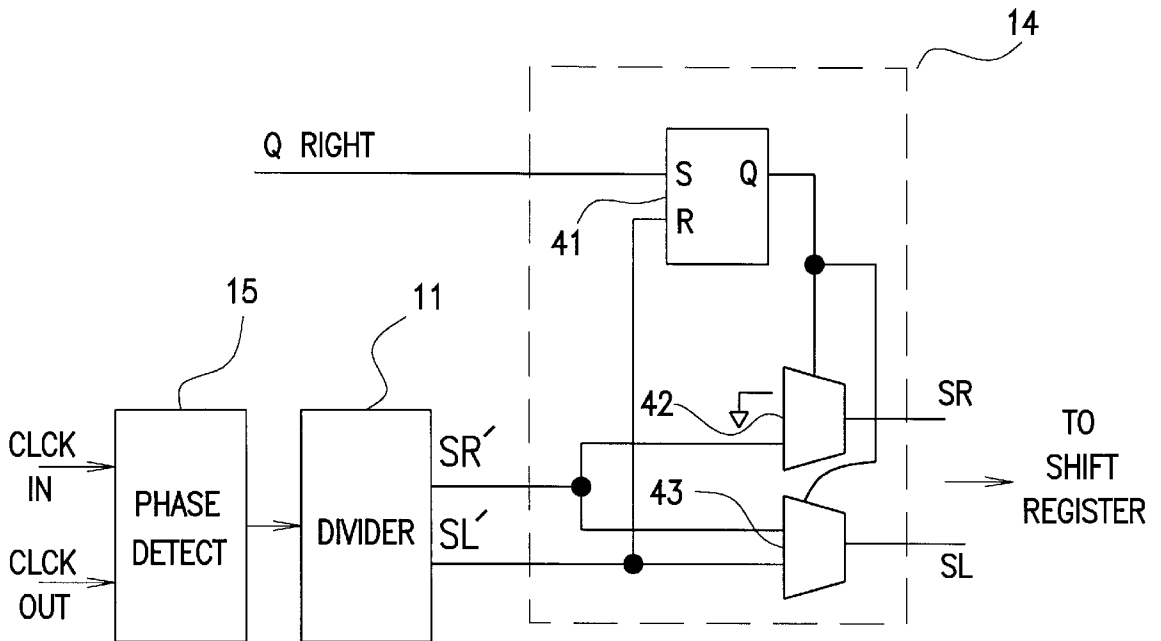
FIG. 7

DDLL STATE / LATCH	SR	SL
NOT MIN DELAY NOT LATCHED	SR = SR	SL = SL
NOT MIN DELAY LATCHED	SR = 0	SL = SR
MIN DELAY SET LATCH	SR = 0	SL = SR
NOT MIN DELAY LATCHED SL´ HAPPENS (RESET LATCH)	SR = SR	SL = SL

FIG. 8

PRIOR ART

SELECT

DELAY LINE

51

OUTPUT

INPUT

52

L L H L L

50

SHIFT REGISTER

FIG. 9A

Δt_1 Δt_2

$\Delta t_1 \neq \Delta t_2$

FIG. 9B

$\Delta t_1'$ $\Delta t_2'$

$\Delta t_1' \approx \Delta t_2'$
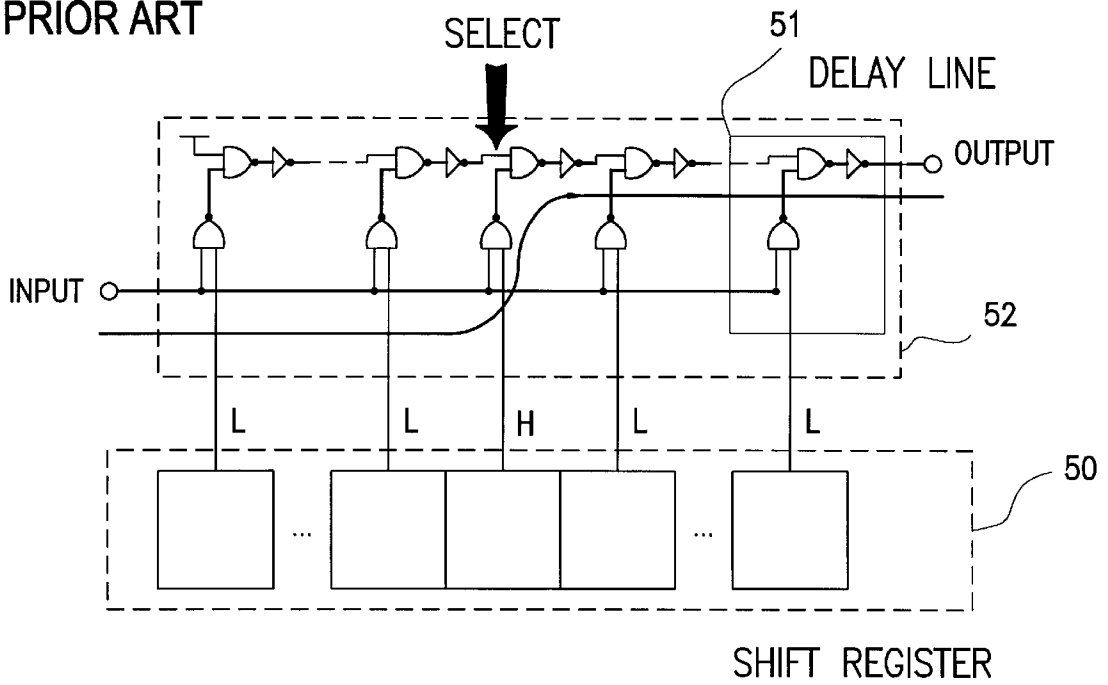
FIG. 10

FIG. 11

METHOD AND APPARATUS FOR IMPROVING THE PERFORMANCE OF DIGITAL DELAY LOCKED LOOP CIRCUITS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to circuitry for generation of periodic signals such as clock signals. More specifically, the present invention relates to digital delay locked loop circuits (DDLLs) having improved stability and performance.

2. Discussion of Related Art

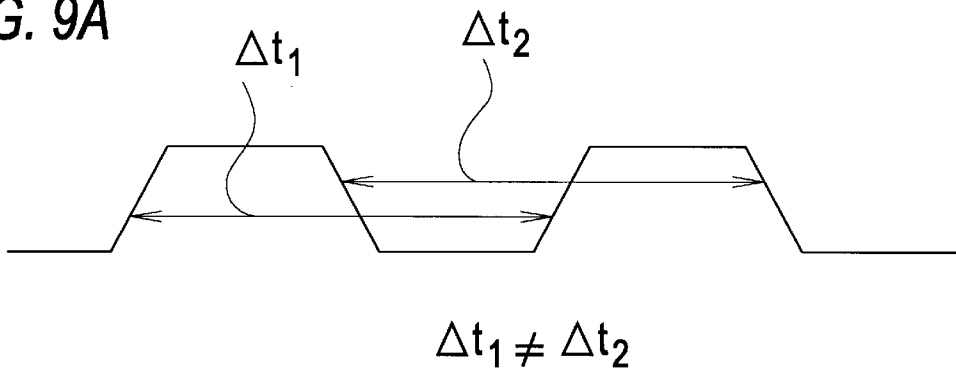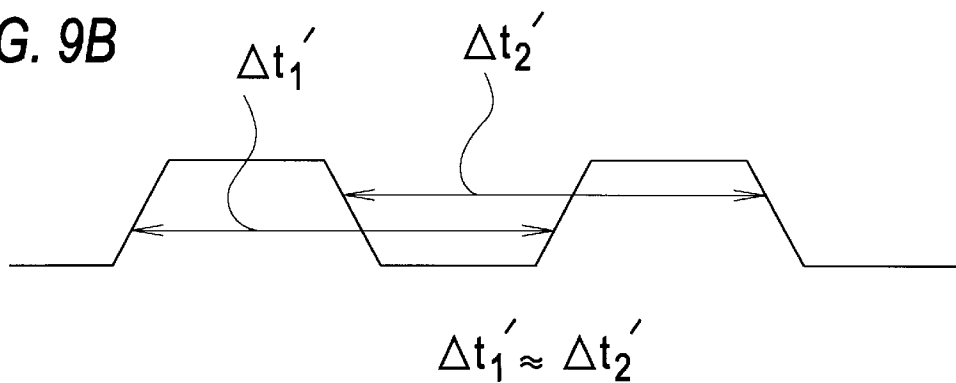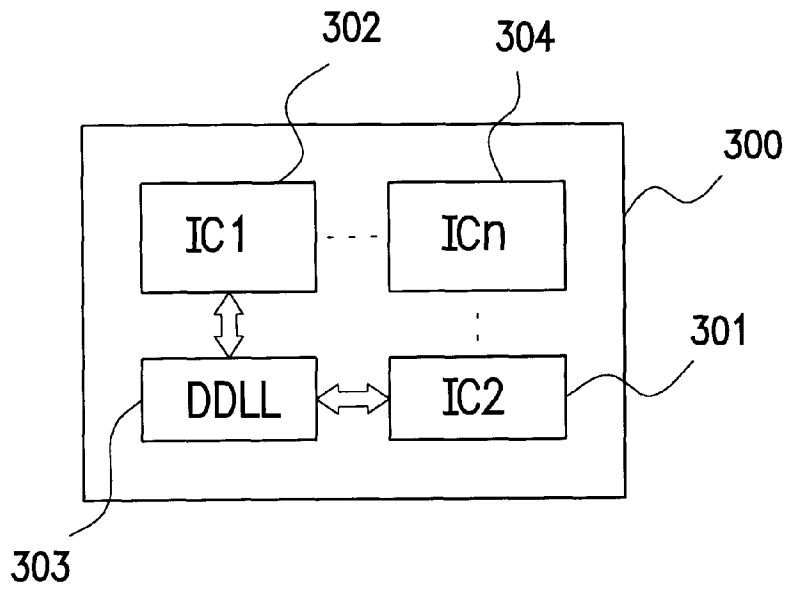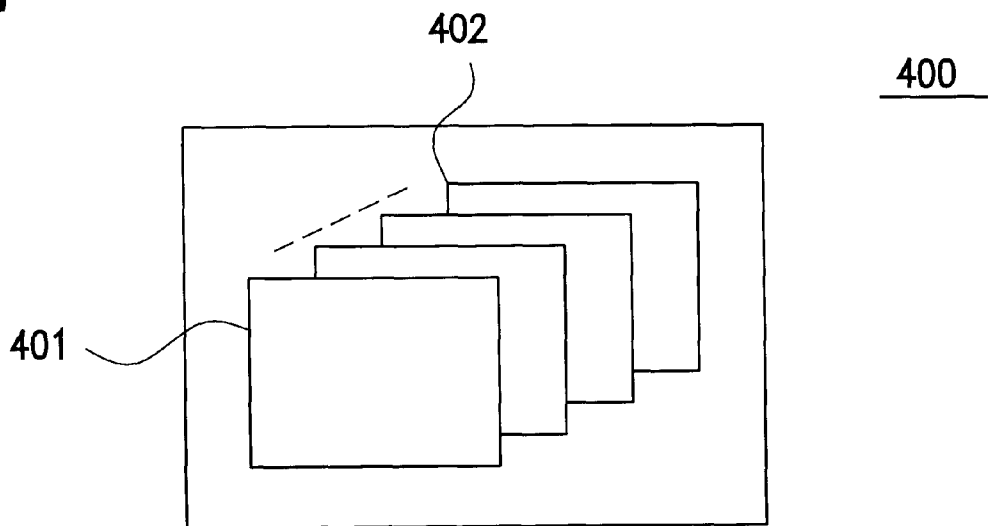Many high speed electronic systems possess critical timing requirements which dictate the need to generate a periodic clock wave form that possesses a precise time relationship with respect to some reference signal. The improved performance of computing integrated circuits (ICs) and the growing trend to include several computing devices on the same board present a challenge with respect to synchronizing the time frames of all the components.

While the operation of all components in the system should be highly synchronized, i.e., the maximum skew or difference in time between the significant edges of the internally generated clocks of all the components should be minute, it is not enough to feed the reference clock of the system to all the components. This is because different chips may have different manufacturing parameters which, when taken together with additional factors such as ambient temperature, voltage, and processing variations, may lead to large differences in the phases of the respective chip generated clocks.

Conventionally, synchronization is achieved by using DDLL circuits to detect the phase difference between clock signals of the same frequency and produce a digital signal related to the phase difference. By feeding back the phase difference-related signal to control a delay line, the timing of one clock signal is advanced or delayed until its rising edge is coincident with the rising edge of a second clock signal.

The operation of conventional DDLLs is shown in FIGS. 1 and 2. In FIG. 1, clock input buffer 104, delay lines 101, 102, and data output buffer 109 constitute an internal clock path. Delay line 101 is a variable delay generator with a logic-gate chain. A second delay line 102 is connected to replica circuits 108, which emulate the internal clock path components. Replica circuits 108 include dummy output buffer 110, with dummy load capacitance 111 and dummy clock buffer 107. The dummy components and second delay line 102 constitute a dummy clock path having exactly the same delay time as the internal clock path. Shift register 103 is used for activating a number of delay elements in both delay lines based on a command generated by phase comparator 106.

Phase comparator 106 compares the dummy clock and the external clock phases which differ by one cycle. This comparison is illustrated in FIGS. 2A, 2B, 2C, and 2D. External clock signal 200 is divided down in divider 105 to produce divided-down external signal 201. Signal 202 is the signal at the output of dummy delay line 102. Signal 203, which is generated inside phase comparator 106, is a one delay unit delayed output dummy line signal 202. If both signals 202 and 203 go high before 201 goes low, this means that the output clock is too fast and phase comparator 106 outputs a shift left (SL) command to shift register 103, as illustrated in FIG. 2B. Shift register 103 shifts the tap point of delay lines 102 and 101 by one step to the left, increasing the delay. Conversely, if both signals 202 and 203 go high

after 201 goes low, this means that the output clock is too slow and phase comparator 106 outputs a shift right (SR) command to shift register 103, as illustrated in FIG. 2D. Shift register 103 shifts the tap point of delay lines 102 and 101 by one step to the right, decreasing the delay. If 201 goes low between the time 202 and 203 go high, the internal cycle time is properly adjusted and no shift command is generated, as illustrated in FIG. 2C. The output of the internal clock path in this case coincides with the rising edge of the external clock and is independent of external factors such as ambient temperature and processing parameters.

Conventional DDLLs, however, suffer from numerous drawbacks. One such drawback occurs in the event the DDLL is placed in a state of minimum or maximum delay. A state of minimum delay occurs when the delay between the input and output clock signals is as close to zero as allowed by the parameters of the delay line (i.e. when the tap point is at the very end of the delay line). In this case, if the DDLL attempts to decrease the delay, such decrease would be impossible because the delay line is already at minimum delay. Conversely, maximum delay occurs when the DDLL is as close to maximum delay as allowed by the parameters of the delay line (i.e. when the tap point is at the opposite end of the delay line). In the latter case, if the DDLL attempts to increase the delay, such increase would be impossible because the delay line is already at maximum delay. In these minimum and maximum delay states, the DDLL would be inoperable. A solution to this problem may be achieved by constructing a wrap-around loop, so that when the DDLL is at minimum delay, the delay line would shift around to maximum delay. This is not an optimal solution, however, because delay lines are typically of significant length and a lock could be achieved with a harmonic of the signal, which is undesirable.

Another drawback of conventional DDLLs is that they are inherently inaccurate. This inaccuracy is due to the fact that they compare a divided down version of the input clock signal, rather than the actual input clock signal, with the output clock signal, as shown in FIG. 2.

A further drawback of conventional DDLLs is that they are inherently inaccurate due to asymmetries in the delay line design. Typical logic-gate delay elements in conventional DDLLs are shown in FIG. 8 and operate as follows. Delay line 52 includes series connected delay elements, each delay element 51 consisting of two NAND gates and an inverter. The external clock is input into delay line 52 through a selected tap point, indicated by a high logic state in shift register 50. Depending on the command generated by the phase comparator (SL, SR, or no change), shift register 50 moves the tap point one delay element to the left or right, or does not shift the tap point. Unless the pull-up and pull-down times of the transistors forming the inverters and NANDs in each delay element are identical, however, the output of delay line 52 will consist of pulses with asymmetrical rising and falling edges. This asymmetry leads to differing time periods between any two rising and falling edges, as shown in FIG. 9(a). The output signal, therefore, will differ in shape from the input signal, which may lead to inaccuracies.

Yet another drawback of conventional DDLLs is that they operate under the constraint of random-initialized logic starting up at unknown values. This problem is typically resolved in conventional DDLLs by using initialization circuitry to power up the DDLL at some predetermined value. A drawback of this method of resolving the random-initialized logic problem is that if the initialization circuitry fails, it will be impossible for the DDLL to operate.

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There is a need, therefore, to improve the performance of DDLLs by resolving the inoperability of the DDLL in states of minimum and maximum delay without losing accuracy due to the possibility of locking on to a harmonic of the signal, rather than the actual signal. Further, there is a need for increasing the accuracy of DDLLs by achieving a lock with the actual input signal, rather than a divided-down version of the input signal. Additionally, there is a need for improving the performance of DDLLs by providing a symmetrical delay line output signal. Finally, there is a need for improving the accuracy and performance of DDLLs by ensuring insensitivity to random-initialized logic at power up.

SUMMARY OF THE INVENTION

The present invention alleviates to a great extent the above shortcomings of conventional DDLLs. The invention provides a unique method of and apparatus for improving the performance of DDLLs by resetting the DDLL in the event it enters a state of maximum delay. Further, the invention provides a unique method of and apparatus for improving the performance and accuracy of DDLLs by providing a symmetrical delay line design, power up insensitivity of the DDLL, and lock-on to the actual, not divided down, version of the input clock.

An apparatus for improving the performance of DDLLs in accordance with the present invention comprises the addition of a correction latch to a conventional DDLL, which latches an activation signal upon detection of a state of minimum delay and generates an override shift left (or disabled shift right) signal, causing the delay line to shift left towards more delay. The correction latch is reset once the system itself generates a shift left signal towards more delay, at which point the system resumes normal operation. An apparatus for improving the performance of DDLLs in accordance with the present invention further comprises a reset mechanism which resets the shift register to a state of minimum delay, upon detection of a state of maximum delay. The DDLL then continues operation as in a state of minimum delay. The clock insertion point of the DDLL is the first zero-to-one transition. Using the first zero-to-one transition as the clock insertion point ensures insensitivity of the present invention to random-initialized logic at power up.

Further, an apparatus for improving the performance of DDLLs in accordance with the present invention comprises a three-NAND logic circuit delay element design which results in substantially symmetrical rising and falling edges of the output signal.

Finally, the apparatus for improving the performance of DDLLs in accordance with the present invention comprises a phase detect circuit comparing the actual, not a divided-down, input signal with the output signal, thereby increasing the accuracy of the present invention over conventional DDLLs.

The present invention thus provides a DDLL with improved performance and accuracy due to its novel correction latch and reset mechanism circuitry for eliminating minimum and maximum DDLL delay state inoperability without the risk of locking on to a harmonic of the signal passing through the delay line, while at the same time ensuring power up insensitivity Additionally, the present invention provides a DDLL with improved performance and accuracy due to its symmetrical delay line design ensuring substantially symmetrical rising and falling edges of the signal at the output of each delay line logic circuit element.

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Finally, the present invention provides a DDLL with improved performance and accuracy due to ensuring a comparison between the actual, not divided-down, input signal and an output signal during a phase detect operation.

These and other advantages and features of the invention will become more clearly apparent from the following detailed description of the invention which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the operation of a known digital delayed lock loop circuit (DDLL);

FIG. 2A is a timing diagram showing the operation of the DDLL of FIG. 1;

FIG. 2B is a timing diagram showing a faster internal signal than the external signal;

FIG. 2C is a timing diagram showing adjusted internal and external signals;

FIG. 2D is a timing diagram showing a slower internal signal than the external signal;

FIG. 3 is a block diagram showing the operation of an improved DDLL in accordance with a preferred embodiment of the present invention;

FIG. 4 is a timing diagram showing the DDLL in a state of minimum delay;

FIG. 5 is a circuit diagram showing the logic circuit design of each delay element in the symmetrical delay line according to a preferred embodiment of the present invention;

FIG. 6 is a circuit diagram of the correction latch ensuring override shift left signals upon detection of a state of minimum delay, according to a preferred embodiment of the present invention;

FIG. 7 is a table indicating the operation of the correction latch in FIG. 6 depending upon the state of the correction latch;

FIG. 8 is a circuit diagram showing the logic circuit design of each delay element in a known delay line;

FIG. 9A is a timing chart showing the difference between the rising and falling edges of the signals at the outputs of the logic circuit delay elements shown in FIG. 8;

FIG. 9B is a timing chart showing the difference between the rising and falling edges of the signals at the outputs of the logic circuit delay elements shown in FIG. 5;

FIG. 10 is a block diagram of a printed circuit board (PCB) implementing the DDLL of the present invention; and

FIG. 11 is a block diagram of a computer system implementing the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention are now described in detail in connection with the accompanying drawings. FIG. 3 illustrates a block diagram of DDLL 10, which differs from a conventional DDLL in that there is a newly provided correction latch 14 which is connected to receive the shift left (SL) or shift right (SR) correction signal from phase detect circuit 15 via divide by two circuit 11. DDLL 10 further differs from a conventional DDLL in that there is newly provided a reset mechanism 16, designed to reset shift register 12 upon detection of a state of maximum delay.

DDLL 10 has an input clock signal CLCK IN (reference signal) which is fed into delay line 13 and an output clock

signal CLCK OUT, which differs in phase with respect to CLCK IN by a quantum of time, but which ideally should be in phase with CLCK IN. Phase detector 15 compares the phases of the CLCK IN and CLCK OUT signals (preferably, phase detect 15 operates to match the rising edge of signal CLCK OUT to a rising edge of signal CLCK IN) and generates a digital signal related to the difference in phase between the two signals. Preferably, phase detector 15 is a phase comparator wherein the output of the phase detector is a binary signal that is high if CLCK OUT is ahead in phase of CLCK IN and low if CLCK OUT is behind CLCK IN in phase. Alternatively, phase detector 15 may be configured to generate a low output if CLCK OUT is ahead in phase of CLCK IN and a high output if CLCK OUT is behind CLCK IN.

The binary signal is representative of whether CLCK OUT is delayed with respect to CLCK IN, fast with respect to CLCK IN, or in phase with respect to CLCK IN. Thus, this binary signal represents a shift left, shift right, or no signal, respectively, to be applied to shift register 12 for aligning the phases of CLCK IN and CLCK OUT.

The output of phase detector 15 is applied, after passing through divide by two circuit 11, to shift register 12, causing a change in the bit value of shift register 12 if CLCK IN and CLCK OUT are out of phase. Shift register 12 contains a plurality of stages storing a bit pattern which consists of all "0"s followed by all "1"s (or vice versa). The point of transition is where shift register 12 sets the delay of delay line 13. Consequently, the shift left and shift right signals cause this transition point to move one register stage to the left or right depending on the incoming command from divider 11.

Divider circuit 11 produces at its output two signals, SL' and SR', divided down from the output of phase detect 15. In this embodiment, divider circuit 11 is a divide by two circuit. The bit value change is one bit to the right if CLCK OUT is delayed with respect to CLCK IN or one bit to the left if CLCK OUT is ahead of CLCK IN. If CLCK IN and CLCK OUT are in phase, there is no change in the bit value of shift register 12.

A change in the bit value of shift register 12 to the left or to the right, operates to regulate the delay of delay line 13 by shifting the tap point (delay element) which controls the amount delay by one delay element to the left or the right respectively. Thus, in an 8-bit shift register, the first zero to one transition, is indicative of the location of the tap point. The tap point in FIG. 5, for example, is delay element n, indicating the first zero to one transition in shift register 12 (looking from left).

The problem arises when DDLL 10 in FIG. 3 enters a state of minimum or maximum delay. Minimum delay is the state when the tap point is the rightmost delay element of delay line 13 (i.e., delay element n+4 in FIG. 5). In this case, if CLCK IN and CLCK OUT are very close together, yet not completely in phase, DDLL 10 will operate to minimize the delay by generating an SR signal. However, delay line 13 cannot shift any further to the right because it is already at the last delay element (i.e., a high value in the last delay element would be indicative of minimum delay state and of the existence of a tap in the last delay element).

Thus, when the last delay element (n+4 in FIG. 5) goes high, delay line 13 generates a Qright signal to correction latch 14, which latches to override the SR' signal at the output of phase detect 15 and divider 11 and to instead generate a SL signal at its output. In this case, shift register 12 begins to shift left for each correction signal, beginning to fill shift register 12 with zeros from bit n+4 towards bit n−3.

The operation of DDLL 10 in a state of minimum delay is shown in FIG. 4. If DDLL 10 is in a state of minimum delay, but CLCK IN and CLCK OUT are not completely in phase as indicated by rising edges 25 (CLCK IN) and 27 (CLCK OUT), DDLL 10 will attempt to minimize the delay by shifting right to align rising edge 27 of CLCK OUT with rising edge 25 of CLCK IN. The delay line, however, cannot decrease the delay any more and the DDLL will begin generating a continuous SR command, without the delay line having the ability to implement it. Correction latch 14 registers this state based on the high Qright signal and overrides the shift right command, causing shift register 12 to begin shifting to the left, going more and more into delay, until it locks rising edges 26 and 28. Correction latch 14 is reset upon receipt of a SL' command from phase detect circuit 15, indicating that rising edge 26 is ahead of rising edge 28, and the system resumes normal operation. The Qright signal is generated whenever the rightmost bit position of shift register 12 (i.e., bit position n+4 in FIG. 5) contains a "1."

The function of divider circuit 11 in FIG. 3 is to reduce the instability that would otherwise be caused as a result of DDLL 10 attempting to make phase corrections in mid-cycle. This means that delay line 13 must be provided with at least one clock cycle to implement the previous phase detect SR or SL command, before being issued a new one. Divide by two circuit 11 enables corrections via correction latch 14 to occur on every other clock cycle, rather than on every cycle. This helps eliminate mid-cycle correction oscillation or jitter because it enables the current delay to propagate through delay line 13 before changing the value of delay line 13. Mid-cycle delay adjustments cause jitter because the delay line is adjusting itself on the fly, while at the same time feeding the output signal into phase detect circuit 15.

Reset mechanism 16 resets the DDLL to a state of minimum delay, if a state of maximum delay is encountered. Reset mechanism 16 may comprise, for example, a NAND gate. Maximum delay is the state when delay line 13 is functioning at its maximum delay (i.e. the tap is the leftmost element n−3 in delay line 13) and shift phase detect 15 issues a SL command. In this case, shift register 12 will be filled with low values (or zeros). Most importantly, the value of shift register bit n-3 will become zero, which will cause reset mechanism 16 to reset shift register 12 to a state of minimum delay. The DDLL then operates as described above with respect to a state of minimum delay (all "1"s).

The present invention is insensitive to random values upon initialization. The DDLL will operate regardless of the state it powers up to because the first zero to one transition in the shift register will cause the DDLL to operate normally. If the DDLL powers up to a state where there are no zero to one transitions (i.e. shift register 12 is filled with all ones or all zeros), the DDLL will operate as follows. If shift register 12 is filled with all ones, the DDLL is in a state of minimum delay and will operate as described above with respect to minimum delay. If shift register 12 is filled with all zeros, the DDLL is in a state of maximum delay and will be shifted to a state of minimum delay and operate as described above with respect to minimum delay.

FIG. 6 depicts the circuitry of correction latch 14 in FIG. 3 in more detail, according to a preferred embodiment of the present invention. Correction latch 14 consists of set-reset latch 41 and two multiplexers 42 and 43 connected to the SL' and SR' outputs of divider 11. The operation of this circuit is explained in connection with the table in FIG. 7. Signal Qright is generated when the rightmost delay element n+4 in

delay line **13** goes to a "1" state, i.e., when the DDLL is in minimum delay.

The table depicted in FIG. **7** indicates the status of the shift right (SR) and shift left (SL) signals at the output of correction latch **14** in FIG. **6**, depending on the latched/ unlatched state of set-reset latch **41**. Thus, when set-reset latch **41** is not latched, SL'=SL and SR'=SR, until Qright goes high ("1") and latch **41** latches. That would be the case of minimum delay, and SR' is high, but correction latch **14** operates to override it and to provide SR=0 and SL=SR, that is, SL goes high instead of SR and the shift register begins to insert zeros in the delay line starting at the n+4 element. This continues until correction latch **14** is reset, i.e., even if the DDLL is not in minimum delay and Qright now goes to "0," SR=0 and SL=SR will continue as the output of latch **14** until latch **14** is reset. Latch **14** is reset upon SL' going high, which indicates that CLCK OUT is ahead of CLCK IN and phase detect circuit **15** is compensating for this. At this time, SR=SR and SL=SL and the DDLL resumes its normal operation.

FIG. **5**. illustrates another aspect of the present invention, the structure and operation of delay element n in delay line **13**. FIG. **5** depicts an 8-bit shift register **12** connected to an 8-element delay line **13**, each delay element n of which has a novel symmetrical 3-NAND gate design. Each delay element n consists of 3 NAND logic circuits **31**, **32** and **33**, where the inputs of NAND **31** are the CLCK IN signal and the corresponding shift register bit (n); the inputs of NAND **32** are the output of the preceding delay element (n−1) and the output of NAND **31**; and the inputs of NAND **33** are the output of NAND **32** and the subsequent shift register bit (n+1). Thus, the clock insertion point (i.e., tap) in delay line **13** is at the first **0** to **1** transition (viewed from right to left in FIG. **5**).

Another aspect of the structure of delay element n in delay line **13** (FIG. **5**) is that because of its 3-NAND symmetrical design, it provides substantially symmetrical rising and falling edges of the CLCK OUT signal at its output. This is depicted in FIG. **9**(*b*), where Δt1' is very close to Δt2'. This is a significant advantage over the prior art shown in FIG. **8**, where delay element **51** of delay line **52** consists of two NAND elements and an inverter. Because the transistors forming the inverters and the NANDs in each delay element do not have identical rise and decay times, the signal at the output of prior art delay element **51** has asymmetrical rising and falling edges. The CLCK OUT signal will therefore differ in shape from the CLCK IN signal, leading to inaccuracies.

FIG. **10** shows printed circuit board (PCB) **300** with multiple ICs **301**, **302**, **304** having differences in the phases of the IC generated internal clocks. DDLL **303** operates to align the phases of the internally generated clock signals of ICs **301** and **302** according to the instant invention. PCB **300** could be used in a computer system where one of ICs **301** and **302** is a microprocessor and the other is a memory device, a storage device controller, or an input/output device controller.

FIG. **11** shows electronic system **400** having multiple PCBs **401**, **402**, operating as PCB **300** in FIG. **10**.

The present invention has broad applicability in all electronic computer systems employing more than one IC with an internal clock. The above description is intended to be illustrative, not restrictive. Many modifications which do not depart from the spirit or scope of the invention will be apparent to those skilled in the art upon reviewing the above description. Accordingly, the invention is not limited by the

foregoing description, but is only limited by the scope of the appended claims.

What is claimed is new and desired to be secured by Letters Patent of the United States is:

1. A computer system comprising:

a plurality of integrated circuits at least one of which is a microprocessor, each of said integrated circuits requiring a clock signal; and

at least one digital delay locked loop for synchronizing the required clock signals for said integrated circuits, said delay locked loop comprising:

a phase detect circuit for comparing the phases of an input and output clock signal and for outputting a control signal based on said comparison;

a delay line coupled to said input clock signal and a shift register, said delay line controlling a delay of said input clock signal based on a command from said shift register and for outputting a delayed input clock signal as said output clock signal to be compared by said phase detect circuit, said delay line having a delay state output; and

a correction latch coupled to said control signal, said shift register and said delay state output, said correction latch generating an override shift command to said shift register when a state of minimum delay is provided by said delay state output.

2. A computer system as in claim **1**, wherein said override shift command causes said shift register to output to said delay line a command to increase the delay in said delay line until the phase detect circuit generates a control signal to increase the delay.

3. A computer system as in claim **1**, wherein said digital delay locked loop further comprises a reset mechanism coupled to said shift register for resetting said shift register to a predetermined state when contents of said shift register correspond to a state of maximum delay in said delay line.

4. A computer system as in claim **1**, wherein said digital delay locked loop further comprises a divide by n frequency divider having an input coupled to said control signal and n outputs representing said control signal coupled to said correction latch, said n outputs controlling said correction latch to allow delay line correction on every nth input to said frequency divider.

5. A computer system as in claim **4**, wherein n equals 2.

6. A computer system as in claim **1**, wherein said delay line comprises at least two delay elements, at least one of which comprises:

a first logic circuit coupled to said input clock signal and an N output stage of said shift register;

a second logic circuit coupled to an output of said first logic circuit and an output of another of said at least two delay elements; and

a third logic circuit coupled to an output of said second logic circuit and to an N+1 output stage of said shift register,

whereby a transition from a low state to a high state between said N and N+1 output stages of said shift register controls an insertion point of said input clock signal into said delay line, thereby controlling said delay of said input clock signal.

7. A computer system as in claim **6**, wherein each of said logic circuits is a NAND gate.

8. A computer system as in claim **7**, wherein said at least one delay element ensures substantially symmetrical rising and falling edges of said output clock signal.

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9. A computer system comprising:

at least one printed circuit board having at least one reference clock and a plurality of integrated circuits at least one of which is a microprocessor, each of said integrated circuits requiring a clock signal; and

at least one digital delay locked loop for synchronizing the required clock signals for said integrated circuits, said delay locked loop comprising:

    a phase detect circuit for comparing the phases of an input and output signal and for outputting a control signal based on said comparison;

    a shift register responsive to said control signal;

    a delay line coupled to said input signal and said shift register, said delay line controlling a speed of said output signal based on a command from said shift register and for outputting said output signal to be compared by said phase detect circuit; and

    a reset mechanism coupled to a maximum delay stage of said shift register for resetting said shift register to a predetermined value when contents of said maximum delay stage correspond to a state of maximum delay in said delay line.

10. A computer system as in claim 9, wherein said digital delay locked loop further comprises:

    a latch circuit coupled to said shift register; and

    a divide by n frequency divider having an input coupled to said control signal and n outputs representing said control signal coupled to said latch circuit, said n outputs controlling said latch circuit to allow delay line correction on every nth input to said frequency divider.

11. A computer system as in claim 10, wherein n equals 2.

12. A computer system as in claim 9, wherein said delay line comprises at least two delay elements, at least one of which comprises:

    a first logic circuit coupled to said input signal and an N output stage of said shift register;

    a second logic circuit coupled to an output of said first logic circuit and an output of another of said at least two delay elements; and

    a third logic circuit coupled to an output of said second logic circuit and to an N+1 output stage of said shift register,

    whereby a transition from a low state to a high state between said N and N+1 output stages of said shift register controls an insertion point of said input signal into said delay line, thereby controlling said delay of said input signal.

13. A computer system as in claim 12, wherein each of said logic circuits is a NAND gate.

14. A computer system as in claim 13, wherein said at least one delay element ensures substantially symmetrical rising and falling edges of said output signal to be compared by said phase detect circuit.

15. A printed circuit board comprising:

a plurality of integrated circuits, at least some of which require a clock signal; and

at least one digital delay locked loop for synchronizing the required clock signals for said integrated circuits, said delay locked loop comprising:

    a phase detect circuit for comparing the phases of an input and output signal and for outputting a control signal based on said comparison;

    a delay line coupled to said input signal and a shift register, said delay line controlling a speed of said

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    output signal based on a command from said shift register and for outputting said output signal to be compared by said phase detect circuit, said delay line having a delay state output; and

    a correction latch coupled to said control signal, said shift register and said delay state output, said correction latch generating an override shift command to said shift register when a state of minimum delay is provided by said delay state output.

16. A printed circuit board as in claim 15, wherein said override shift command causes said shift register to output to said delay line a command to increase the delay in said delay line until the phase detect circuit generates a control signal to increase the delay.

17. A printed circuit board as in claim 15, wherein said digital delay locked loop further comprises a reset mechanism coupled to a maximum delay stage of said shift register for resetting said shift register when contents of said maximum delay stage correspond to a state of maximum delay in said delay line.

18. A printed circuit board as in claim 15, wherein said digital delay locked loop further comprises a divide by n frequency divider having an input coupled to said control signal and n outputs representing said control signal coupled to said correction latch, said n outputs controlling said correction latch to allow delay line correction on every nth input to said frequency divider.

19. A printed circuit board as in claim 15, wherein n equals 2.

20. A printed circuit board as in claim 15, wherein said delay line comprises at least two delay elements, at least one of which comprises:

    a first logic circuit coupled to said input signal and an N output stage of said shift register;

    a second logic circuit coupled to an output of said first logic circuit and an output of another of said at least two delay elements; and

    a third logic circuit coupled to an output of said second logic circuit and to an N+1 output stage of said shift register.

21. A printed circuit board as in claim 20, wherein each of said logic circuits is a NAND gate.

22. A printed circuit board as in claim 21, wherein said at least one delay element ensures substantially symmetrical rising and falling edges of said output signal to be compared by said phase detect circuit.

23. A printed circuit board comprising:

a plurality of integrated circuits, at least some of which require a clock signal; and

at least one digital delay locked loop for synchronizing the required clock signals for said integrated circuits, said delay locked loop comprising:

    a phase detect circuit for comparing the phases of an input and output signal and for outputting a control signal used to control a shift register based on said comparison,

    a delay line coupled to said input signal and said shift register for controlling a speed of said output signal based on a command from said shift register and for outputting said output signal to be compared by said phase detect circuit; and

    a reset mechanism coupled to a maximum delay stage of said shift register for resetting said shift register to a predetermined state when contents of said maximum delay stage correspond to a state of maximum delay in said delay line.

24. A printed circuit board as in claim 23, wherein said digital delay locked loop further comprises:

a latch circuit coupled to said shift register; and

a divide by n frequency divider having an input coupled to said control signal and n outputs representing said control signal coupled to said latch circuit, said n outputs controlling said latch circuit to allow delay line correction on every nth input to said frequency divider.

25. A printed circuit board as in claim 24, wherein n equals 2.

26. A printed circuit board as in claim 23, wherein said delay line comprises at least two delay elements, at least one of which comprises:

a first logic circuit coupled to said input signal and an N output stage of said shift register;

a second logic circuit coupled to an output of said first logic circuit and an output of another of said at least two delay elements; and

a third logic circuit coupled to an output of said second logic circuit and to an N+1 output stage of said shift register,

whereby a transition from a low state to a high state between said N and N+1 output stages of said shift register controls an insertion point of said input signal into said delay line, thereby controlling said delay of said input signal.

27. A printed circuit board as in claim 26, wherein each of said logic circuits is a NAND gate.

28. A printed circuit board as in claim 27, wherein said at least one delay element ensures substantially symmetrical rising and falling edges of said output signal to be compared by said phase detect circuit.

29. A digital delay locked loop circuit comprising:

a delay line for receiving an input signal and providing a delayed output signal a predetermined time after the input signal, said delay line having a delay state output;

a phase detect circuit for comparing the phases of the delayed output signal and the input signal and generating a phase detect signal related to the difference in phase between said two signals;

a shift register connected to said delay line for controlling a delay of said delay line; and

a correction latch coupled to the output of said phase detect circuit, said delay state output and said shift register, said correction latch sending an override signal to said shift register when a state of minimum delay is provided by said delay state output.

30. A digital delay locked loop circuit as in claim 29, wherein said override shift command causes said shift register to output a command to increase the delay in said delay line until the phase detect circuit generates a phase detect signal to increase the delay.

31. A digital delay locked loop circuit as in claim 30, further comprising a reset mechanism coupled to said shift register for resetting said shift register to a predetermined state when contents of said shift register correspond to a state of maximum delay in said delay line.

32. A printed circuit board as in claim 29, wherein said digital delay locked loop further comprises a divide by n frequency divider having an input coupled to said phase detect signal and n outputs representing said phase detect signal coupled to said correction latch, said n outputs controlling said correction latch to allow delay line correction on every nth input to said frequency divider.

33. A digital delay locked loop as in claim 32, wherein n equals 2.

34. A digital delay locked loop as in claim 29, wherein said delay line comprises at least two delay elements, at least one of which comprises:

a first logic circuit coupled to said input signal and an N output stage of said shift register;

a second logic circuit coupled to an output of said first logic circuit and an output of another of said at least two delay elements; and

a third logic circuit coupled to an output of said second logic circuit and to an N+1 output stage of said shift register,

whereby a transition from a low state to a high state between said N and N+1 output stages of said shift register controls an insertion point of said input clock signal into said delay line, thereby controlling said delay of said input signal.

35. A digital delay locked loop as in claim 34, wherein each of said logic circuits is a NAND gate.

36. A digital delay locked loop as in claim 35, wherein said at least one delay element ensures substantially symmetrical rising and falling edges of said output signal to be compared by said phase detect circuit.

37. A digital delay locked loop circuit comprising:

a delay line for receiving an input signal and providing a delayed output signal a predetermined time after the input signal;

a phase detect circuit for comparing the phases of the delayed output and input signals and generating a phase detect signal related to the difference in phase between said two signals;

a shift register connected to said phase detect signal and said delay line for controlling a delay of said delay line proportional to said phase detect signal; and

a reset mechanism coupled to a maximum delay stage of said shift register for resetting said shift register to a predetermined state when contents of said maximum delay stage correspond to a state of maximum delay in said delay line.

38. A digital delay locked loop as in claim 37, wherein said digital delay locked loop further comprises:

a latch circuit coupled to said shift register; and

a divide by n frequency divider having an input coupled to said phase detect signal and n outputs representing said phase detect signal coupled to said latch circuit, said n outputs controlling said latch circuit to allow delay line correction on every nth input to said frequency divider.

39. A digital delay locked loop as in claim 38, wherein n equals 2.

40. A digital delay locked loop as in claim 39, wherein said delay line comprises at least two delay elements, at least one of which comprises:

a first logic circuit coupled to said input signal and an N output stage of said shift register;

a second logic circuit coupled to an output of said first logic circuit and an output of another of said at least two delay elements; and

a third logic circuit coupled to an output of said second logic circuit and to an N+1 output stage of said shift register,

whereby a transition from a low state to a high state between said N and N+1 output stages of said shift register controls an insertion point of said input signal into said delay line, thereby controlling said delay of said input signal.

41. A digital delay locked loop as in claim **40**, wherein each of said logic circuits is a NAND gate.

42. A digital delay locked loop as in claim **41**, wherein said at least one delay element ensures substantially symmetrical rising and falling edges of said output signal to be compared by said phase detect circuit.

43. A method of synchronizing the phases of an input signal and an output signal, the method comprising the steps of:

receiving in a delay line an input signal and generating from the delay line a delayed output signal a predetermined time after the input signal;

outputting a delay state output from the delay line to a correction circuit connected to the phase detect circuit;

comparing the phases of the delayed output and input signals in a phase detect circuit and generating a phase detect signal related to the difference in phase between said output and input signals;

applying the phase detect signal to a shift register connected to the delay line through the correction circuit;

controlling a delay of the input signal in the delay line in accordance with a command from the shift register based on said phase detect signal; and

applying an override shift command from the correction circuit to the shift register when the delay state output represents a state of minimum delay in said delay line.

44. A method of synchronizing the phases of an input signal and an output signal as in claim **43**, further comprising the step of:

resetting said shift register when contents of said shift register correspond to a state of maximum delay in said delay line.

45. A method of synchronizing the phases of an input signal and an output signal as in claim **43**, further comprising the step of:

dividing the frequency of the output of said phase detect circuit in a frequency divider to generate a number of

divided outputs representing the output of the phase detect circuit; and

outputting the divided outputs to the correction circuit, whereby the divided outputs cause said correction circuit to provide said override shift command on every nth input to said frequency divider.

46. A method of synchronizing the phases of an input signal and an output signal as in claim **45**, wherein n equals 2.

47. A method of synchronizing the phases of an input signal and an output signal as in claim **46**, further comprising the step of:

detecting when contents of a maximum delay stage in the shift register represents a state of maximum delay in said delay line.

48. A logic circuit delay element of a delay line coupled to a shift register for controlling a delay of an input signal in a digital delay locked loop circuit, said delay element comprising:

a first logic circuit coupled to said input signal and an N output stage of said shift register;

a second logic circuit coupled to an output of said first logic circuit and an output of another delay element of the digital delay lock loop circuit; and

a third logic circuit coupled to an output of said second logic circuit and to an N+1 output stage of said shift register,

whereby a transition from a low state to a high state between said N and N+1 output stages of said shift register controls an insertion point of said input signal into said delay line, thereby controlling said delay of said input signal.

49. A delay element as in claim **48**, wherein each of said logic circuits is a NAND gate.

50. A delay element as in claim **49**, wherein said NAND gates ensure substantially symmetrical rising and falling edges of an output signal representing a delayed input signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

6,069,506

PATENT NO. :

DATED   :   May 30, 2000

INVENTOR(S) : Jason Miller et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 10:

Claim 19, line 1, "15" should read --18--.

Signed and Sealed this

Third Day of April, 2001

Attest:

NICHOLAS P. GODICI

Attesting Officer   *Acting Director of the United States Patent and Trademark Office*