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[54] SERIAL TO PARALLEL CONVERSION WITH PHASE LOCKED LOOP

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[51] Int. Cl.⁶ **H03M 9/00**

[52] U.S. Cl. **341/100; 386/46**

[58] Field of Search **341/100, 101**

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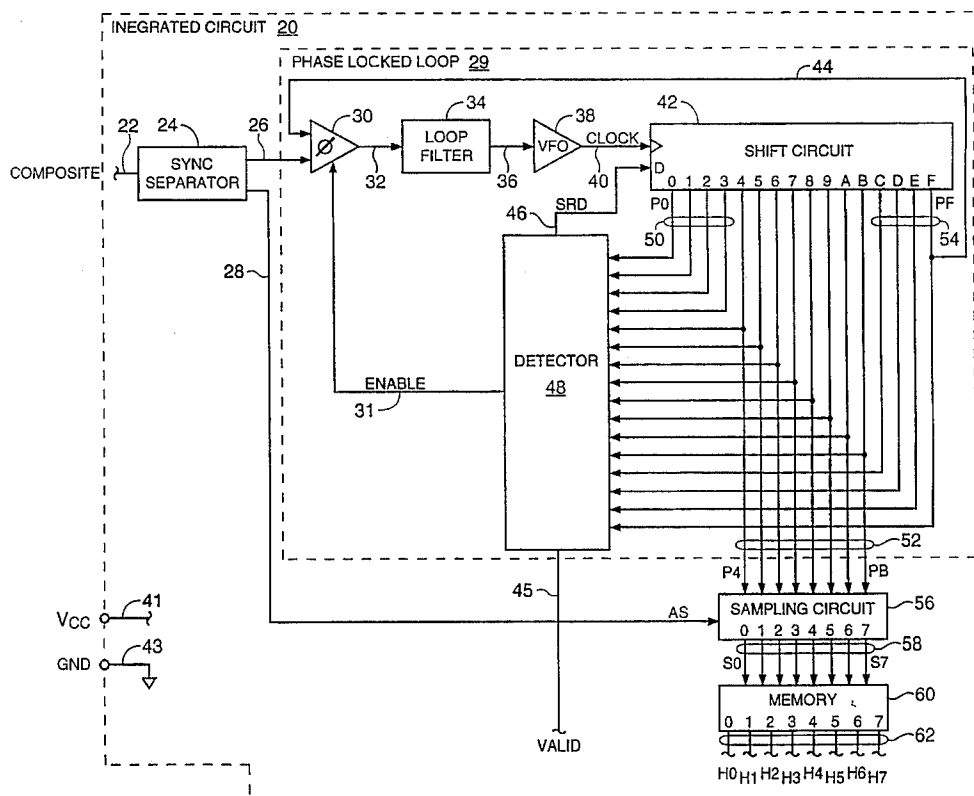
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[57] ABSTRACT

A serial to parallel conversion circuit uses a dynamic shift register in a phase locked loop for an index to access a parallel holding register. The composite input signal includes serial data to be sampled and a synchronizing signal at an integer factor of the sampling serial data rate. The phase locked loop generates a control signal for sampling the serial data at a multiple of the synchronizing frequency by incorporating a delay between a variable frequency oscillator output and a phase comparator input. The delay element in one embodiment includes a shift register with a walking-one pattern that overflows to the phase comparator. The walking-one pattern is used to identify which position of the holding register should store the next sample of the input signal. The shift register is self-initialized by a logic combination of all shift register outputs. Power dissipation by the serial to parallel conversion circuit is minimal because only one 7-transistor shift register cell draws current at a time.

22 Claims, 5 Drawing Sheets



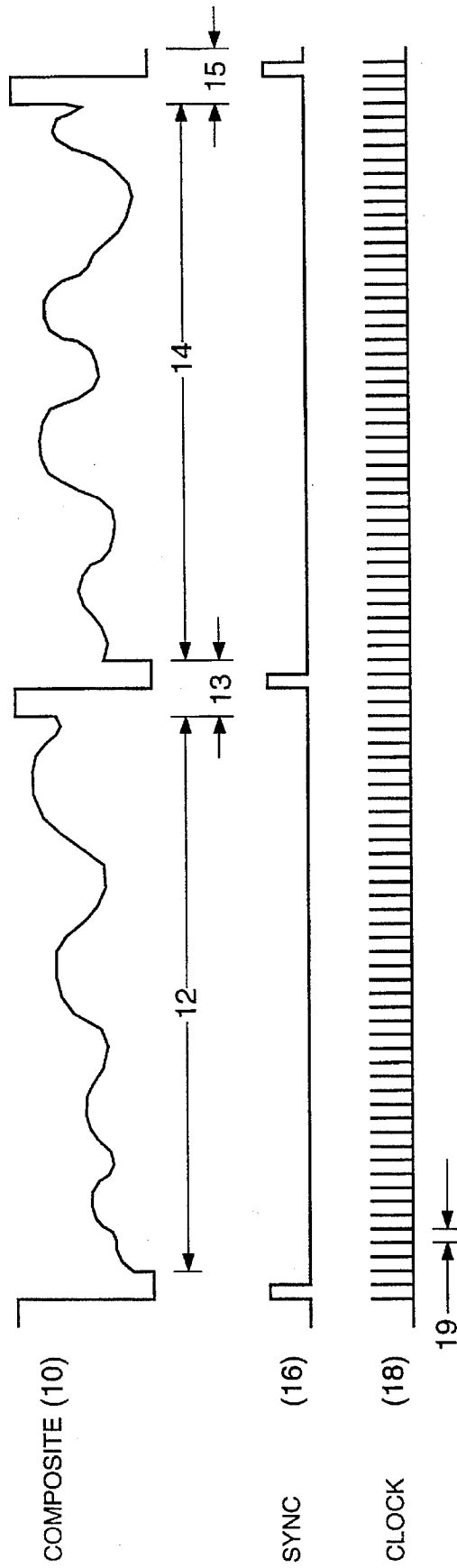


FIG. 1

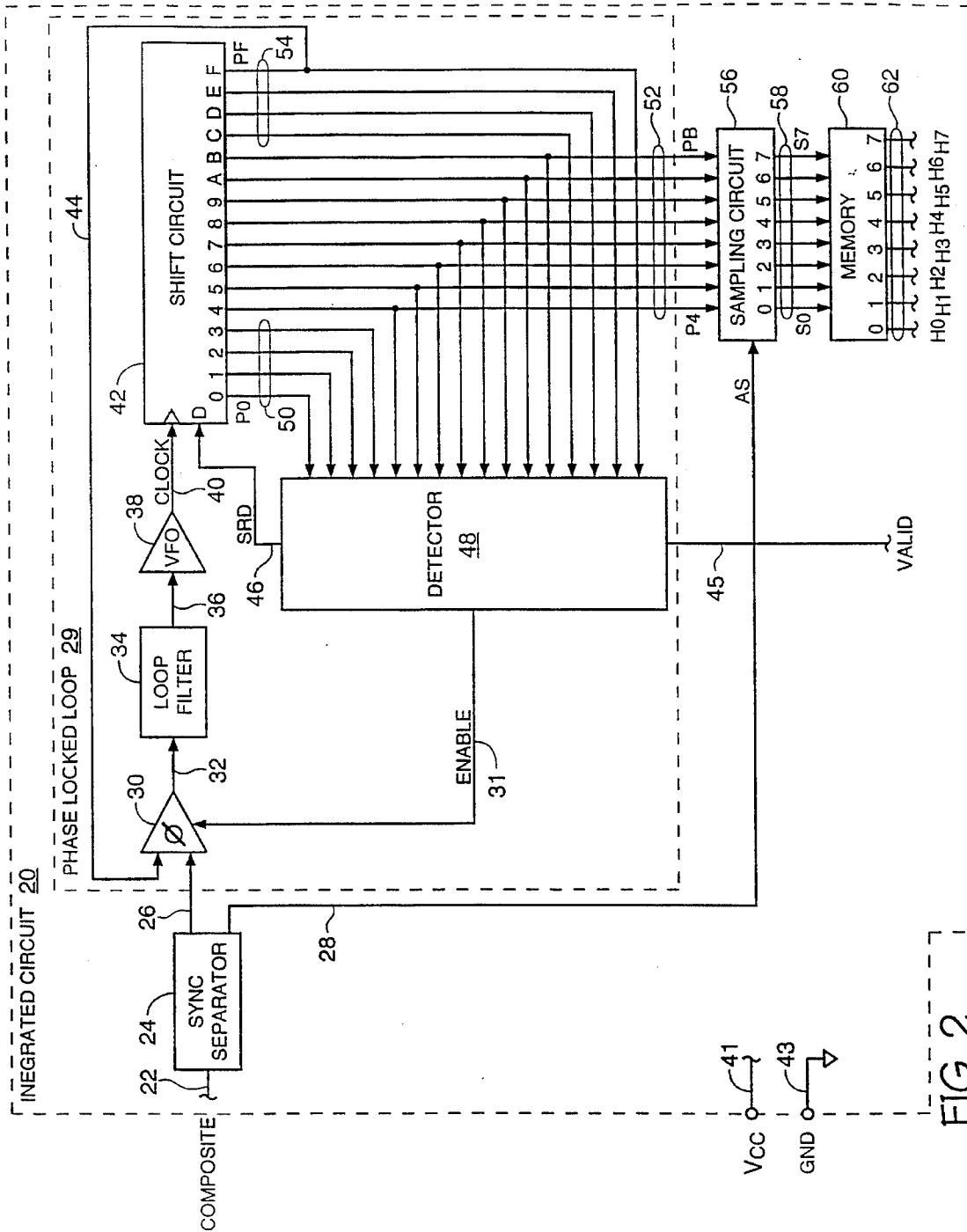


FIG. 2

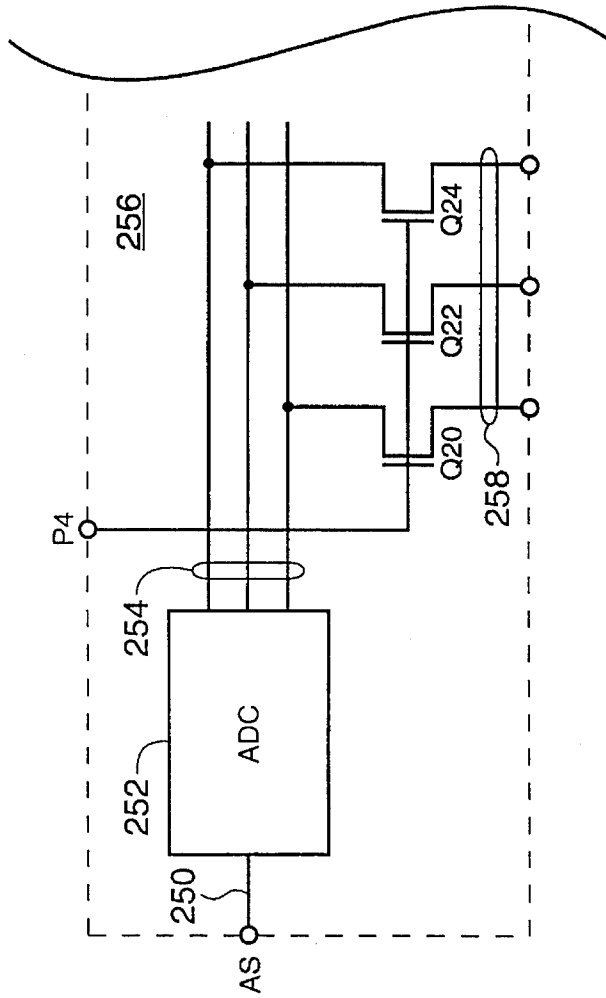


FIG. 3

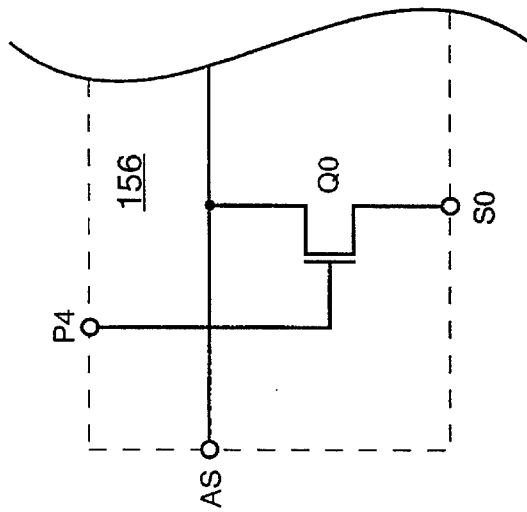


FIG. 4

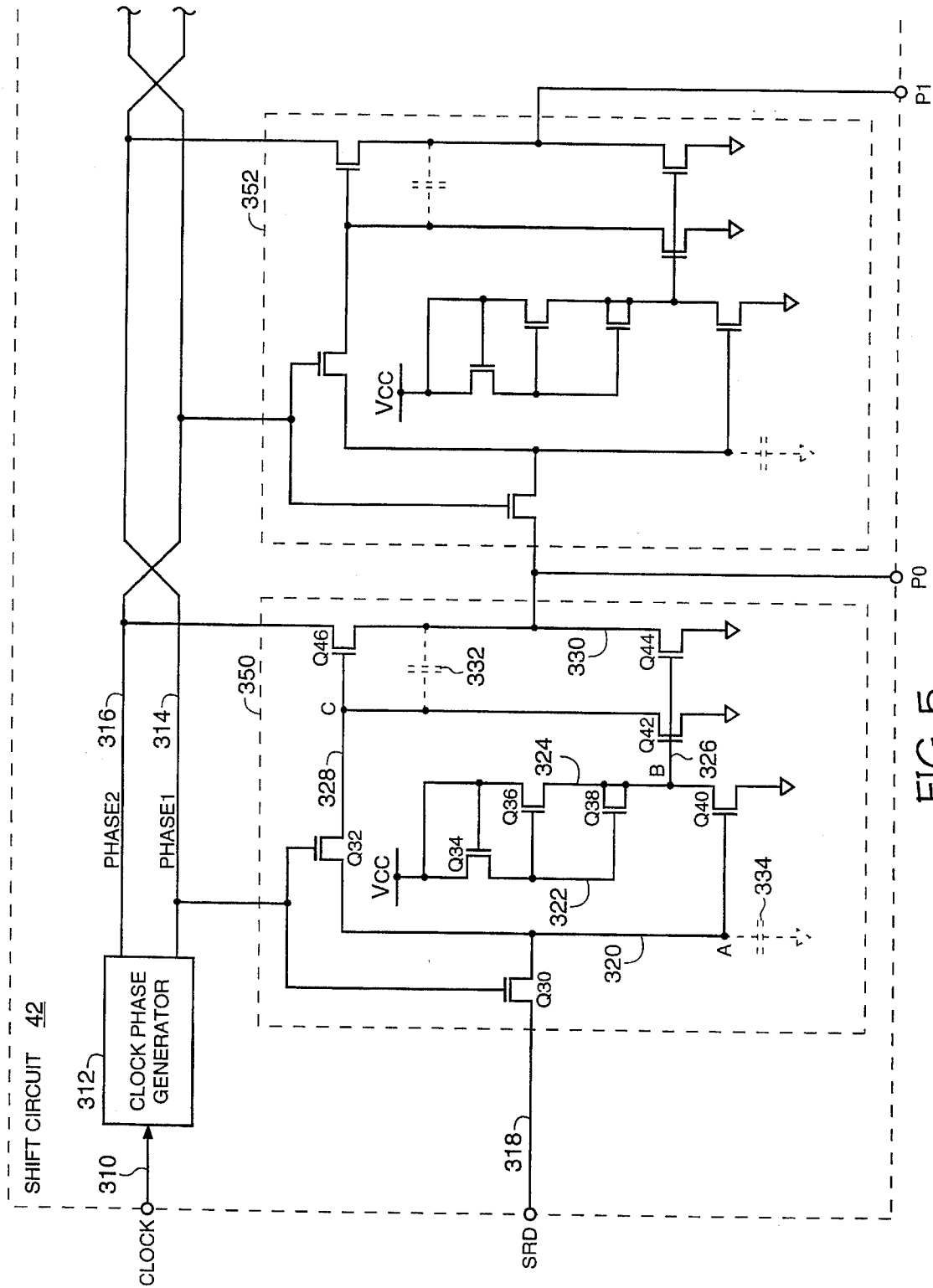


FIG. 5

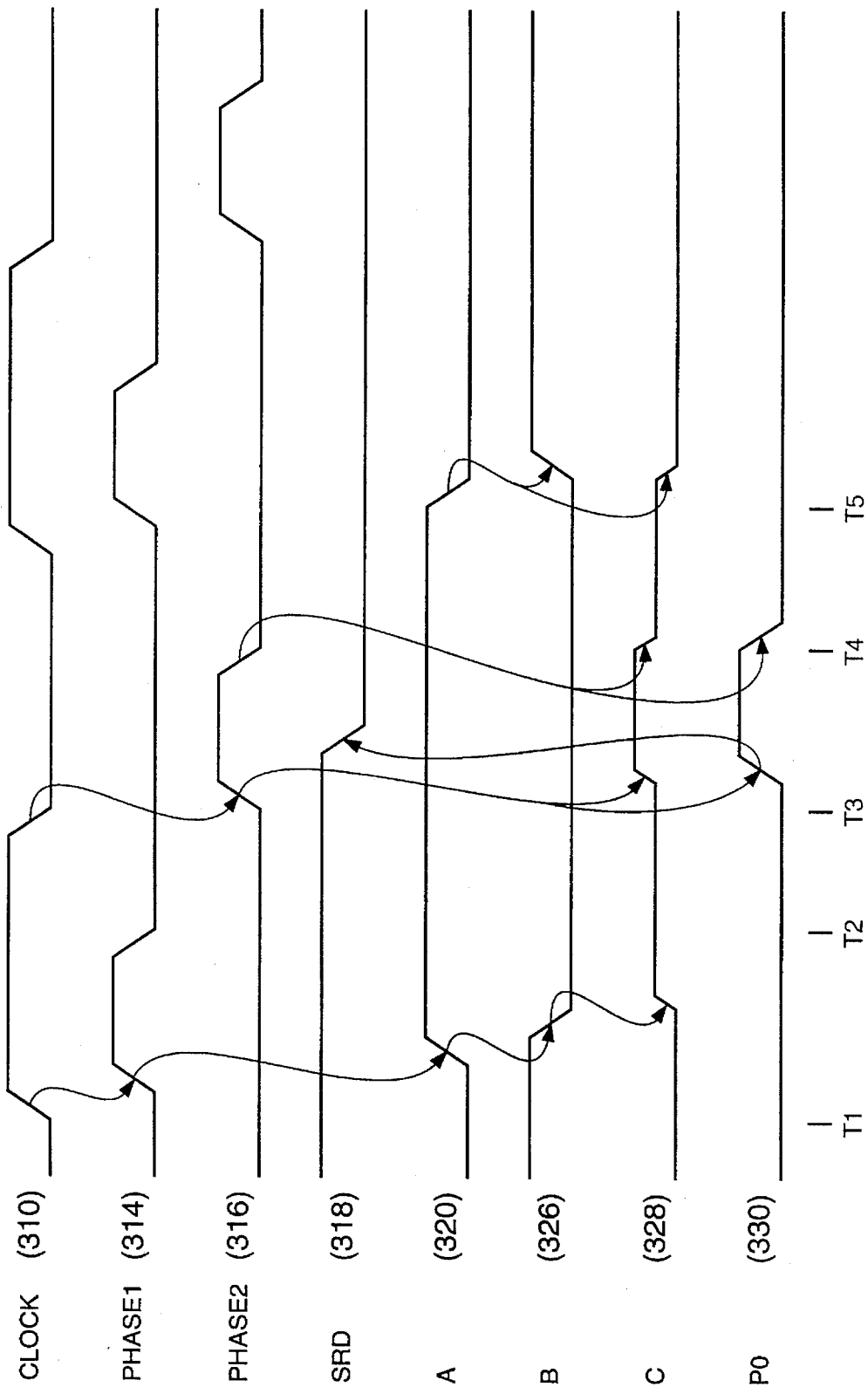


FIG. 6

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SERIAL TO PARALLEL CONVERSION WITH PHASE LOCKED LOOP

This invention was made with Government support under Contract No. DABT63-93-C-0025 awarded by Advanced Research Projects Agency (ARPA). The Government has certain rights in this invention.

FIELD OF THE INVENTION

This invention relates to serial to parallel conversion circuits and to systems for sampling composite signals.

BACKGROUND OF THE INVENTION

As an introduction to the problems solved by the present invention, consider a composite signal **10** containing both amplitude modulated information during a first period **12** and a synchronization signal, sometimes called a "sync" signal during a second period **13** as shown generally in FIG. **1**. Such signals are useful in instrumentation telemetry and communications systems, to name a few technologies, where a processor of analog information must be synchronized with the source of analog signals.

At the processor, sync signal **16** is separated from composite signal **10** to facilitate clock recovery. Conventional clock recovery circuits include a phase locked loop having a binary counter as a delay element. The carry signal, provided when the maximum count (N) of the counter is exceeded, is connected to a phase comparator of the loop along with the sync signal. The error signal resulting from phase comparison and low-pass filtering will keep a variable frequency oscillator (VFO) of the loop locked at a frequency N times the sync frequency. The clock recovered by the phase locked loop is then used to control sampling of the amplitude modulated portion of composite signal **10**.

Serial to parallel conversion of a number of samples is conventionally accomplished by separately addressing a memory device for each sample so that a number of samples can be provided in parallel. Where an analog memory, such as a charge storage device, is used, a shifting scheme is conventionally employed to simplify addressing. Where digital conversion and storage is used, a barrel shifter, or random access memory is conventionally employed with more complex addressing circuitry.

The serial to parallel circuit architecture described above is costly to implement as an integrated circuit. That architecture requires considerable surface area on the integrated circuit substrate, is adversely complex so that reliability and manufacturing yields cannot be further improved, suffers from considerable power consumption, and generates an adverse amount of heat.

In view of the problems described above and related problems that consequently become apparent to those skilled in the applicable arts, the need remains in serial to parallel conversion circuits and in systems for sampling composite signals for a serial to parallel conversion circuit especially for use on an integrated circuit substrate.

SUMMARY OF THE INVENTION

Accordingly, a serial to parallel conversion circuit in one embodiment of the present invention provides a plurality of output signals in parallel in response to an input signal that conveys data in serial, for example in the form of analog amplitudes, and a synchronizing signal. The conversion circuit includes a phase locked loop and a plurality of

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memory devices. The phase locked loop includes an oscillator, a shift circuit, and a comparator. The oscillator provides a clock signal at a period responsive to an error signal. The shift circuit shifts in response to the clock signal, and provides a pointer signal and an overflow signal. The comparator provides the error signal by comparing in response to the input signal and the overflow signal. The pointer signal identifies a memory device of the plurality for writing in response to the data. The memory devices thereby provide the plurality of output signals.

According to a first aspect of such an embodiment, the shift circuit serves two functions: to lock the loop on an integer multiple of the synchronizing signal and to identify the memory device for writing. By serving two functions, several benefits inure including: over all circuit complexity is reduced, less surface area on the integrated circuit substrate is used for the serial to parallel conversion function, reliability and manufacturing yields are improved, and power and heat consumption are reduced.

According to another aspect, the shift circuit shifts a walking pattern to assert the pointer signal. In one embodiment, the pointer signal is conveyed on a plurality of lines connecting the shift circuit and the memory devices. By shifting a walking-one pattern, only one line of the plurality is active, thus identifying a memory device without additional addressing circuitry such as a counter.

According to another aspect, the shift circuit includes a detector responsive to the pointer signal. The detector establishes and maintains the walking pattern. These functions constitute self-initialization. By self-initializing, the need for conventional power-on and power-fail detection circuitry is eliminated and start up problems associated with such circuitry are avoided.

According to yet another aspect, the shift circuit includes a plurality of stages characterized by minimal DC current consumption in one of two logic states. In operation, such a stage reduces power dissipation during shifting. By arranging the walking pattern with all but one stage in the state having minimal DC current consumption, overall power dissipation is reduced.

According to still another aspect, a shift stage of the present invention operates from a two phase clock so that generation of a clock at the sampling rate is not necessary. By operating from two half-frequency clocks, circuits of the present invention generate less noise, consume less power, and are less subject to variation in circuit structure and performance attributable to integrated circuit fabrication process variation.

The present invention may be practiced according to a method for providing a plurality of output signals in parallel, each respective output signal of the plurality responsive to a respective input signal value occurring during a first period. The method includes the steps of (1) determining the beginning of the first period and (2) maintaining the plurality of output signals in parallel. To determine the beginning of the first period, a variable frequency oscillator in cooperation with a phase comparator determines a second period by comparing the phase of a first signal, characterized by an integer multiple of the second period, with a second signal, characterized by the first period. An output of the oscillator is coupled to a shift circuit comprising shift bit positions at least equal in number to the integer. And, the shift circuit provides, for each shift bit position, a respective identifying signal. The plurality of output signals is maintained in parallel by, for each respective output signal, setting a respective memory device identified by the respective iden-

tifying signal, wherein setting is in response to sampling the respective input signal value.

According to a first aspect of such a method, by generating the identifying signal using the same shift circuit that is used to control the oscillator, synchronization between the input signal and the plurality of output signals is reliably maintained.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the articles, devices, methods, and combinations particularly pointed out in the appended claims.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a timing diagram of composite signal 10 for conversion by circuits and methods of the present invention.

FIG. 2 is a functional block diagram of an integrated circuit embodiment of the present invention.

FIG. 3 is a schematic diagram of a portion of the sampling circuit shown in FIG. 2.

FIG. 4 is a schematic diagram of an alternate sampling circuit of the present invention.

FIG. 5 is a schematic diagram of a portion of the shift circuit shown in FIG. 2.

FIG. 6 is a timing diagram of the operation of a shift stage of shift circuit 42 shown in FIG. 2.

A person having ordinary skill in the art will recognize where portions of a diagram have been expanded to improve the clarity of the presentation.

In each functional block diagram, a single line between functional blocks represents one or more signals. Signals that appear on several figures and have the same mnemonic are coupled together by direct connection or by additional devices. A signal named with a mnemonic and a second signal named with the same mnemonic followed by an asterisk are related by logic inversion.

In each timing diagram the vertical axis represents analog voltage or binary logic levels and the horizontal axis represents time. The vertical axis is intended to show the transition from active (asserted) to passive (non-asserted) levels of each logic signal. The voltages corresponding to the logic levels of the various signals are not necessarily identical among the various signals.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a timing diagram of a composite signal for conversion by circuits and methods of the present invention. COMPOSITE signal 10 includes a series of analog voltages representing varying data during a recurring period 12, 14. A synchronizing signal during periods 13, 15 recurs between each successive update of varying data. Because the synchronizing signal recurs once for every series of analog voltages, and the bandwidth of the analog voltages is limited, a frequency of the synchronizing signal can be determined by circuits receiving COMPOSITE signal 10. The number of analog voltages between successive recurrences of the sync signal is predetermined by systems design as an integer, for example 1000. The 1000 data values in period 12, also referred to as 1000 channels, in one embodiment are

updated by 1000 new data values in period 14. In another embodiment, data values in period 14 are unrelated to values in period 12 so that several thousand data values are communicated with a synchronizing signal.

By circuits and methods of the present invention discussed below, the plurality of analog amplitudes during periods 12, 14 are provided in parallel so that the value as last received for each channel is continuously maintained.

The remaining signals shown in FIG. 1 are discussed below in the context of circuits of the present invention that operate with reference to such signals.

FIG. 2 is a functional block diagram of an integrated circuit embodiment of the present invention. COMPOSITE signal 10 on line 22 is converted to parallel outputs H0 through H7 on lines 62 by integrated circuit 20. COMPOSITE signal 10 includes a synchronizing signal during periods 13, 15 shown in FIG. 1 as a maximum amplitude followed by a minimum amplitude with a bandwidth greater than the bandwidth of the composite signal during periods 12, 14. Sync separator circuit 24 detects this out-of-band signal and provides SYNC signal 16 on line 26. Conventional techniques are used in sync separator circuit 24 to detect and separate signals, such as edge detection, threshold detection, switching, filtering, and delay techniques.

The signal on line 28 in one embodiment includes COMPOSITE signal 10. In a second embodiment, the signal on line 28 is a blanked version of signal 10 so that the waveform during periods 13, 15 does not adversely affect other circuits of integrated circuit 20. Blanking is accomplished with conventional methods and circuits known in the art.

An integrated circuit in an alternate embodiment of the present invention does not include on-chip sync separation. In operation, lines 26 and 28 are coupled by two or more conductors to an external sync separator for receiving a sync signal and for receiving a signal separated from the synchronization signal.

Integrated circuit 20 includes phase locked loop 29 including phase detector 30, loop filter 34, variable frequency oscillator (VFO) 38, and shift circuit 42. Signal CLOCK 18, as shown in FIG. 1, appears on line 40 at the output of VFO 38. Shift circuit 42 provides a delay so that phase locked loop 29 locks on a period of the synchronizing frequency shown in FIG. 1 as period 12 plus period 13 while VFO 38 operates at a shorter period 19 as shown in FIG. 1. Phase detector 30, loop filter 34, and VFO 38 employ conventional circuits known in the art. For example, a conventional voltage controlled oscillator (VCO) is used in an alternate and equivalent embodiment of VFO 38.

In operation, phase comparator 30 responds to a difference in the phase of signals on lines 26 and 44 by outputting an error signal on line 32 at least in part proportional to the extent of the phase difference. Loop filter 34 in a preferred embodiment includes a low-pass filter for removing high frequency components from the error signal, to provide a band-limited frequency control signal on line 36. VFO 38 responds to the frequency control signal by adjusting its operating oscillator frequency and, hence, the period 19 of signal CLOCK 18 on line 40. By filtering the error signal, loop filter 34 prevents erratic frequency changes by VFO 38.

Shift circuit 42 shifts a pattern of high and low states in response to signal CLOCK 18 and provides pointer signals P0 through PF. Shift circuit 42 includes 16 shift stages. In alternate embodiments, fewer or more stages are used to provide a delay consistent with the duration between recurring periods 13, 15 and the number of analog amplitudes to be sampled as serial data during period 12.

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On initial or subsequent receipt of operating power on lines 41 and 43, the collective state of these shift stages will include a random population in the "high" state and the remainder in the "low" state. These stages are connected in series from a first shift bit position coupled to output P0 to a last shift bit position coupled to output PF so that, for every period of signal CLOCK 18 on line 40, the pattern of high and low states shifts to the right one shift bit position. Signal PF, provided at the last shift bit position, constitutes an overflow signal from shift circuit 42 and indicates, when "high" that a walking-one pattern has been shifted 15 times from the time the pattern was established.

Shift circuit 42 provides pointer signals P0 through PF on three groups of lines 50, 52, and 54. Pointer signals on lines in group 52 are connected to sampling circuit 56 for controlling sampling and for directing access to memory 60. Signals in groups 50 and 54 are connected to detector 48 for maintaining the walking-one pattern. By reserving a number of pointer lines at the beginning and at the end of period 12 shown on FIG. 1, accuracy of sampling is improved because sampling circuit 56 has time to settle or otherwise prepare for receipt of analog signals during period 12. In an alternate embodiment of integrated circuit 20, COMPOSITE signal 10 includes one or more additional periods during which serial to parallel conversion by integrated circuit 20 is not required. The length of such additional periods can be compensated for by selecting an appropriate number of lines for groups 50 and 54 as will be apparent to one of ordinary skill.

The pointer signal coupled from shift circuit 42 to sampling circuit 56 in the illustrated embodiment includes signals on 8 lines for identifying 8 samples per period 12. Also, signal group 52 is preceded and followed by shift bit positions not coupled to sampling circuit 56. In alternate and equivalent embodiments the number and time occurrence of signals to be sampled during period 12 varies with system design and the pointer signal is conveyed on one or more lines with one or more logic levels being associated with each pointer value. Also, the number of preceding and following shift bit positions (if any) that are not coupled to a sampling circuit may be in alternate embodiments, any number including zero.

For example, in another embodiment, 1000 samples immediately follow the sync signal period and an additional period having a duration equivalent to 3000 samples stands between the last sample and the next occurrence of the synchronizing signal. A shift circuit in such an embodiment includes 1000 shift stages and provides pointer signals P0 through P999 coupled to a sampling circuit in a manner similar to that shown in FIG. 2. In place of 3000 additional shift stages, a counter, started by the overflow signal P999, counts the remaining 3000 periods of the clock signal until the next sync signal is expected to occur. In such an embodiment, a conventional counter circuit is used to generate a carry signal used by detector circuitry, as would be appreciated by one of ordinary skill in the art in view of the detector functions described below.

In the embodiment shown in FIG. 2, detector 48 establishes and maintains a walking-one pattern in shift circuit 42, provides an ENABLE signal on line 31 and provides a VALID signal on line 45 using conventional logic circuitry. For establishing and maintaining a walking-one pattern, in one embodiment, detector 48 includes a 16 input NOR gate for providing an output "low" on signal SRD on line 46 when any input pointer signal P0 through PF is "high." Only when all pointer signals are "low" will the gate provide a "high" signal SRD on line 46. In operation, "low" signals are

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clocked into shift circuit 42 and shifted toward shift bit position PF until all shift stages of shift circuit 42 are "low." Then, one "high" signal is shifted into the first shift bit position; after which the walking-one pattern has been established and will be so maintained.

Detector 48 provides an ENABLE signal on line 31 so that phase comparator 30 is enabled for phase detection only when signal ENABLE is asserted. By not asserting signal ENABLE, the locked condition of phase locked loop 29 is easier to maintain. Phase comparator 30, when not enabled for phase comparison, maintains the error signal using one or more memory devices during times when signal ENABLE is not asserted.

To convert the COMPOSITE signal 10 shown in FIG. 1, a simpler variation of the circuit shown in FIG. 2 can be employed. As shown COMPOSITE signal 10 does not include additional periods during which serial to parallel conversion by integrated circuit 20 is required. For serial to parallel conversion of COMPOSITE signal 10, a phase comparator that remains continuously enabled for comparison is employed in place of phase comparator 30 shown in FIG. 2. Likewise, a detector that does not generate an ENABLE signal is employed in place of detector 48.

In the embodiment shown in FIG. 2, detector 48 also provides signal VALID on line 45. Parallel output values of signals H0 through H7 are considered valid when a walking-one pattern has been established and maintained for the maximum number of shifts of shift circuit 42.

Sampling circuit 56 samples analog signal AS on line 28 and provides signals 58 to memory 60. Operation of each of two different embodiments of sampling circuit 56 is discussed below with reference to FIGS. 3 and 4. In each embodiment, when one pointer signal, for example P4, is asserted, a measurement of the amplitude of signal AS is provided as sample signal S0.

Memory 60 includes 8 addressable storage locations corresponding to pointer signals P4 through PB, respectively, into which samples of analog signal AS on line 28 are stored as conveyed by signals S0 through S7 on lines 58. For each address, memory 60 includes a memory device of the type appropriate to the signal to be stored. For example, when sample signal S0 is an analog amplitude, the memory device associated with output signal H0 is a conventional analog memory, such as a charge coupled device, a capacitance, or the like. Alternately, when sample signal S0 is a digital signal, the memory device is a conventional digital memory circuit such as a flip flop, a register, a dynamic memory cell, a magnetic bubble, or the like. In an alternate and equivalent embodiment where signal S0 is, for example, a 3-bit digital signal, 3 memory devices in parallel are used for each address in memory 60.

Memory 60 provides 8 output signals H0 through H7 on lines 62, one corresponding to each addressable storage location. These 8 output signals appear in parallel, accomplishing the serial to parallel conversion function of integrated circuit 20.

FIG. 3 is a schematic diagram of a portion of the sampling circuit shown in FIG. 2. In an embodiment wherein memory 60 stores analog samples, sampling circuit 156 performs the functions of sampling circuit 56 as already described. Transistor Q0 is a MOS field effect transistor that operates as a gate, conducting analog signal AS to be conveyed to memory 60 by signal S0 when pointer signal P4 is asserted "high."

In an alternate and equivalent embodiment, signal AS is coupled to the gate of transistor Q0 and pointer signal P4 is

coupled to the channel. This alternate embodiment matches P4 and AS signal drive capabilities and the signal S0 response time to alternate system performance criteria.

FIG. 4 is a schematic diagram of a portion of an alternate sampling circuit of the present invention wherein memory 60 stores digital samples. Sampling circuit 256 performs the functions of sampling circuit 56 as already described. Analog to digital converter (ADC) 252 in one embodiment includes a conventional flash ADC circuit that provides a 3-bit binary value on lines 254 proportional to the amplitude of signal AS. Each transistor Q20 through Q24 is a MOS field effect transistor that operates as a gate, conducting a signal on a respective line 254 to be conveyed to memory 60 on a respective line 258 when pointer signal P4 is asserted "high." In the embodiment shown in FIG. 4, signal S0 conveys a 3-bit binary value for each sample and memory 60 includes 3 digital memory devices per position.

Before discussing FIG. 5, it is worth noting that in an alternate and equivalent embodiment, shift circuit 42 shown in FIG. 2 is constructed of conventional bi-stable flip flop circuits. Such circuits are static in that the pattern is maintained when shifting is postponed indefinitely. Similarly in another alternate embodiment, some power savings and substrate surface savings result from using conventional dynamic shift register stage circuitry for shift circuit 42. In a preferred embodiment, considerable savings in both power dissipation and substrate surface area are realized using a plurality of dynamic shift circuit stages for shift circuit 42, each stage as shown in FIG. 5.

FIG. 5 is a schematic diagram of a portion of shift circuit 42 shown in FIG. 2. In the portion shown, clock phase generator 312 cooperates with all shift stages of which shift stages 350 and 352 are representative. Transistors Q30 through Q46 form shift stage 350 at the first shift bit position and generate pointer signal P0 on line 330. Based on signal CLOCK 18 on line 310, clock phase generator 312 generates two non-overlapping clock phase signals, PHASE1 and PHASE2, on lines 314 and 316 using conventional timing and logic circuits. Because shift circuit 42 shifts on every edge of CLOCK signal 18, the need for a signal of twice the frequency of signal CLOCK signal 18 is eliminated. Operation of shift stage 350 is best understood with reference to a timing diagram. All stages in shift circuit 42, in the preferred embodiment, are identical to shift stage 350, shown in FIG. 5.

FIG. 6 is a timing diagram of the operation of shift stage 350 of shift circuit 42 shown in FIG. 2. In summary, from time T1 to time T3 stage 350 toggles from "low" to "high" in response to a "high" signal SRD on line 318. Consequently, stage 350 asserts identifying signal P0 on line 330 "high." From time T3 to time T5, a "low" on signal SRD on line 318 toggles stage 350 so that identifying signal 330 is not asserted.

Assuming for the sake of description that stage 350 was providing a "low" on identifying signal P0 prior to time T1, at time T1 the rising edge of signal CLOCK 18 on line 310 causes transistors Q30 and Q32 to conduct, signal A on line 320 to go "high," transistor Q40 to conduct, transistor Q42 to stop conducting, and signal C on line 328 to go "high." After a delay prescribed by clock phase generator 312, signal PHASE1 goes "low" isolating stage 350 from further changes or noise on line 318. Then, in response to the falling edge of signal CLOCK 18, signal PHASE2 on line 316 goes "high," transistor Q46, in cooperation with an intrinsic capacitance between lines 328 and 330, "boots" and provides signal P0 on line 330 at or near the Vcc power supply potential.

Stage 350 is coupled to the next stage 352 by data line 320 and clock lines 314 and 316. By reversing lines 314 and 316 into next stage 352, operations in stage 350 just after time T1 are performed in next stage 352 just after time T3. Therefore, when signal PHASE2 on line 316 goes "low" so that transistor Q46 no longer supplies current to line 330, there is no adverse effect in next stage 352, since next stage 352 has already seized data from line 330 and will soon enter the isolated state.

Stage 350 draws minimal current when identifying signal P0 is "low" and little additional current when a "low" bit is shifted through stage 350. Stage 350 draws a nominal current through transistors Q34 through Q38 when signal A on line 320 is "high." However, since shift circuit 42 in cooperation with logic circuit 48 shifts a walking-one pattern, identifying signal P0 is predominantly "low" resulting in remarkably low power dissipation in shift circuit 42.

In a preferred embodiment of the circuit shown in FIG. 5, transistor Q42 is designed to provide weak drive capability. This capability is realized by conventional techniques including making the channel of Q42 for example four times longer than the nominal channel length used for the remaining transistors shown on FIG. 5. Other performance advantages are realized by (1) arranging transistors Q36 and Q38 to provide significant capacitance for "booting" transistor Q42, (2) arranging parasitic capacitances at line 320 to ground and between lines 328 and 330 for improved switching operation, and (3) arranging a favorable capacitive divider at node C. The latter is accomplished in a preferred embodiment by making transistor Q46 about 3 times larger than transistor Q32 and by using conventional layout techniques to assure that the capacitance between lines 314 and 328 is about ten times smaller than all other capacitance on node C.

The foregoing description discusses preferred embodiments of the present invention, which may be changed or modified without departing from the scope of the present invention.

For example, P-channel FETs may be replaced with N-channel FETs (and vice versa) in some applications with appropriate polarity changes in controlling signals as required. Moreover, the P-channel and N-channel FETs discussed above generally represent active devices which may be replaced with bipolar or other technology active devices.

Still further, those skilled in the art will understand that the logical elements described above may be formed using a wide variety of logical gates employing any polarity of input or output signals and that the logical values described above may be implemented using different voltage polarities. As an example, an AND element may be formed using an AND gate or a NAND gate when all input signals exhibit a positive logic convention or it may be formed using an OR gate or a NOR gate when all input signals exhibit a negative logic convention.

These and other changes and modifications are intended to be included within the scope of the present invention.

While for the sake of clarity and ease of description, several specific embodiments of the invention have been described; the scope of the invention is intended to be measured by the claims as set forth below. The description is not intended to be exhaustive or to limit the invention to the form disclosed. Other embodiments of the invention will be apparent in light of the disclosure to one of ordinary skill in the art to which the invention applies.

The words and phrases used in the claims are intended to be broadly construed. An "integrated circuit" refers gener-

ally to circuits produced using photolithography and includes but is not limited to a packaged integrated circuit, a portion of a packaged integrated circuit, an unpackaged integrated circuit, a combination on a substrate of packaged or unpackaged integrated circuits or both, a microprocessor, a microcontroller, a memory, combinations thereof, and equivalents.

A "memory device" refers generally to a static random access memory, a dynamic random access memory, a register, a flip-flop, a charge-coupled device, combinations thereof, and equivalents.

A "signal" refers to mechanical and/or electromagnetic energy conveying information. When elements are coupled, a signal is conveyed in any manner feasible with regard to the nature of the coupling. For example, if several electrical conductors couple two elements, then the relevant signal comprises the energy on one, some, or all conductors at a given time or time period.

When a physical property of a signal has a quantitative measure and the property is used by design to control or communicate information, then the signal is said to be characterized by having a "value." The amplitude may be instantaneous or an average. For a binary (digital) signal, the two characteristic values are equivalently called logic states and logic levels "high" and "low."

What is claimed is:

1. An integrated circuit responsive to an input signal for providing a first plurality of parallel signals, the integrated circuit formed on a substrate, the integrated circuit comprising:

- a. a voltage controlled oscillator, formed on the substrate, responsive to an error signal for determining a frequency of oscillation and thereby determining a first period;
- b. an N-bit dynamic shift register, formed on the substrate and clocked by the oscillator, the shift register for multiplying the first period by an integer N to determine a second period, the shift register comprising N parallel register outputs, the shift register comprising a first bit and a last bit;
- c. a phase comparator, formed on the substrate, comprising a first input coupled to the last bit, and a second input responsive to the input signal, the phase comparator for providing the error signal in response to the first input and the second input;
- d. a gate, formed on the substrate, having a gate output coupled to the first bit, the gate responsive to the register outputs for initializing the shift register with a pattern comprising only one asserted bit, the pattern being aligned at the last bit N shifts after being aligned at the first bit; and
- e. a sampling circuit, formed on the substrate, responsive to the register outputs and the input signal for sampling the input signal to provide a second plurality of samples, for storing the second plurality of samples, and for outputting in response to the second plurality of samples the first plurality of parallel signals.

2. The integrated circuit of claim 1 wherein:

- a. the input signal comprises a synchronizing signal and an analog signal, the phase comparator being responsive to the synchronizing signal for providing the error signal, the sampling circuit being responsive to the analog signal for providing the second plurality of samples; and
- b. the synchronizing signal and the analog signal are conveyed within the integrated circuit on one conductor.

3. The integrated circuit of claim 1 wherein:

- a. the input signal comprises a synchronizing signal; and
- b. the second input of the phase comparator is responsive to the synchronizing signal for providing the error signal.

4. The integrated circuit of claim 3 wherein:

- a. the synchronizing signal is received by the integrated circuit on a first conductor; and
- b. the input signal comprises an analog signal received by the integrated circuit on a second conductor, the sampling circuit being responsive to the analog signal for providing the second plurality of samples.

5. A serial to parallel conversion circuit that provides a plurality of parallel signals in response to an input signal, wherein the input signal conveys data in serial and conveys a synchronizing signal, the conversion circuit comprising:

- a. a phase locked loop comprising:
 - (1) an oscillator that provides a clock signal at a period responsive to an error signal;
 - (2) a shift circuit that shifts in response to the clock signal, provides a pointer signal, and provides an overflow signal;
 - (3) a comparator that provides the error signal by comparing in response to the synchronizing signal and the overflow signal; and
- b. a plurality of memory devices that provide the plurality of parallel signals, wherein the pointer signal identifies a memory device of the plurality for writing in response to the data.

6. The integrated circuit of claim 5 wherein the memory device is identified for writing once during each second period.

7. The integrated circuit of claim 5 wherein the memory device is identified for writing during selected recurrences of the second period.

8. The conversion circuit of claim 5 wherein the shift circuit comprises a flip flop.

9. The conversion circuit of claim 5 wherein the shift circuit comprises a dynamic shift register stage.

10. The conversion circuit of claim 5 wherein the shift circuit shifts a walking pattern to assert the pointer signal.

11. The conversion circuit of claim 10 wherein the shift circuit comprises a detector responsive to the pointer signal, and the walking pattern is maintained by clocking an output of the detector into the shift circuit.

12. The conversion circuit of claim 11 wherein the detector provides a validity signal when the plurality of output signals correspond to the data as clocked between two successive occurrences of the overflow signal.

13. The conversion circuit of claim 10 wherein:

- a. the pointer signal comprises a signal on each of a plurality of lines; and
- b. the walking pattern asserts a signal on only one of the plurality of lines.

14. The conversion circuit of claim 5 wherein:

- a. the comparator is selectively enabled for providing the error signal in response to a phase difference between the overflow signal and the synchronizing frequency; and
- b. the comparator comprises a second memory device for maintaining the error signal when the phase comparator is not enabled.

15. The conversion circuit of claim 5 wherein:

- a. the plurality of memory devices comprises a first number of memory devices; and

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b. the shift circuit comprises a second number of shift stages, the second number being greater than the first number.

16. The conversion circuit of claim 15 wherein a memory device of the plurality of memory devices is written when the overflow signal is provided. 5

17. The conversion circuit of claim 16 wherein a memory device of the plurality of memory devices is written when a first occurring clock signal is provided after the overflow signal is provided. 10

18. The conversion circuit of claim 5 wherein:

a. a memory device of the plurality of memory devices is written when the overflow signal is provided; and

b. a memory device of the plurality of memory devices is written when a first occurring clock signal is provided after the overflow signal is provided. 15

19. The integrated circuit of claim 5 wherein:

a. the shift circuit comprises a first integer number of shift stages; 20

b. the first plurality comprises a second integer number of parallel signals; and

c. the first number is greater than the second number.

20. The conversion circuit of claim 5, operative between a first potential and a second potential, wherein the shift circuit comprises a shift stage comprising: 25

a. an input node that receives a bit to be shifted;

b. an output node that provides the pointer signal;

c. a circuit that receives the clock signal and provides a first control signal and a second control signal; 30

d. a first field effect transistor comprising:

(1) a first gate that receives the first control signal; and

(2) a first channel coupled in series between the input node and a first node; 35

e. a second field effect transistor comprising:

(1) a second gate coupled to the first node; and

(2) a second channel coupled in series between a second node and the second potential;

f. a device having a resistance, the device coupled in series between the first potential and the second node; 40

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g. a third field effect transistor comprising:

(1) a third gate coupled to the second node; and

(2) a third channel coupled in series between a third node and the second potential;

h. a fourth field effect transistor comprising:

(1) a fourth gate coupled to the first control signal; and

(2) a fourth channel coupled in series between the first node and the third node;

i. a fifth field effect transistor comprising:

(1) a fifth gate coupled to the second node; and

(2) a fifth channel coupled in series between the output node and the second potential; and

j. a sixth field effect transistor comprising:

(1) a sixth gate coupled to the third node; and

(2) a sixth channel coupled to conduct the second control signal to the output node.

21. A method for providing a plurality of output signals in parallel, each respective output signal of the plurality responsive to a respective input signal value occurring during a first period, the method comprising the steps of:

a. determining the beginning of the first period, using a variable frequency oscillator that determines a second period, by comparing the phase of a first signal, characterized by an integer multiple of the second period, with a second signal, characterized by the first period, an output of the oscillator being coupled to a shift circuit comprising shift bit positions at least equal in number to the integer, the shift register providing, for each shift bit position, a respective identifying signal; and

b. maintaining the plurality of output signals in parallel by, for each respective output signal, setting a respective memory device identified by the respective identifying signal, wherein setting is in response to sampling the respective input signal value.

22. The method of claim 21 further comprising the step of loading all shift bit positions of the shift register in response to a logic combination of all identifying signals.

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