Design and Layout of Schottky Diodes in a Standard CMOS Process

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Research Goals

• Design and layout Schottky diodes in a standard CMOS process
• Increase the active frequency range of the Schottky diodes through improvements in layout design
• Simulate detector circuit
• Fabricate designs through MOSIS and characterize diodes
Diode Improvements

- Reduce series resistance by interdigitating the Schottky and ohmic contacts
- eliminate electrons being swept down to the body
Capacitor Design

- Minimize lost charge through the substrate to ground by increasing $d$ \( (C = \varepsilon A/d) \)
- Sizing set to dominate over junction capacitance of the diode
- Interdigitated layout to take advantage of fringe capacitance
Schottky Diode and Capacitor

Schottky diode layout

Capacitor layout
Layout view in LASI

- Layout view of the Schottky diode and capacitor
Schottky Diodes

- Pictures of devices fabricated through MOSIS (AMI 1.2µm process)
DC Characteristics

- I-V Curves of the Schottky diodes in the Square Law Region
Log \( I_d \) vs \( V_d \)

\[
\frac{I}{(1-e^{-V_d/kT})}
\]

<table>
<thead>
<tr>
<th>Diode Width</th>
<th>30( \mu )m</th>
<th>30( \mu )m int</th>
<th>40( \mu )m</th>
<th>40( \mu )m int</th>
<th>60( \mu )m int</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_s )</td>
<td>70n</td>
<td>100n</td>
<td>3n</td>
<td>90n</td>
<td>100n</td>
</tr>
<tr>
<td>( \phi_b )</td>
<td>.546</td>
<td>.536</td>
<td>.642</td>
<td>.554</td>
<td>.465</td>
</tr>
</tbody>
</table>
Circuit Characteristics

Schottky Detector Circuit

```
.control
destroy all
run
plot vin
plot vout
.endc
D1 VD 0 dmod 30
C1 Vin VD .5p
R1 VD Vout 1k
C2 Vout 0 10p IC=0
Vin Vin 0 sin 0 500m 1G
.TRAN .1n 30u
.MODEL dmod D vj=0.3 cjo=0 tt=0
rs=10
.end
```
What have we been doing?

- Design of Schottky diodes, first-chip
- Picture shown for one of the test sites on the chip.
• Had a spacing problem between the probe pads which affected the microwave measurements. Fixed the problem and re-fabricated.
• Several different types of test structures
• Measured the DC voltage out as a function of microwave power applied to the test structure.
• We also looked at the frequency behavior of the circuit.
Conclusion

• Reduce the series resistance of the Schottky diode by interdigitating the Schottky and ohmic contacts
• Minimize lost charge to the body by interdigitating the capacitor
• Devices have, and will be, fabricated through MOSIS in two processes, 1.2µm and .5µm
• Results will be documented upon return from MOSIS