A *K*-Delta-1-Sigma Modulator for Wideband Analog-to-Digital Conversion

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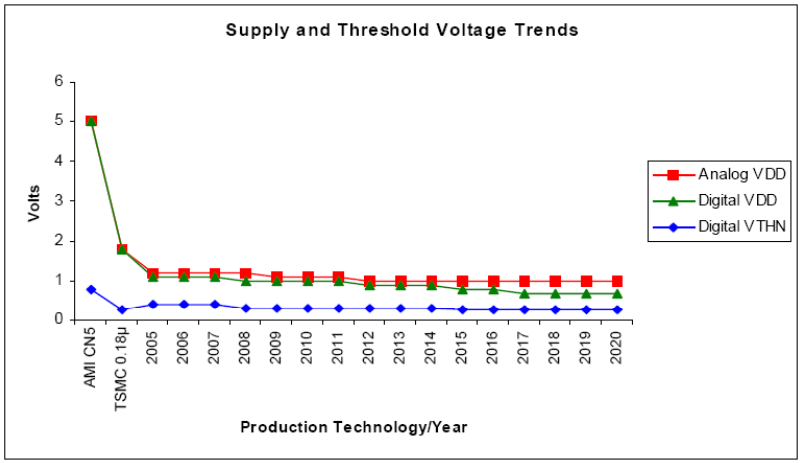
Abstract :

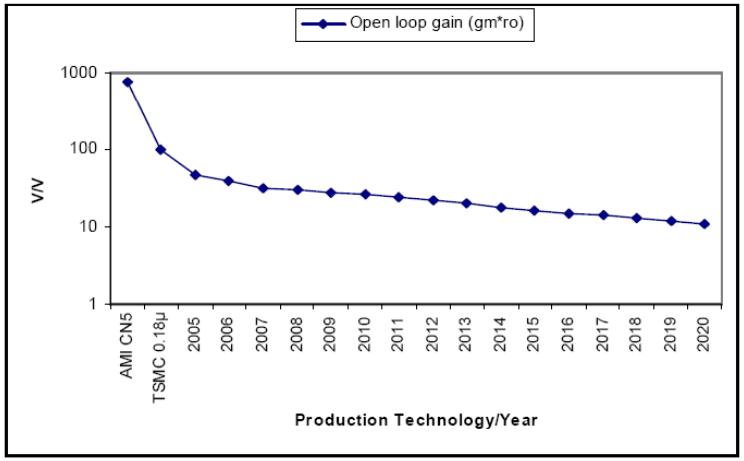
As CMOS technology shrinks, the transistor speed increases enabling higher speed communications and more complex systems. These benefits come at the cost of decreasing inherent device gain, increased transistor leakage currents, and additional mismatches due to process variations. All of these drawbacks affect the design of high-resolution analog-to-digital converters (ADCs) in nano-CMOS processes. To move towards an ADC topology useful in these small processes the K-Delta-1-Sigma (KD1S) modulator-based ADC was proposed. The KD1S topology employs inherent time-interleaving with a shared op-amp and K-quantizing paths and can achieve significantly higher conversion bandwidths when compared to the traditional delta-sigma ADCs. The 8-path KD1S modulator achieves an SNR of 58 dB (or 9.4-bits resolution) when clocked at 100 MHz for a conversion bandwidth of 6.25 MHz and an effective sampling rate equal to 800 MHz. The KD1S modulator has been fabricated in a 500 nm CMOS process and the experimental results are reported. Deficiencies in the first test chip performance are discussed along with their alleviation to achieve theoretical performance.

Outline

- Introduction
- Delta-Sigma Modulation
- Interleaved Delta-Sigma Modulators
- KD1S Modulator Topology
- Test Chip and Results
- Conclusion

CMOS Scaling Trends

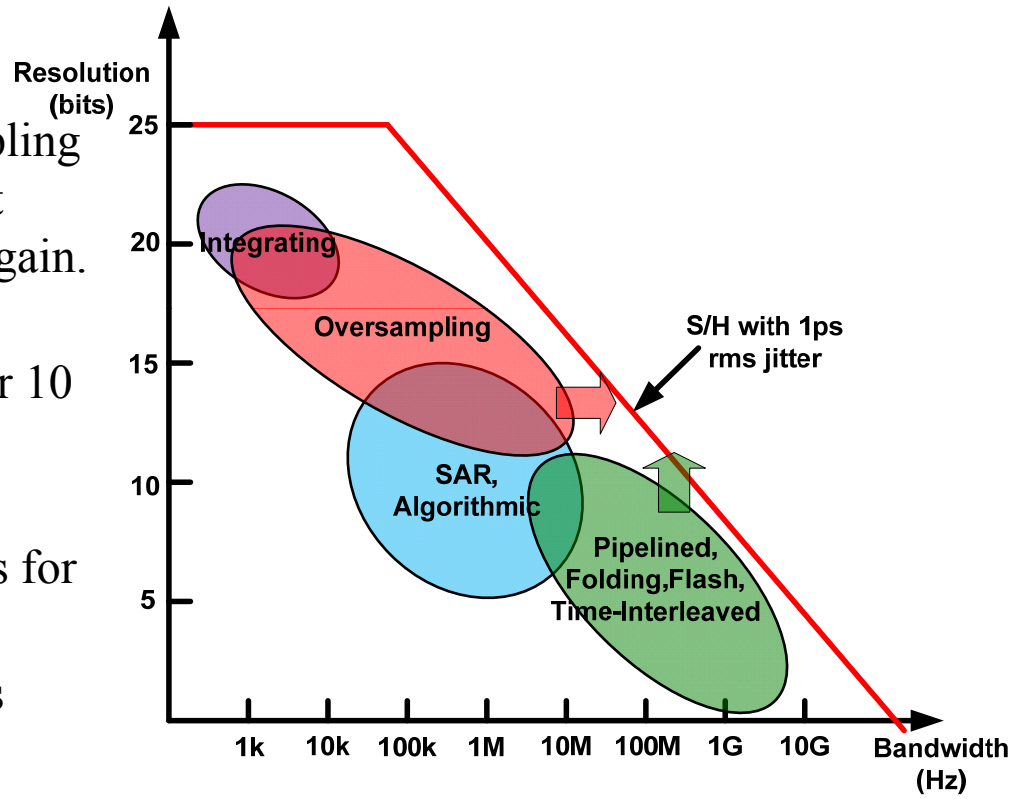




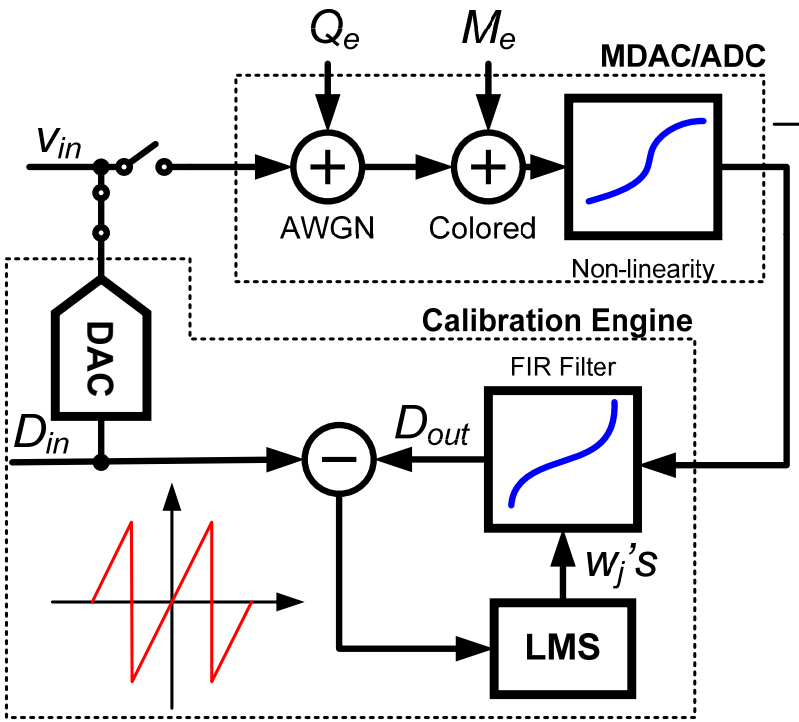
- *VDD* is scaling down but V_{THN} is almost constant.
  - ✓ Design headroom is shrinking.
- Transistor open-loop gain is dropping (~10's in nano-CMOS)
- Random offsets due to device mismatches. $\sigma_{\triangle VTH} \propto \frac{1}{L \cdot W}$

Analog to Digital Converter Trends

- Different ADC architectures for the signal bandwidth and bit resolution requirements.
- CMOS scaling enables higher sampling speeds but at the cost of component mismatches and reduced transistor gain.
- New wireless applications require higher bandwith (25 MHz) and over 10 bits of resolution.
- Software defined radio (SDR) can always utilize higher sampling rates for high resolution.
- Nyquist rate ADCs reaching 10 bits @500 MHz.
  - ✓ Mismatch and reduced gain in nano-CMOS
  - ✓ Digital calibration required.

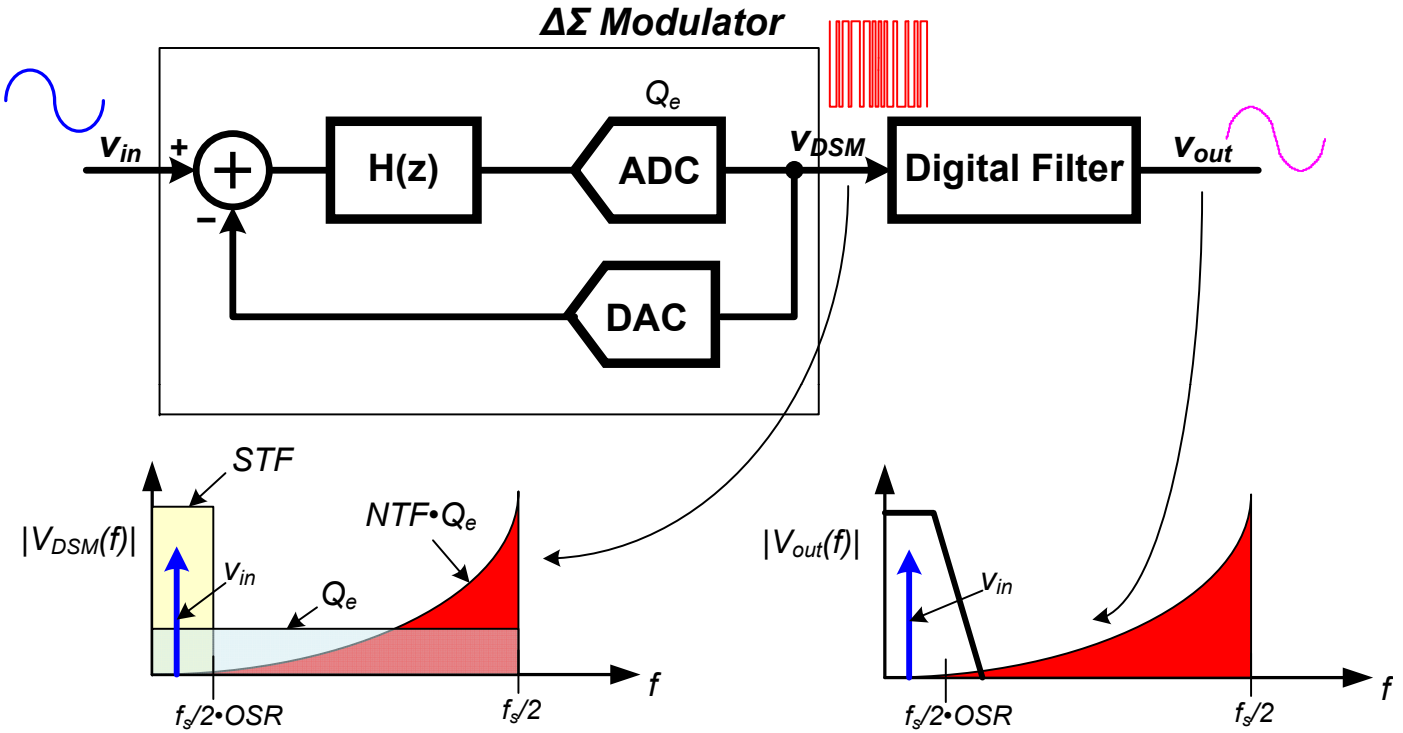


Digital Calibration of ADCs



- Needs a higher precision DAC to adaptively equalize ADC response
  - ✓ DAC runs at slower frequency
    - Calibration may break down at high frequencies and takes time to converge.
- Calibration is only as good as the error modeling!
  - ✓ Promising but cumbersome.
- Not robust with further CMOS scaling and high speed operation.
  - ✓ Need topologies which are inherently robust to mismatches.

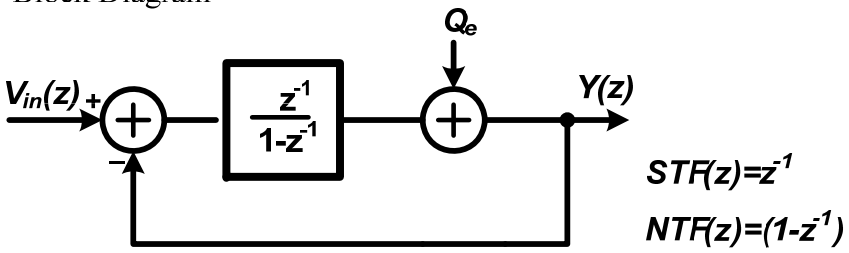
Delta-Sigma (ΔΣ or DS) Modulation



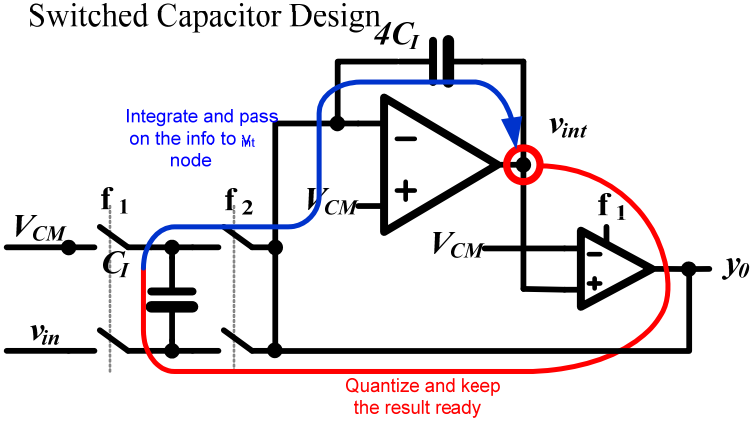
- Use oversampling ($f_s = 2 \cdot OSR \cdot BW$) to shape the quantization noise out of the signal band.
- Digitally filter away the out-of band shaped (modulated) noise.
- Trades-off SNR with oversampling ratio.

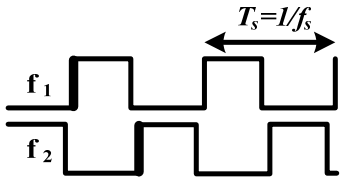
First-Order DSM Review

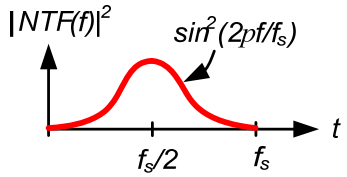
Block Diagram



Switched Capacitor Design







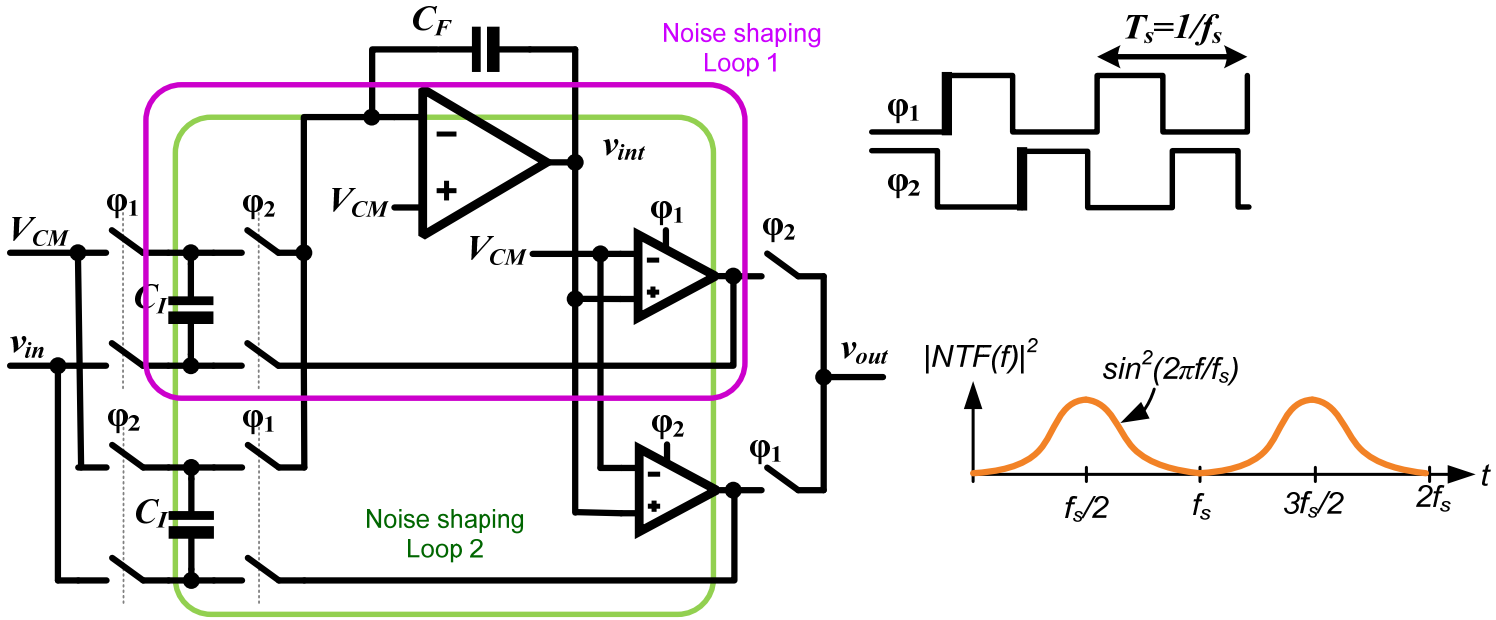
- $Y(z) = z^{-1}V_{in}(z) + (1-z^{-1})Q_e(z)$
  - ✓ Quantization noise is differentiated and pushed out of baseband.
- $N_{eff} = N - 0.566 + 1.5 \cdot \log_2(OSR)$
  - ✓ N is the resolution of the quantizer
  - ✓ $SNR = 6.02N + 1.76 - 5.17 + 30 \cdot \log_{10}(OSR)$
  - ✓ 10 bits for $OSR = 64$ and $N = 1$.
- Feedback structure desensitizes the component mismatches and nonlinearity in the forward path.
- Op-amp can be lower gain ($A_{OL} > OSR$) and lower f_{un}.

DSM for Wideband Data Conversion?

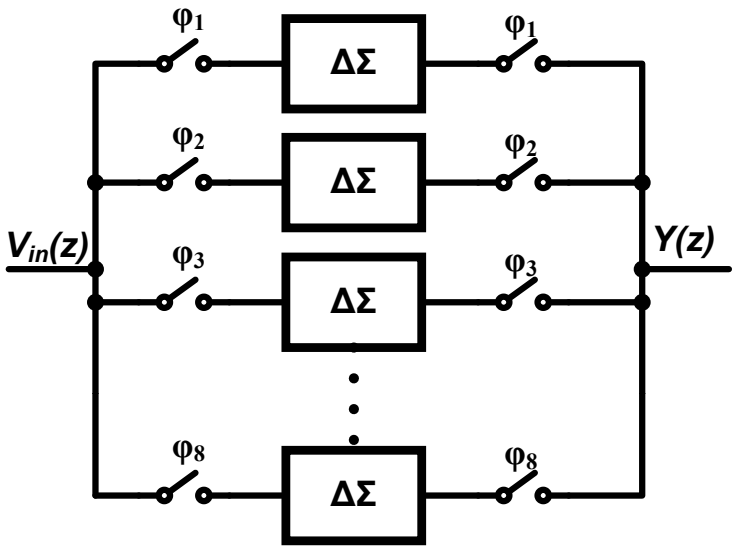
- Delta-Sigma ADC is suitable for nano-CMOS, but it requires oversampling.
  - ✓ Signal bandwith is a fraction of the sampling rate. $BW \leq \frac{f_s}{2 \cdot OSR}$
  - ✗ Not Nyquist-rate sampling as desired.
- Use many DSM's in parallel
  - ✓ Double Sampling
  - ✓ Time-Interleaved/Parallel DSMs.
- Cascade of low-*OSR* DSMs with high sampling rates.

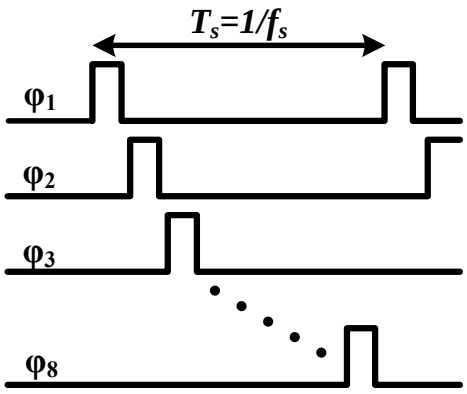
Double Sampling DSM

- Sample input at both the clock phases
  - ✓ Integrator is utilized for both the clock phases.
  - ✓ Can also use a single comparator clocked on both the phases.
- Two noise shaping loops exist, leading to two lobes in *NTF*.
- ✗ Path mismatches lead to folding of noise into baseband.



Time-Interleaved DSM

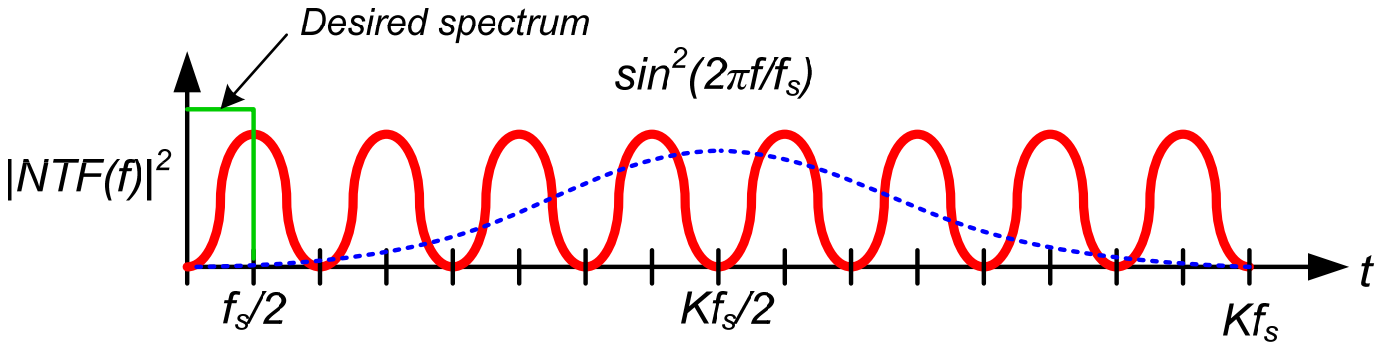




Non-overlapping Clocks

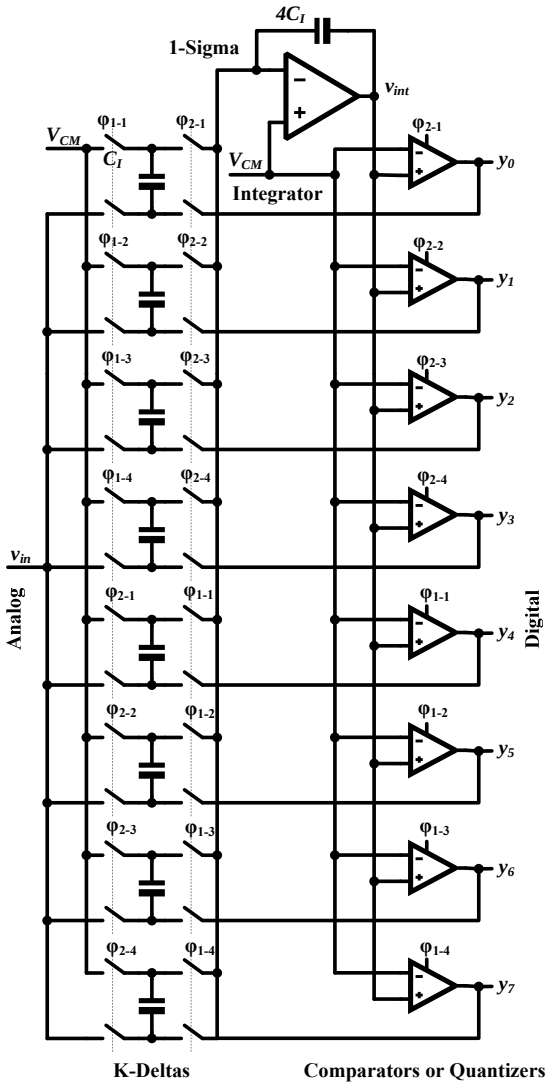
- Use *K* parallel time-interleaved DS Modulators.
  - ✓ Standard technique for Nyquist-rate ADCs.
- K-sets of opamps and comparators
  - × *K*-times power consumption
  - × Large area
  - × Path mismatches will lower SNR and cause spurious tones.
- Does it really behave like a DSM with *K·OSR* oversampling?
  - × No!
- Hadamard-modulation of input can be used to achieve Nyquist rate sampling
  - ✓ Complex digital filters, large area and power.

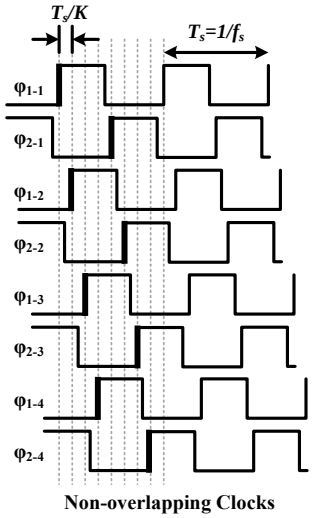
Time-Interleaved DSM: Noise Shaping

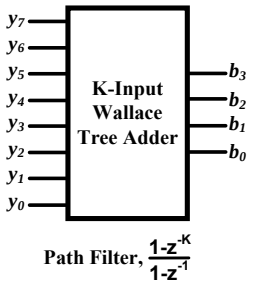


- Ripples in *NTF* with peaks at odd multiples of $f_s/2$.
  - Not true noise-shaping .
  - Only 0.5-bit increase in resolution with doubling in number of paths.
    - $N_{eff} \approx N + (M + \frac{1}{2}) \cdot log_2(OSR) + \frac{1}{2} \cdot log_2(K)$
- The feedback signal in the delta-sigma loop arrives back to the input only after a delay of T_s (= $1/f_s$).
  - Noise shaping looks like a single DSM path.
- True noise shaping only possible when the feedback delay is less than T_s/K.
  - DSMs don't quite stack up like Flash or pipelined ADCs due to the feedback structure.

K-Delta-1-Sigma Modulator (KD1S)

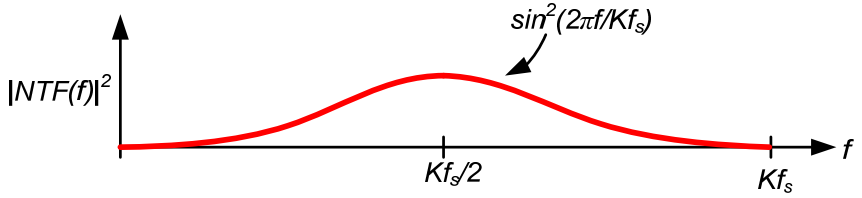






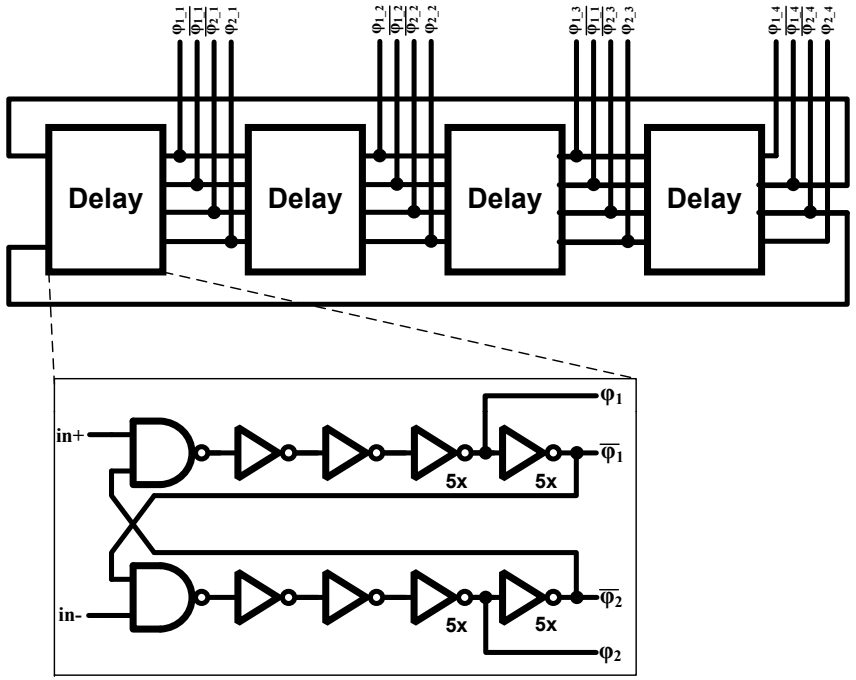
- Share the op-amp across *K*-paths to realize a *K*-Delta-1-Sigma (KD1S) topology.
- Initially assume ideal components:
  - ✓ Comparators settle in $\frac{T_s}{2K}$ time.
  - ✓ Integrator $f_{un} \gg K \cdot f_s$
- Thus the error signal $v_{in}[n] - Y[n]$ is cycled through the integrator within T_s/K duration.
  - ✓ True first order noise shaping.

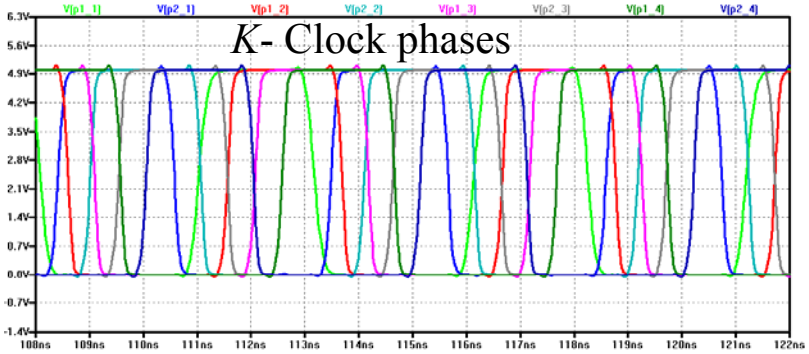
$$N_{eff} = N - 0.566 + 1.5 \cdot log_2 (K \cdot OSR)$$



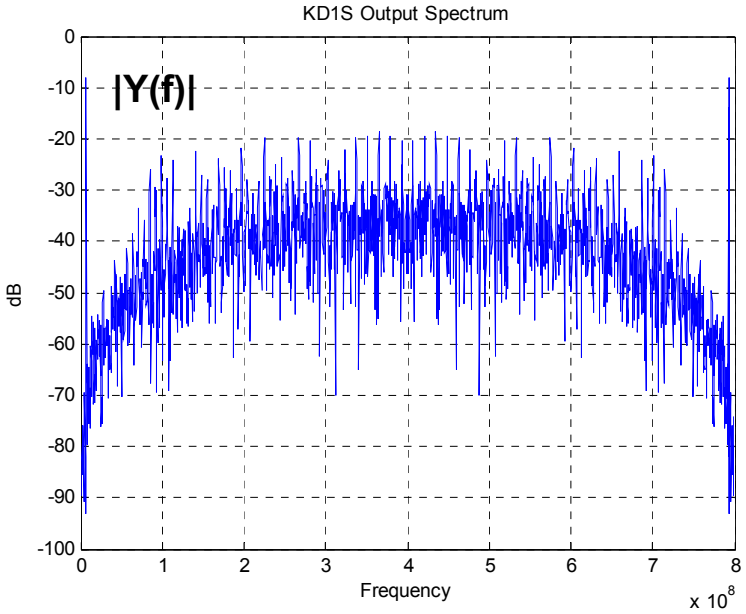
Clock Generation

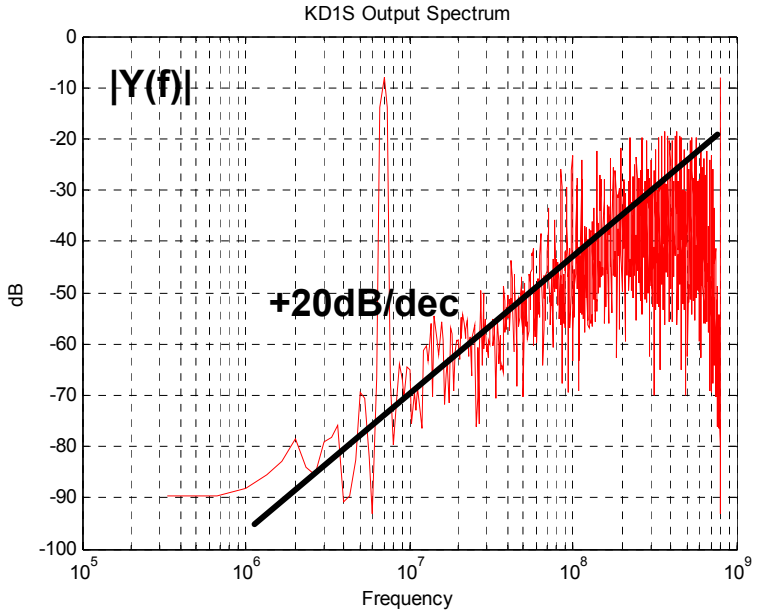
- Ring oscillator is used to generator the *K* clock phases and their complements.
  - ✓ GHz sampling rates as the rate is set by the clock edge spacing.
- A DLL can also be used for low jitter clock phase generation (using an external reference clock).





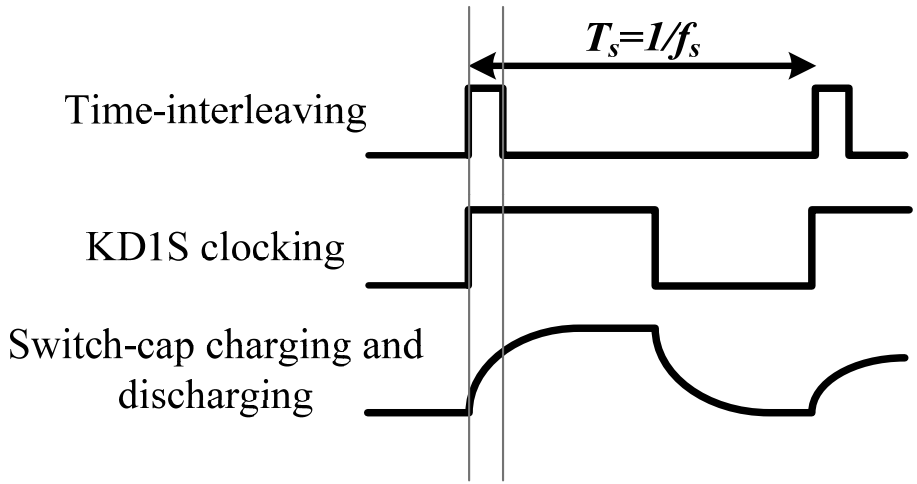
KD1S Simulation





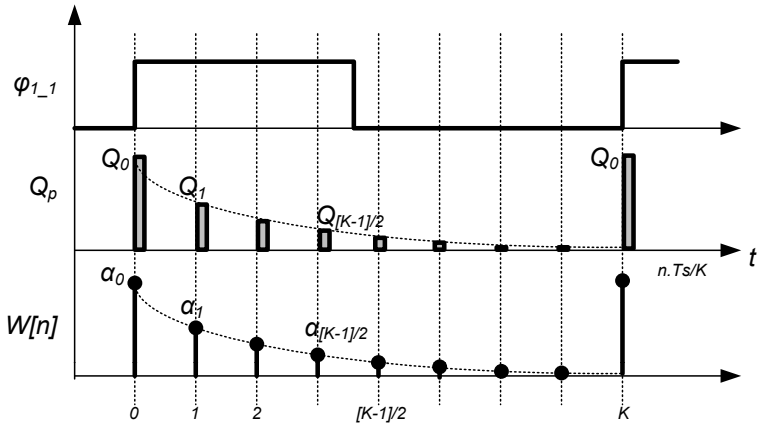
- N = 1-bit, K = 8, OSR = 8, f_s = 100 MHz, $f_{s,new} = K \cdot f_s$ = 800 MHz.
- $$BW = \frac{f_{s,new}}{2K \cdot OSR} = \frac{800MHz}{2 \cdot 8 \cdot 8} = 6.25MHz$$
- SNR = 54 dB, N_{eff} = 9 bits.
  - ✓ Ideal first-order noise shaping.

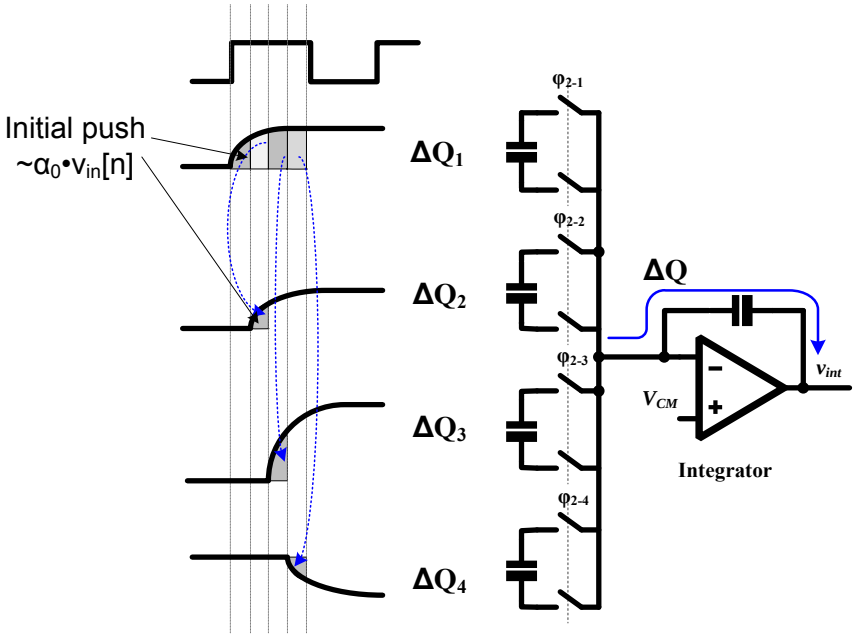
KD1S with Non-ideal Components



- Use a slow op-amp ($f_{un} \approx 3f_s$)
  - ✓ Each integrating path takes $T_s/2$ time to fully settle.
  - ✓ Signal spreads into other paths due to the clocking scheme.
- Finite comparator speed.
- Effective sampling frequency ($f_{s,new}$) is only limited by the comparator speed and not the op-amp f_{un}
  - ✓ Significant speed and power benefits!
- Note that, an equivalent single-path DSM with require opamps with $f_{un} \geq 3K f_s$

Charge Spreading



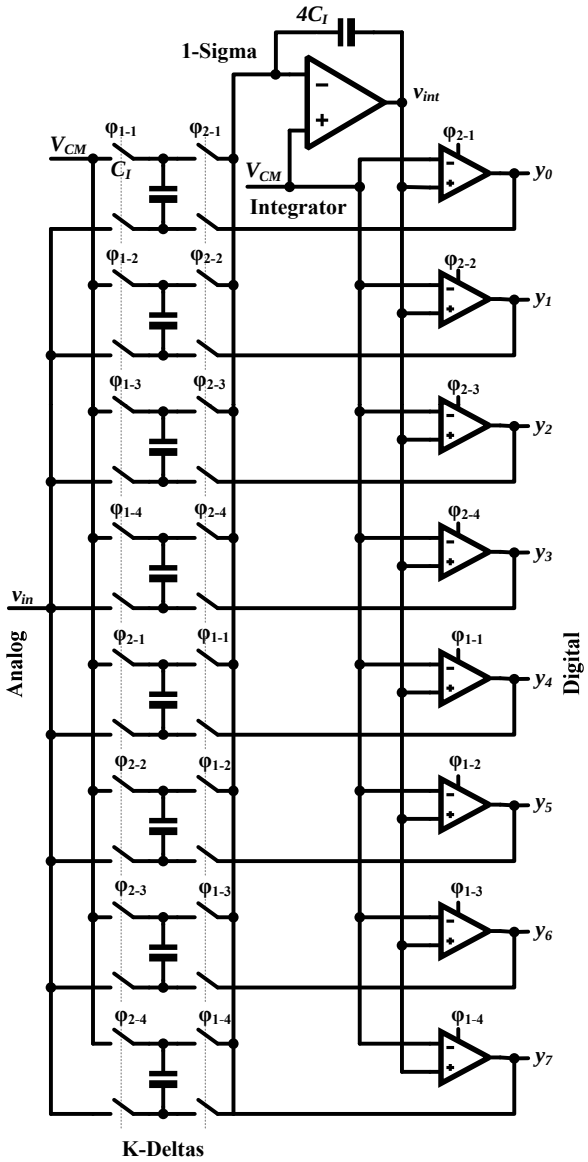


- Each path settles over $T_s/2$ duration.
- At any instance $K/2$ switch capacitors are connected to the integrator.
  - ✓ Charge from path-*i* leaks into path-*j*.
- The impulse response of the block is convolved with the charge spreading filter

$$W(z) = \sum_{n=0}^{\infty} \left(\frac{3}{4}\alpha_0\right)^n z^{-n} = \frac{(1-\alpha_0)}{\left(1-\frac{3}{4}\alpha_0 z^{-1}\right)}$$

where $\alpha_0 = \left(1 - e^{-\frac{\beta f_{un}}{f_s}}\right)$ is the partial settling factor (initial push) of the integrator.

KD1S with Non-Ideal Op-amp

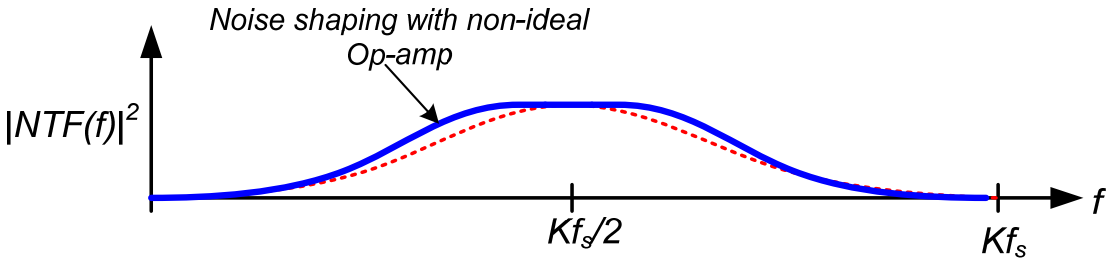


- The theoretical result for the K-path Integrator are plugged into the KD1S Modulator:

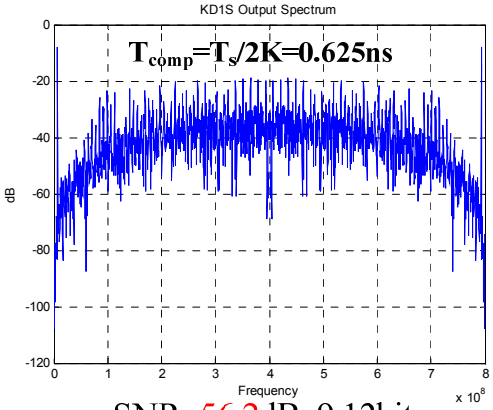
$$NTF(z) = \frac{1}{1+H(z)W(z)}$$

$$STF(z) = \frac{H(z)W(z)}{1+H(z)W(z)}$$

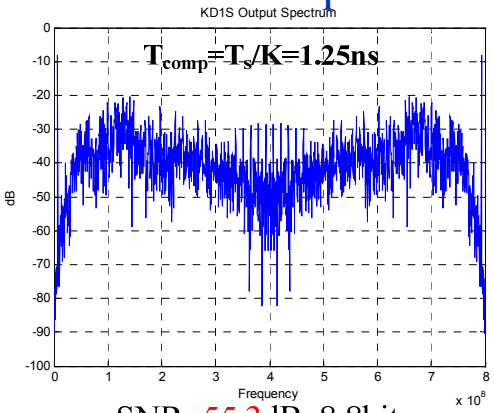
- Worst case loss of ~1-bit resolution over ideal KD1S



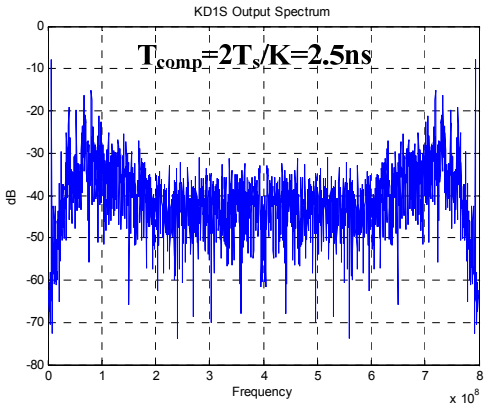
KD1S: Effect of Comparator Delay (T_{comp})



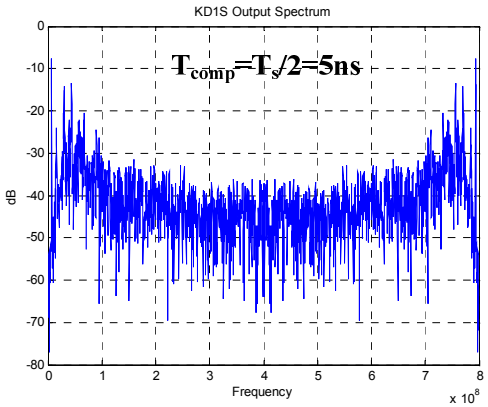
SNR=56.2dB, 9.12bits



SNR=55.3dB, 8.8bits



SNR=43dB, 6.8bits

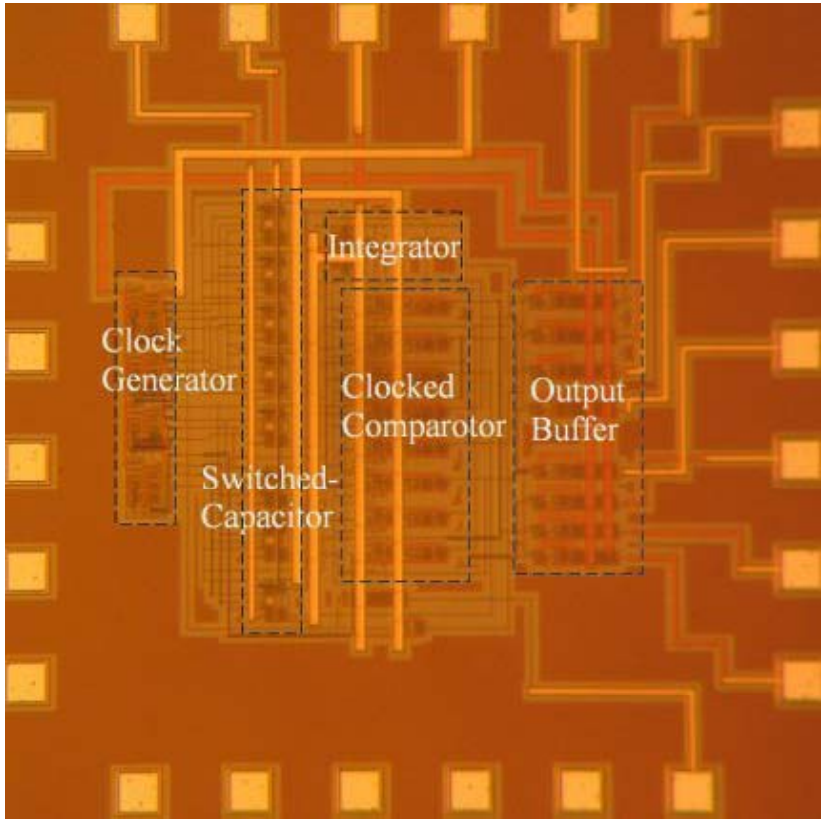


SNR=37.5dB, 6bits

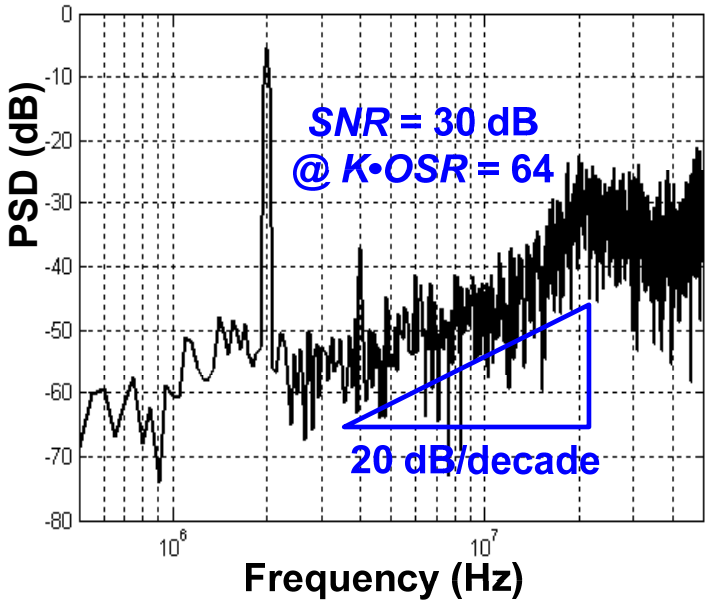
- For true noise-shaping in a process the KD1S should be clocked such that $\frac{T_s}{2K} \geq T_{comp}$
- The resulting bit resolution decreases with an increase in comparator delay.
  - ✓ Resolution drops from 9-bits to 6-bits as we increase T_{comp} from $T_s/2K$ to $T_s/2$.

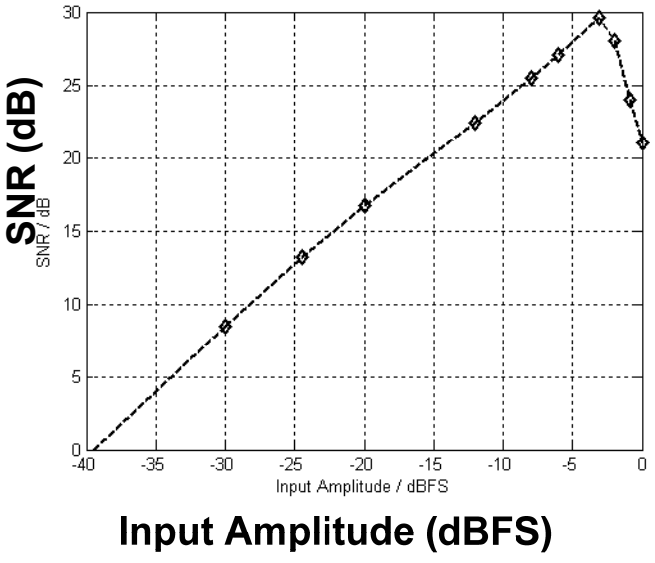
KD1S Test Chip

- KD1S Modulator design in 500 nm CMOS process.
- 8-path outputs registered on a 100 MHz clock.
  - ✓ $f_{s,new}$ = 800 MHz.
- Digital signal processing using Matlab and Agilent MSO7104.



Test Results





- Measured *SNR* for a 2 MHz, 4 $V_{p\text{-}p}$ input tone, and BW = 6.25 MHz
  - ✓ **SNR = 30 dB,** N_{eff} = 5 bits
  - ✓ Proof of Concept: First order wideband noise-shaping achieved.
- Performance lower than expected:
  - ✓ Design mistake in connection of clock phases. Lower op-amp gain.
  - ✓ Rectified in subsequent designs.

KD1S vs. Single-path DSMs

- Why use interleaving rather than a fast single-path modulator?

KD1S topology (and its higher order extensions) employ inherent interleaving to :

- ✓ achieve comparable (or better) performance than CT-DSMs.
- ✓ have the desirable properties of DT-DSMs like frequency scalability and clock jitter tolerance.
- ✓ GHz sampling possible as Opamp gain-bandwidth limitations are eliminated.
- ✓ Modulator can be clocked as fast as the comparator can respond without any stability concerns.

Comparison of KD1S with DT- and CT-DSMs

	Discrete-time DSM	Continuous-time DSM	K-Delta-1-Sigma Modulator
Output code rate	fs	fs	$f_{s,new}=Kf$s
N_{inc}	$(M + 0.5)\cdot \log_2(OSR)$ where M = DSM order	$11.5 + 0.5 \cdot \log_2(OSR)$	$(M + 0.5) \log_2(OSR \cdot K) - 1$ for $f_s = 1/(2T_{comp})$
Opamp f_{un} requirements	2.5fs to 5fs (90% to 99% SC settling)	$\geq f$s	3fs $\approx f_{s,new}/3$ (95% settling in $T_s/2$ interval)
$f_{s,max}$ limited by	Opamp f_{un}: ~$f_T/50$	Excess loop delay and stability: $f_T/20$	Only comparator metastability: GHz sampling
Frequency scalability	Yes	No	Yes
Clock jitter sensitivity	Good	Poor	Good
Process variation	Ratio of C's: <0.1%	RC time constant: 30%	Ratio of C's: <0.1%
Inherent AAF	Yes	No	No
Power Consumption	High	Low	Low
Delay Allocation	Easy	Complicated	Easy
Parallel and Cross-coupled Designs	Possible	Not possible	Possible

Conclusion

- Mismatch calibration is not the panacea for ADC design in nano-CMOS.
- K-Delta-1-Sigma Modulators combine the feedback desensitization of mismatches and inherent interleaving at low-power.
- A first-order noise shaping KD1S topology has been demonstrated.
  - ✓ Easily extended to a second-order KD1S topology.
- Test results for KD1S chip are discussed along with suggested improvements.

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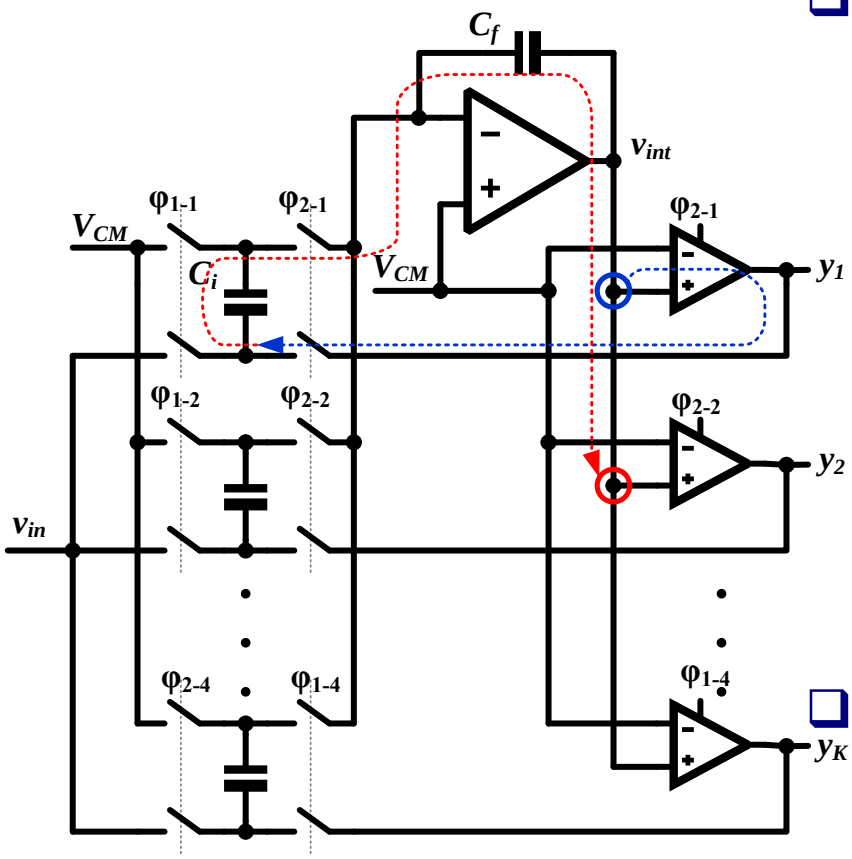
Questions ?

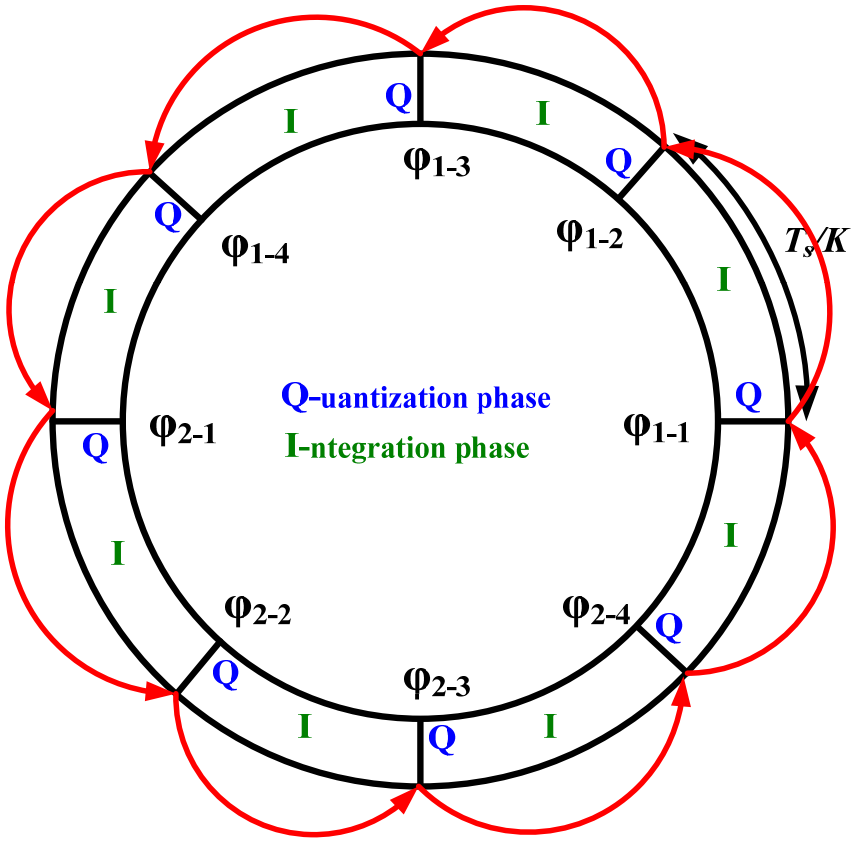
Backup Slides

KD1S – Timing and Charge Flow



- In order to achieve true first order noise shaping (K-times), the chain of noise differentiation should not be broken:
  - ✓ Pick current integrator output (v_{int}), quantize it with comp-1 to get y_1.
  - ✓ This y_1 must be used by path-1 and subtracted from v_{in}.
  - ✓ The result (v_{in}-y_1) is integrated and its result updates v_{int}.
  - ✓ Now path-2 must pick this v_{int} and quantize with comp-2, and so on….
- Always fresh $Q(v_{int})$ information should fed back through the DAC (important!)

Ideal KD1S- Circular Clock Phase Diagram (CCPD)



- A circular phase diagram is a convenient tool to understand the noise flow in a KD1S modulator.
- The arcs represent the cycling of v_{int} info across a path and the integrator forming a loop (T_s/K time):
  - ✓ $v_{int} \rightarrow y_i = Q(v_{int})_t \rightarrow \Delta = vin - y_i \rightarrow v_{int} = \Sigma(\Delta)$
- The arcs show an uninterrupted flow of noise causing differentiation of noise every T_s/K time period.
  - ✓ True first order noise shaping by K-times.