# Design of High-Speed Op-Amps for Signal Processing

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Abstract - As CMOS gate lengths scale to tens of nanometers open circuit gains drop and analog circuit design techniques that minimize the need for good matching become critical. This talk presents techniques useful for implementing high-speed CMOS op-amps for signal processing (e.g. analog-to-digital converters, filters, input receivers, etc.) in nanometer size CMOS. Techniques for biasing, device size selection, topologies, and compensation are discussed. Design examples are presented and used in system level building blocks. The emphasis is on practical design where power, speed, and manufacturability are critical.

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Background and Content

- This talk assumes a background in CMOS op-amp design
  - Biasing using current mirrors
  - Know basics of op-amp design, e.g., compensating two-stage op-amps
  - Calculation of small-signal gains
- The content of this talk is from: *CMOS Circuit Design, Layout, and Simulation, Second Edition,* Wiley-IEEE, 2005.
  - http://cmosedu.com (for the book's figures and simulation netlists)
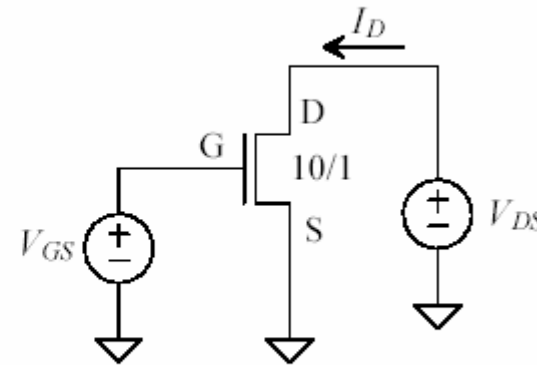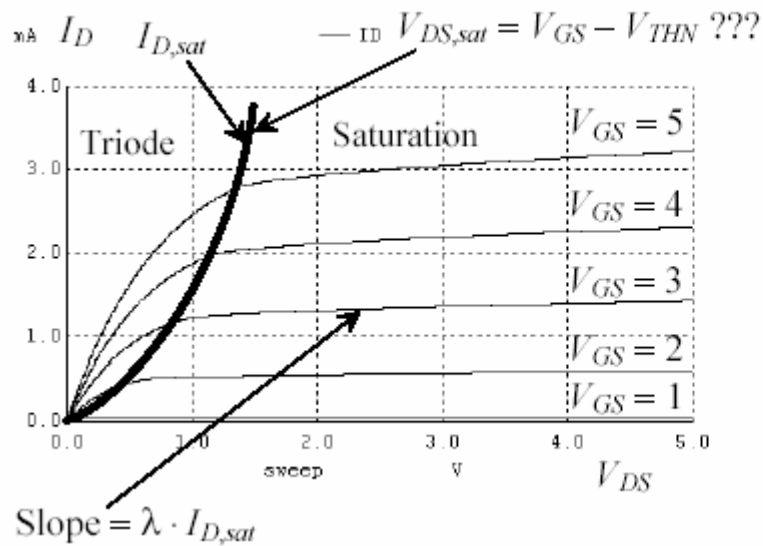

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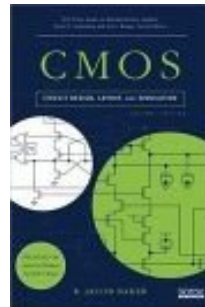
Design with nm devices (here we use a 50 nm process)
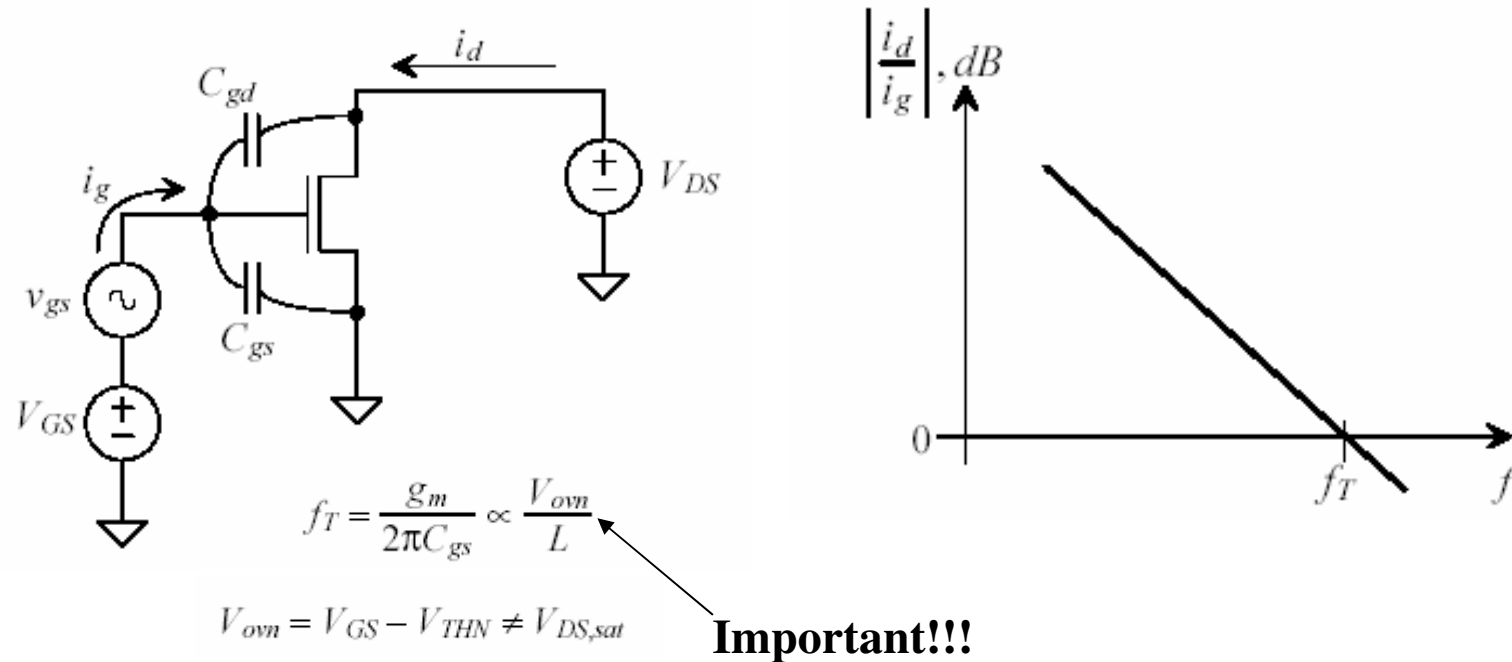
- **Key points**
  - Devices do not follow the square-law equations (so don't use them)!
  - Nanometer CMOS is characterized using:
    - On current
    - Off current
    - VDD
    - Gate oxide capacitance
    - Plots of measured data (note equations can't be used; too complicated for hand calculations).

Long Channel IV curves

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Transition frequency

- FOM (figure of merit) for CMOS amplifier design

$$f_T = \frac{g_m}{2\pi C_{gs}} \propto \frac{V_{ovn}}{L}$$

Important!!!

$$V_{ovn} = V_{GS} - V_{THN} \neq V_{DS,sat}$$

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Biasing for high speed

- Must use minimum length devices
  - Matching becomes even more important
- Larger overdrive results in faster circuits
  - Drawback is that the devices enter the triode region earlier
- For minimum power use mimimum size devices
  - For nm CMOS minimum (drawn) W is, generally, 10 times minimum L
  - Use for NMOS 10/1 and for PMOS, to match drive, 20/1
- Concerns
  - Is there enough drive using minimum-size devices?
  - Matching!!!

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Examples for general design

- Use 2 to 5 times minimum L (use minimum L for high-speed)
  - Increases open circuit gain (output resistance)
  - Using longer L improves matching
- Use overdrive voltage that is 5% of VDD
  - Increase for high-speed design (say 10% of VDD)
- Table on the next page shows typical parameters for general design

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| Short-channel MOSFET parameters for general analog design $VDD = 1$ V and a scale factor of **50 nm** (scale = 50e−9)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	10 µA	10 µA	Approximate, see Fig. 9.31
W/L	50/2	100/2	Selected based on I_D and V_{ov}
Actual W/L	2.5µm/100nm	5µm/100nm	L_{min} is 50 nm
$V_{DS,sat}$ and $V_{SD,sat}$ V_{ovn} and V_{ovp}	50 mV 70 mV	50 mV 70 mV	However, see Fig. 9.32 and the associated discussion
V_{GS} and V_{SG}	350 mV	350 mV	No body effect
V_{THN} and V_{THP}	280 mV	280 mV	Typical
$\partial V_{THN,P}/\partial T$	− 0.6 mV/C°	− 0.6 mV/C°	Change with temperature
v_{satn} and v_{satp}	110 x 10^3 m/s	90 x 10^3 m/s	From the BSIM4 model
t_{ox}	14 Å	14 Å	Tunnel gate current, 5 A/cm^2
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	25 fF/µm^2	25 fF/µm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	6.25 fF	12.5 fF	PMOS is two times wider
C_{gsn} and C_{gsp}	4.17 fF	8.34 fF	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{gdp}	1.56 fF	3.7 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 µA/V	150 µA/V	At $I_D = 10$ µA
r_{on} and r_{op}	167 kΩ	333 kΩ	Approximate at $I_D = 10$ µA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	25 V/V	50 V/V	!!Open circuit gain!!
λ_n and λ_p	0.6 V^{-1}	0.3 V^{-1}	$L = 2$
f_{Tn} and f_{Tp}	6000 MHz	3000 MHz	Approximate at $L = 2$

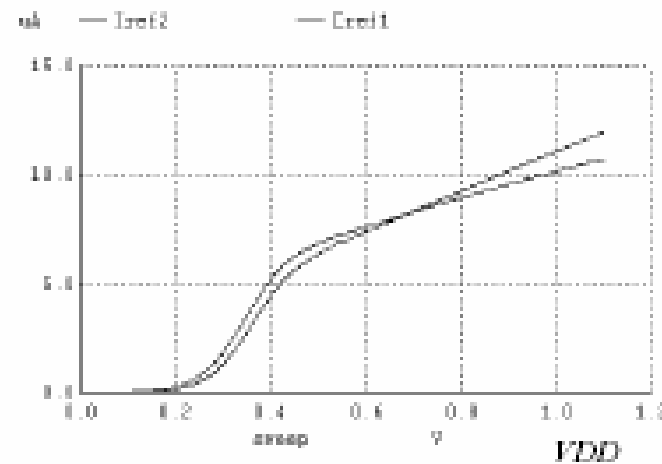Prof. R. Jacob Baker

Bias current (overdrive) and gain
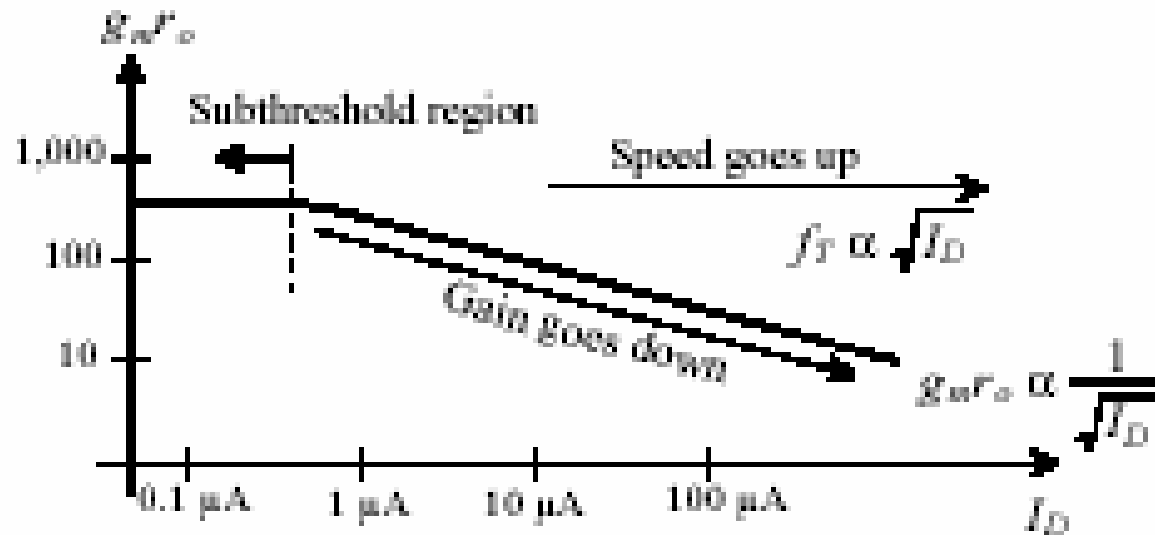
Biasing

- Temperature stability
- Power supply insensitive
- Good variations with process
- Sets the overdrive voltages in the design
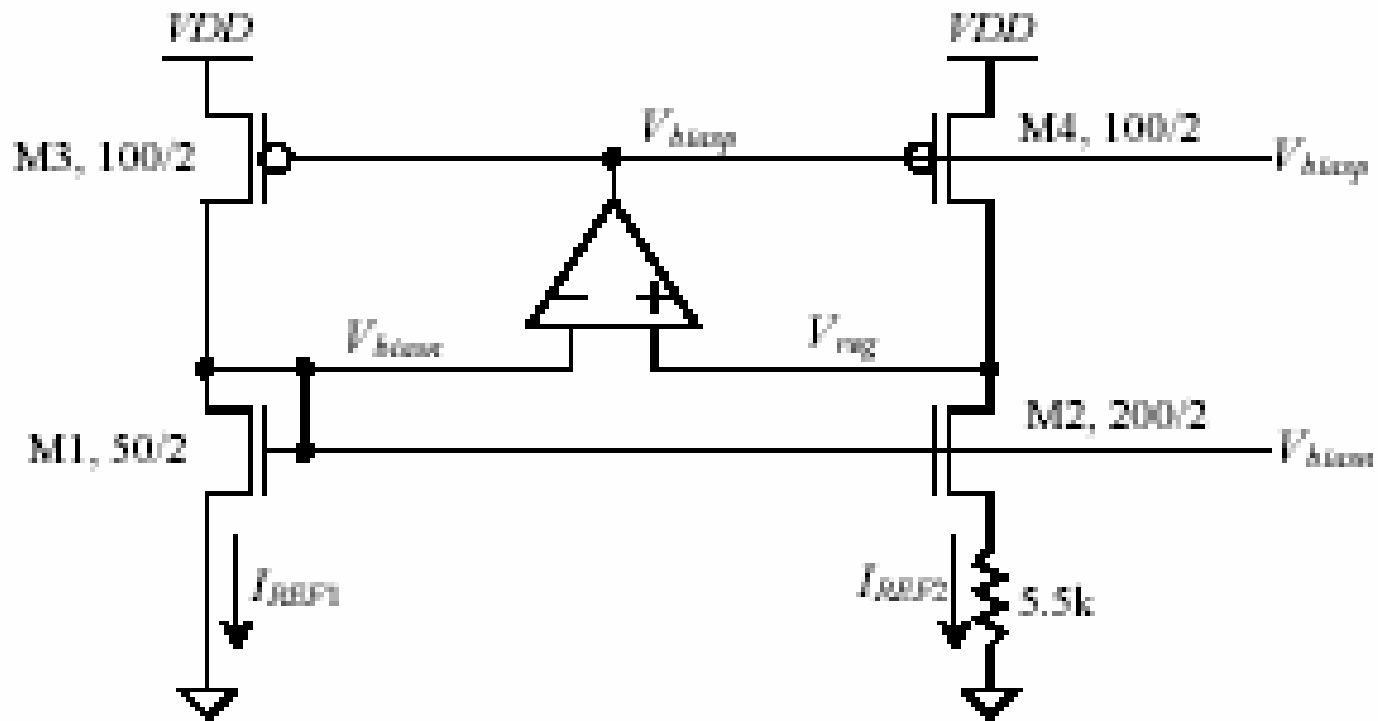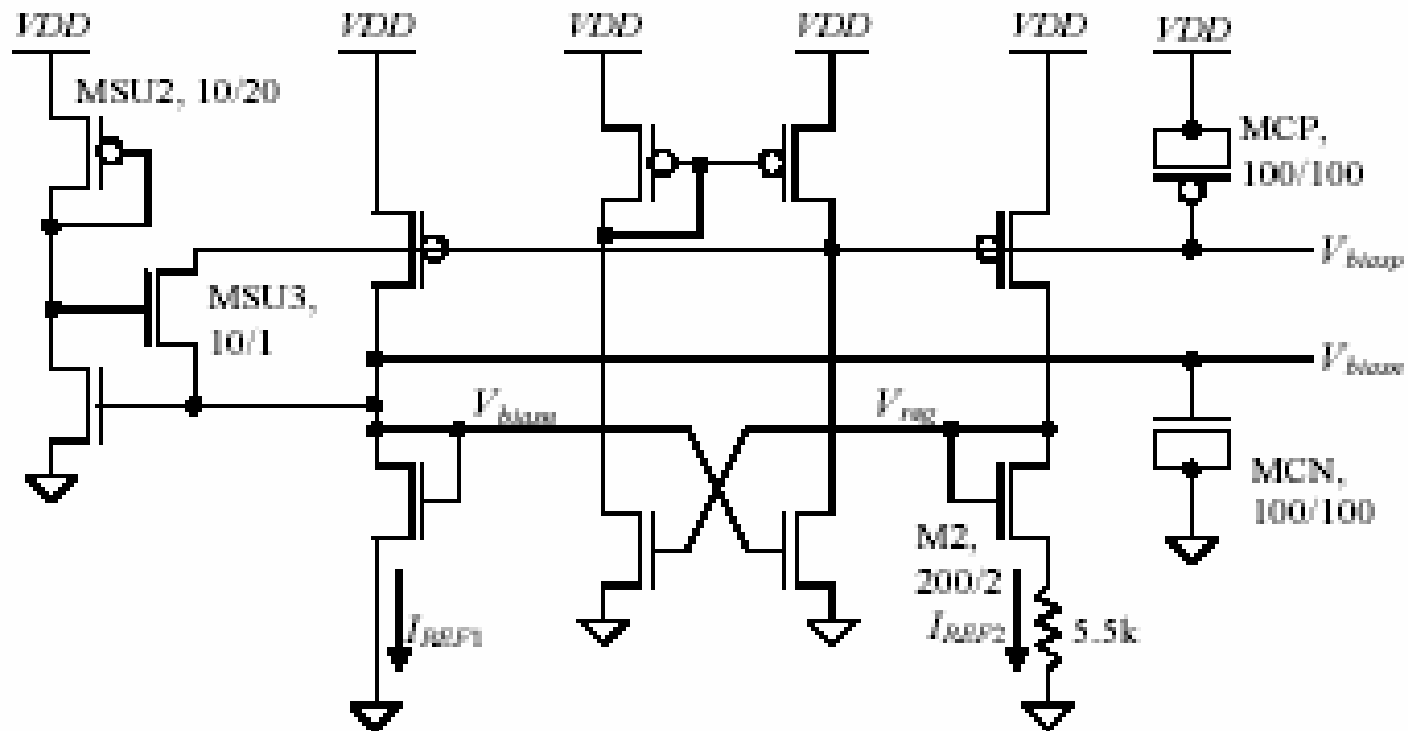- Need a self-biased reference; a beta multiplier reference (BMR)

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Problems with BMRs in nm CMOS

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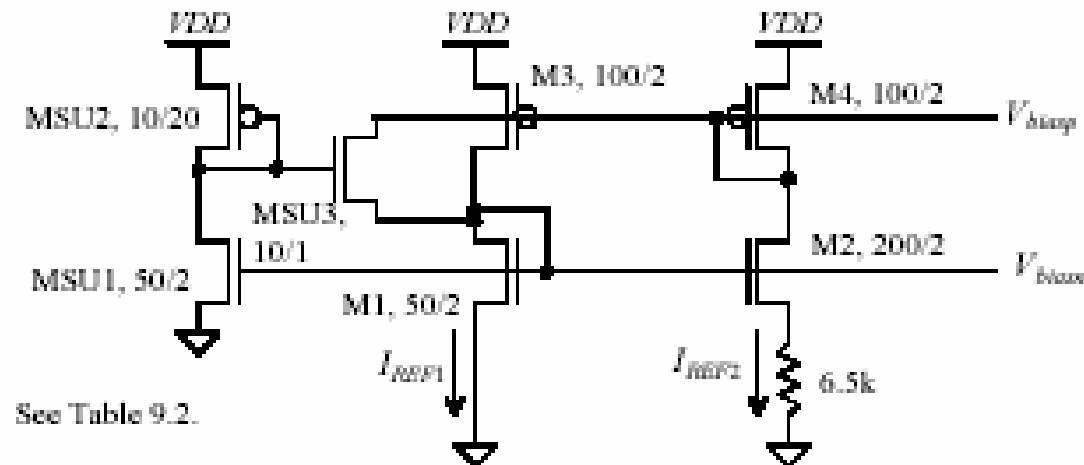
BMR for nm CMOS

Circuit implementation of a BMR in nm CMOS

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Stability is Critical for this design

- Removing the capacitors causes the reference to oscillate.
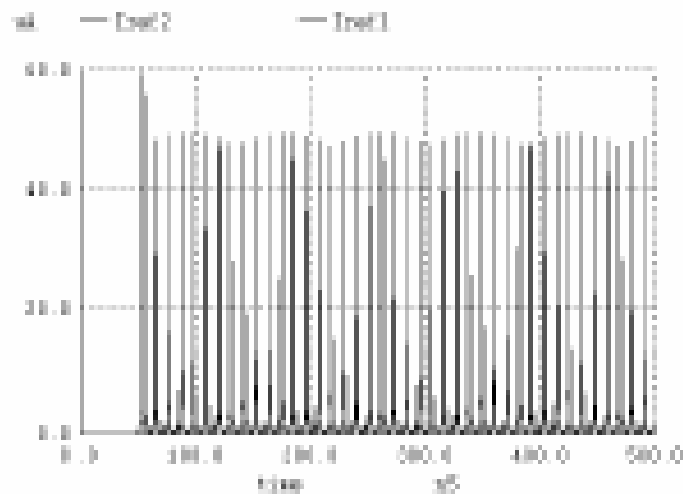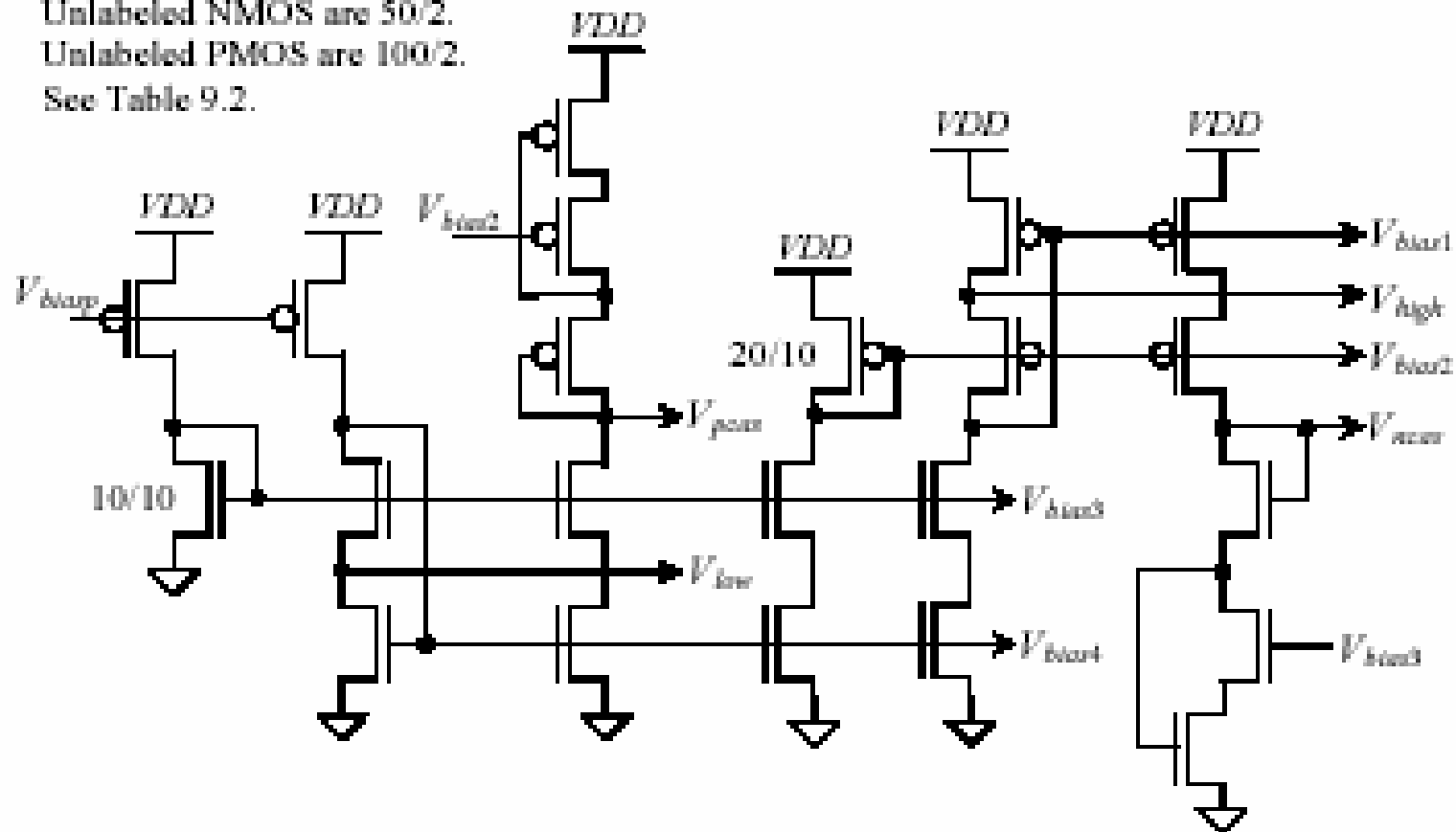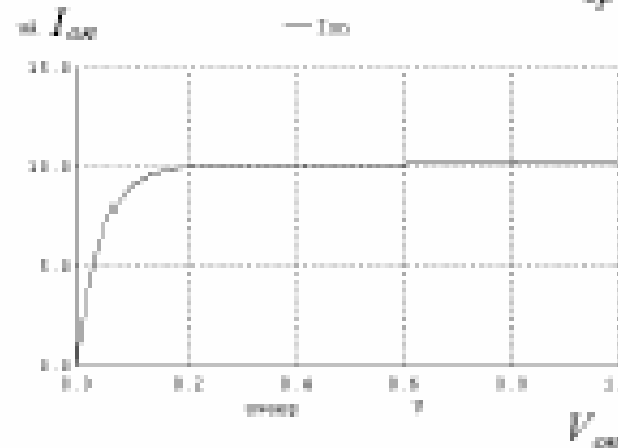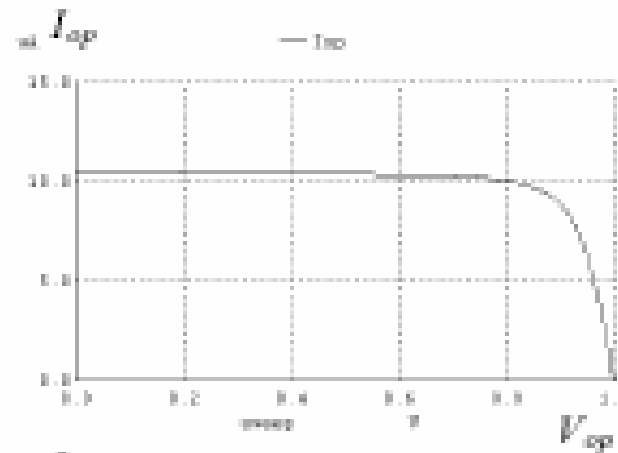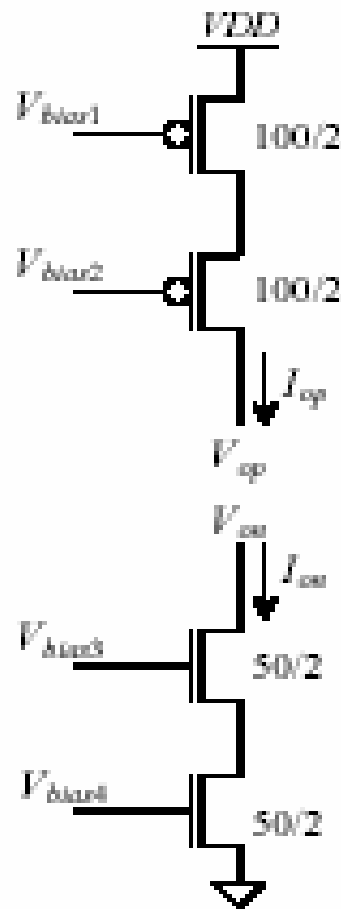

(a) MCP and MCN not present   (b) MCP and MCN present
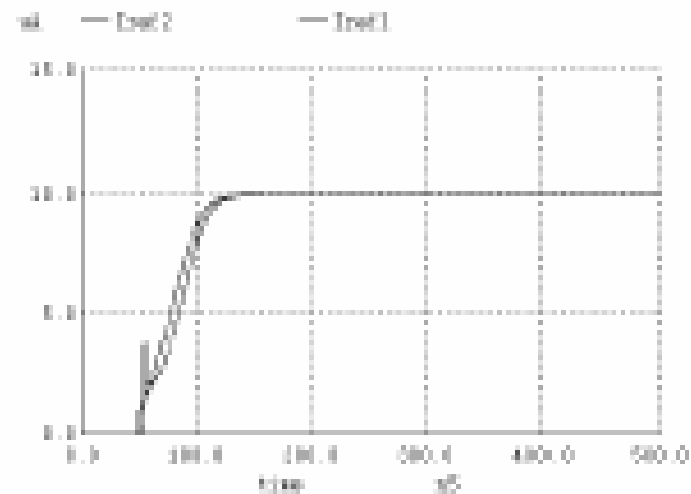
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Generating Bias Voltages for nm Design

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Performance of Cascode Current Mirrors

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Output Buffer with Bias Voltages

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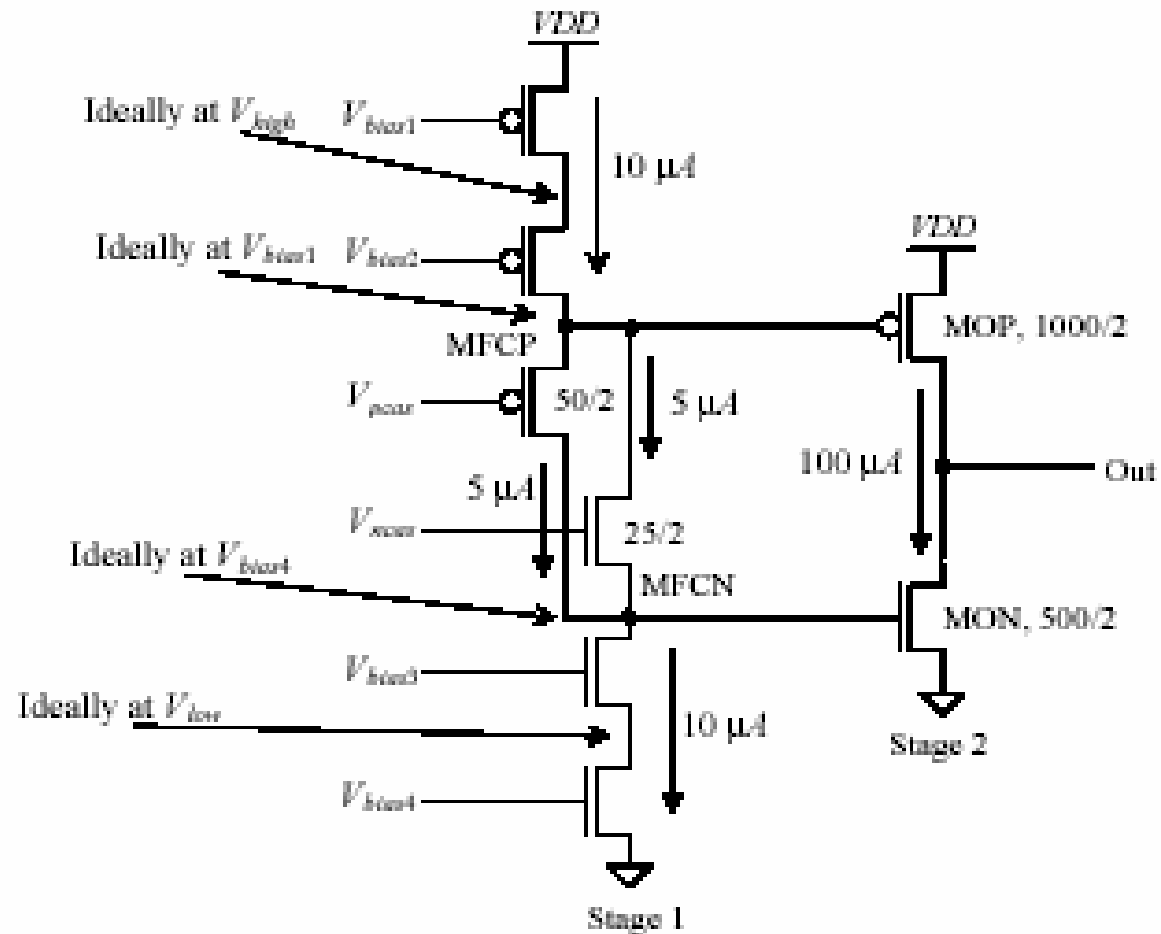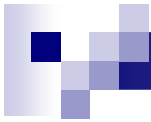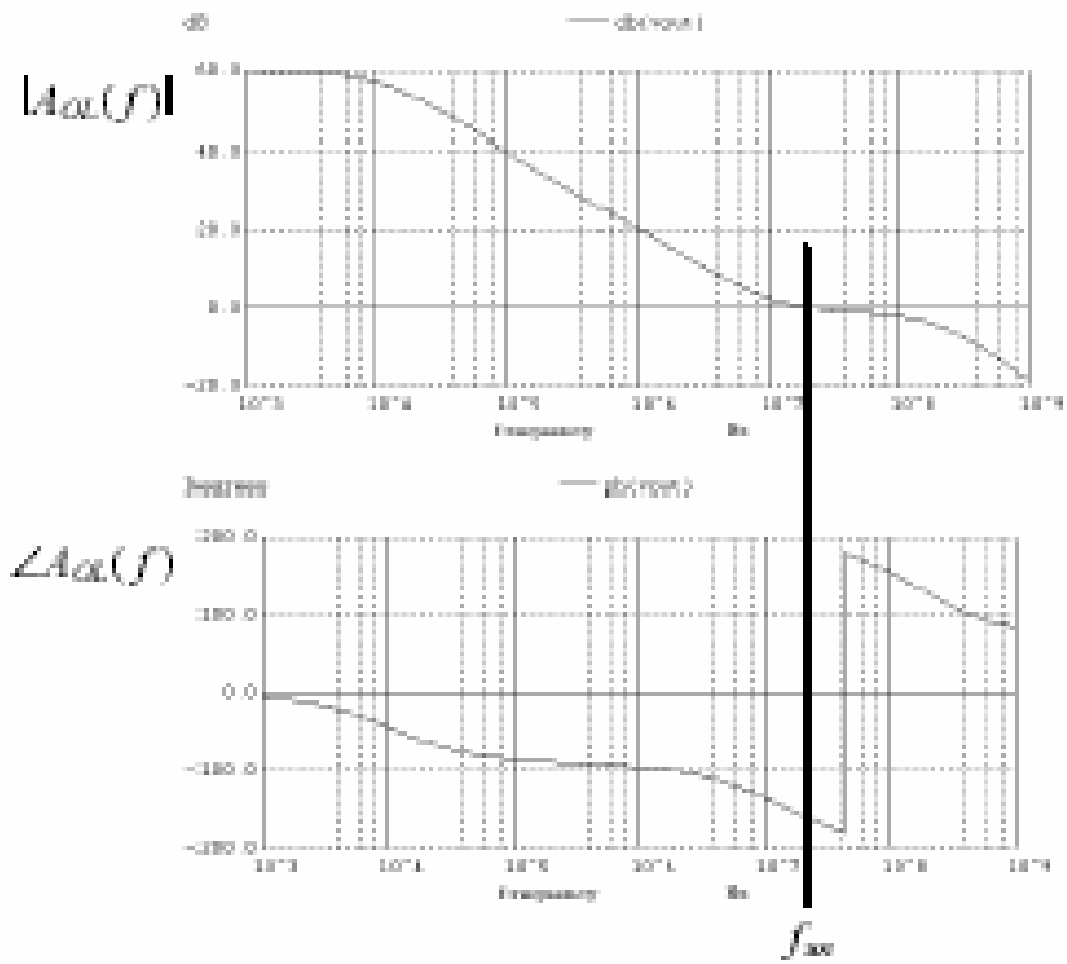
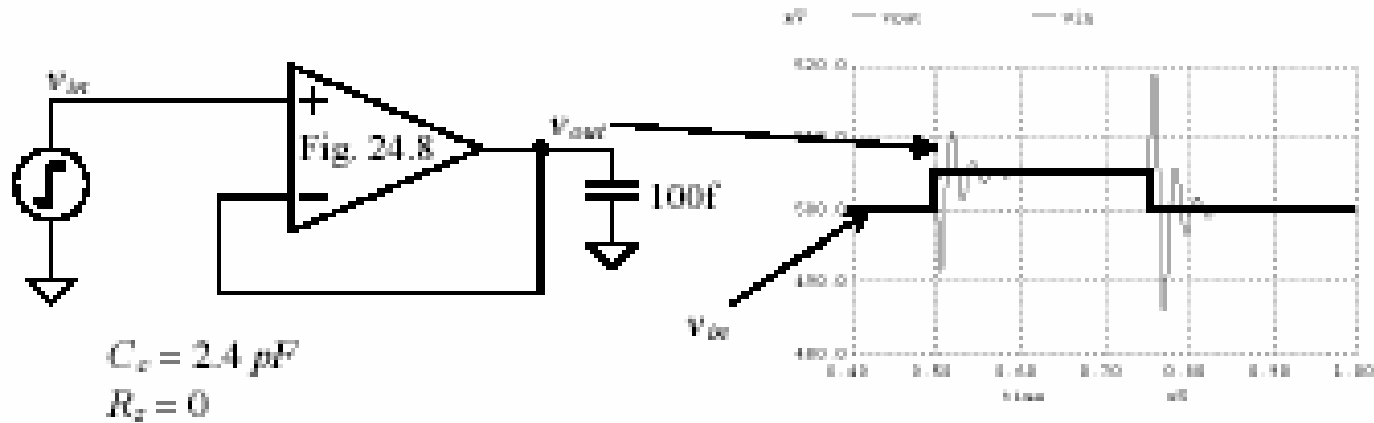# Two-Stage Op-Amp with Miller Compensation

- Simple topology using diff-amp and common-source amplifier
  - Can't drive resistive loads
  - Poor PSRR

- Using Miller compensation
  - Poor PSRR
  - Have that pesky right-half plane zero
  - Slow-speed (unless you use bias with large devices and currents) for a given load C
  - Poor slewing

Example of a bad (academic) op-amp design

Parameters from Table 9.2 with biasing circuit from Fig. 20.47. Unlabeled NMOS are 50/2 and PMOS are 100/2. Scale factor is 50 nm.

Op-amp schematic symbol

AC Response of this bad design with Rz = 0 and Cc = 2.4 pF

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Step response of the bad design

$$C_c = 2.4 \ pF$$
$$R_z = 0$$
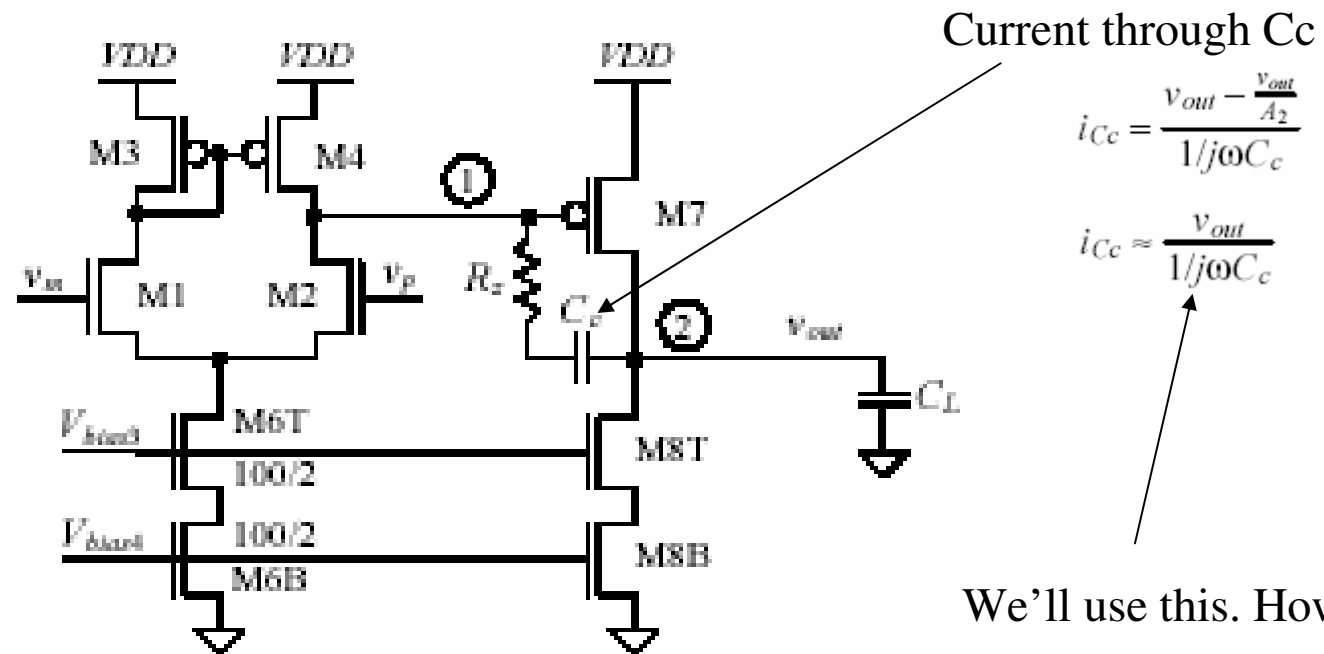
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Making the Op-Amp more Stable

- Obviously we can increase Rz to move the zero into the LHP
  - Controlling the value of Rz becomes challenging over temperature and process

- The stability is becoming a problem because the pole associated with the op-amp's output, f_2 , is too low.

- Increase f_2 by increasing the g_m of the output stage (g_{m2}).
  - Increase widths of the devices so overdrive stays constant (I_D goes up)!
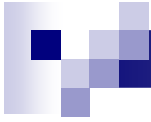 - In general, make sure overdrive voltages are the same in all MOSFETs!

$$f_2 = \frac{g_{m2}C_c}{2\pi(C_cC_1 + C_1C_2 + C_cC_2)}$$

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Practical Way to Compensate an Op-Amp

- Never use Miller Compensation
  - **Never, ever, connect a compensation capacitor between two high-impedance nodes!!! (unless you want slow speed)**
  - The literature is filled with examples of how not to compensate op-amps for high speed operation
- We'll develop **Indirect Feedback Compensation** in the next few pages
  - Practical way to compensate an op-amp
  - Feedback a current indirectly to the output of the diff-amp via:
    - MOSFETs laid out in series (one operating in the triode region)
    - A common-gate amplifier
    - A cascode structure
  - Better PSRR
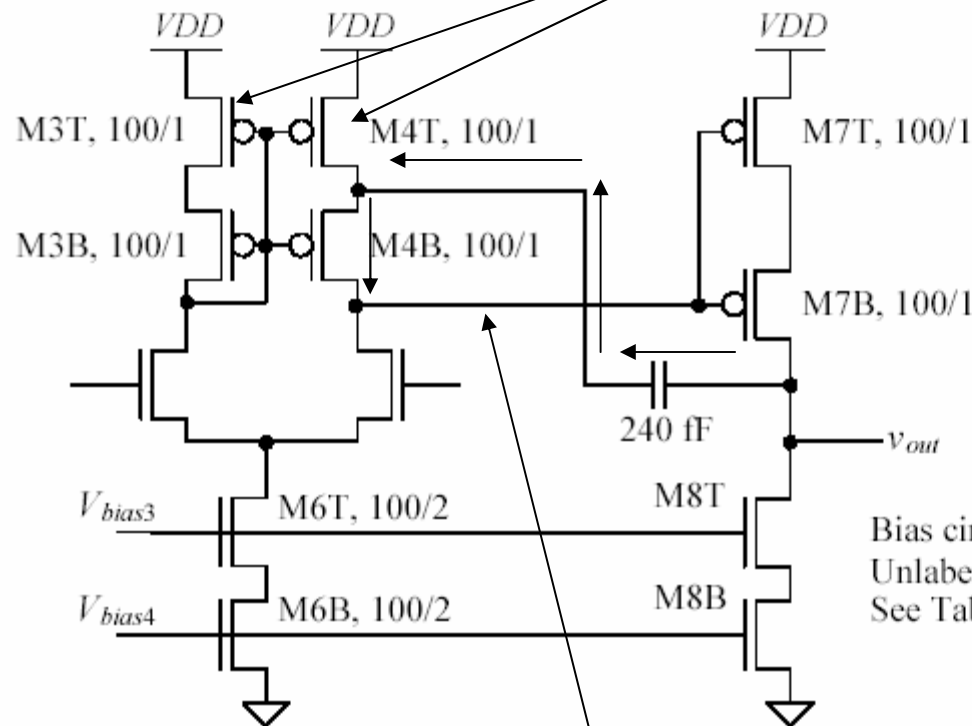 - Smaller layout area (compensation capacitor reduced 4 to 10 times)
  - Much faster!!!

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Indirect Feedback Compensation

Current through Cc

$$i_{Cc} = \frac{v_{out} - \frac{v_{out}}{A_2}}{1/j\omega C_c}$$

$$i_{Cc} \approx \frac{v_{out}}{1/j\omega C_c}$$

We'll use this. How?

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Using Triode Operating MOSFETs

Triode-operating MOSFETs.
100/2 laid out as two 100/1
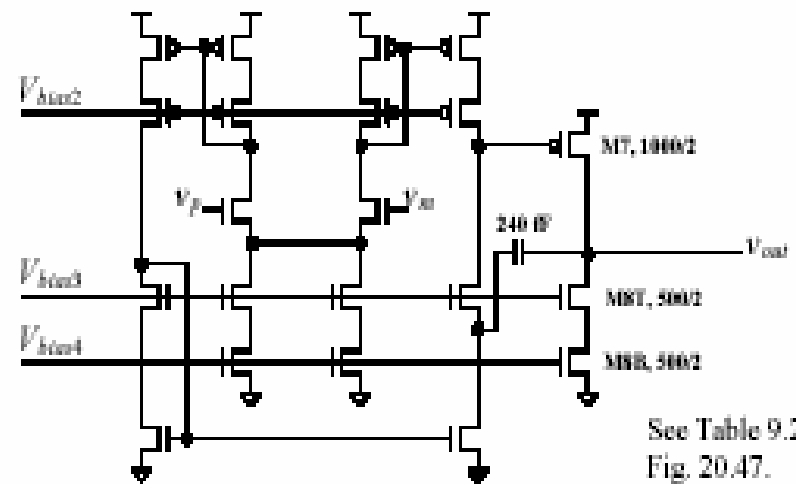
High-impedance node

Bias circuit in Fig. 20.47.
Unlabeled NMOS are 50/2.
See Table 9.2.

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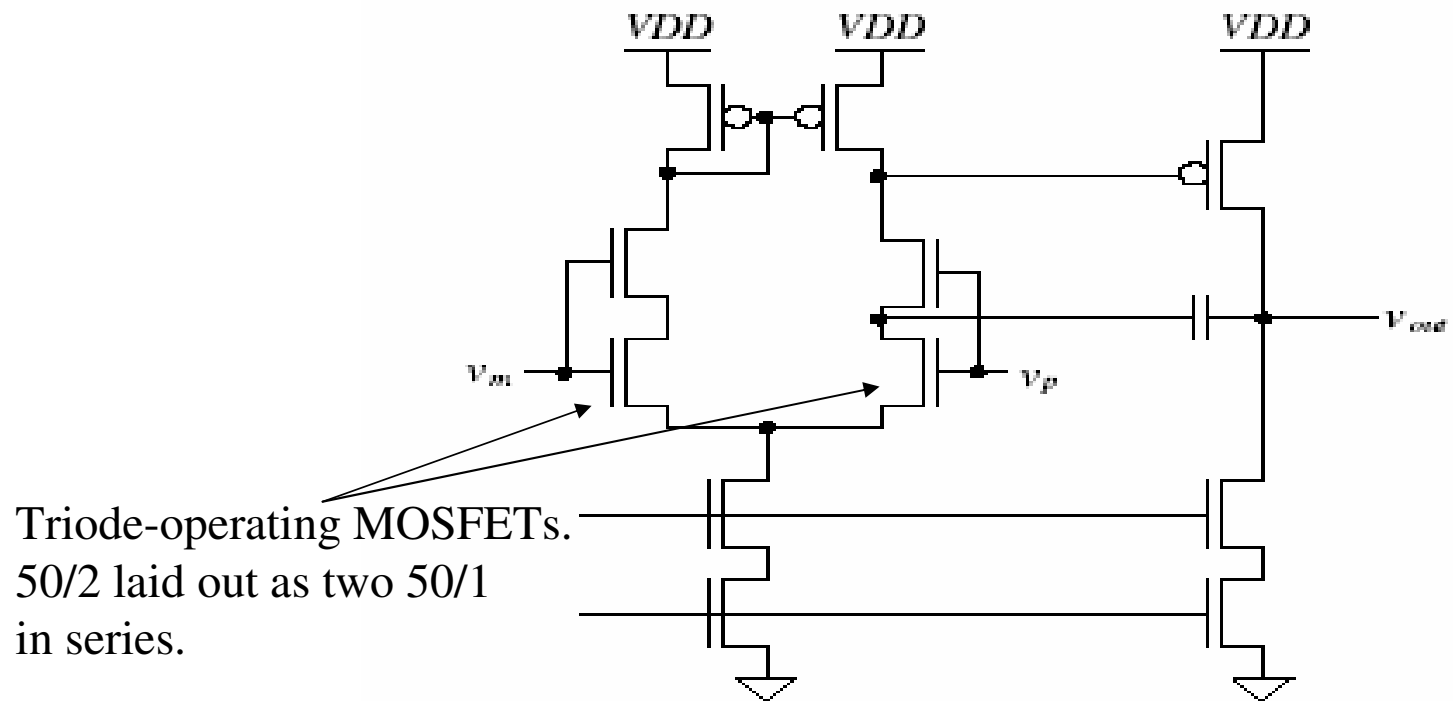
Other examples of Indirect Feedback Compensation
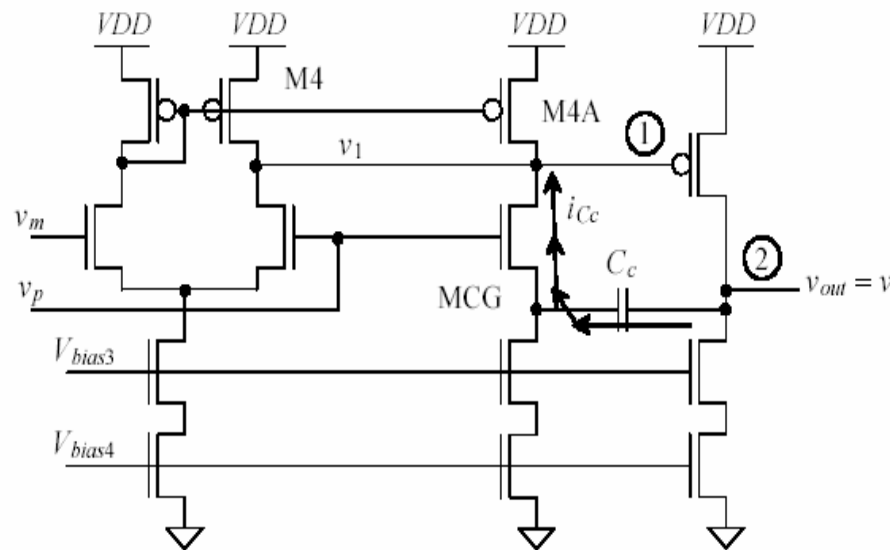
Using a common-gate amplifier

Using a cascode structure

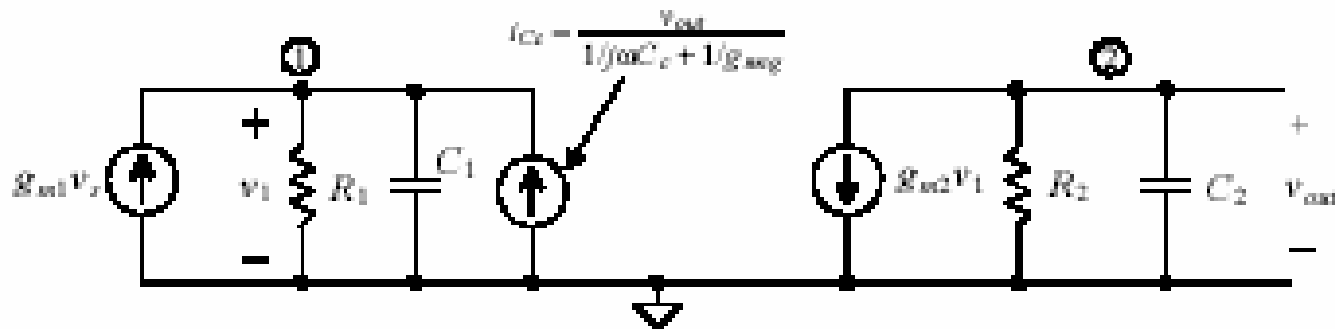See Table 9.2 and Fig. 20.47.

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Other examples of Indirect Feedback Compensation, cont'd

Triode-operating MOSFETs.
50/2 laid out as two 50/1
in series.

Using NMOS triode-operating diff-pair for good PSRR

Equations

$$f_z = \frac{g_{mcg}}{2\pi C_c}$$

RHP zero eliminated. A LHP zero is introduced. The LHP zero increases the phase-margin and speed.

$$f_{un} = \frac{g_{m1}}{2\pi C_c} \quad (\approx f_z \text{ if } g_{m1} \approx g_{mcg})$$

Equation for the unity gain frequency remains the same. However, the value goes up because Cc can drop by 4 to 10

$$f_2 \approx \frac{g_{m2} C_c}{2\pi \cdot C_1 C_2} \approx \frac{g_{m2} C_c}{2\pi \cdot C_1 (C_L + C_c)}$$

Cc drops because load C has less effect on f_2

Example (next page) Two-Stage Op-Amp

- Cascode input stage (sometimes called a telescopic input stage)
- Use a push-pull output stage for rail-to-rail output swing
- Indirect feedback compensation
- > 100 MHz gain-bandwidth product while using 250 μA and a VDD of 1 V (excluding the bias circuit power is 250 μW)
- Excellent PSRR
- Compact layout area

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A Practical General Purpose Op-Amp

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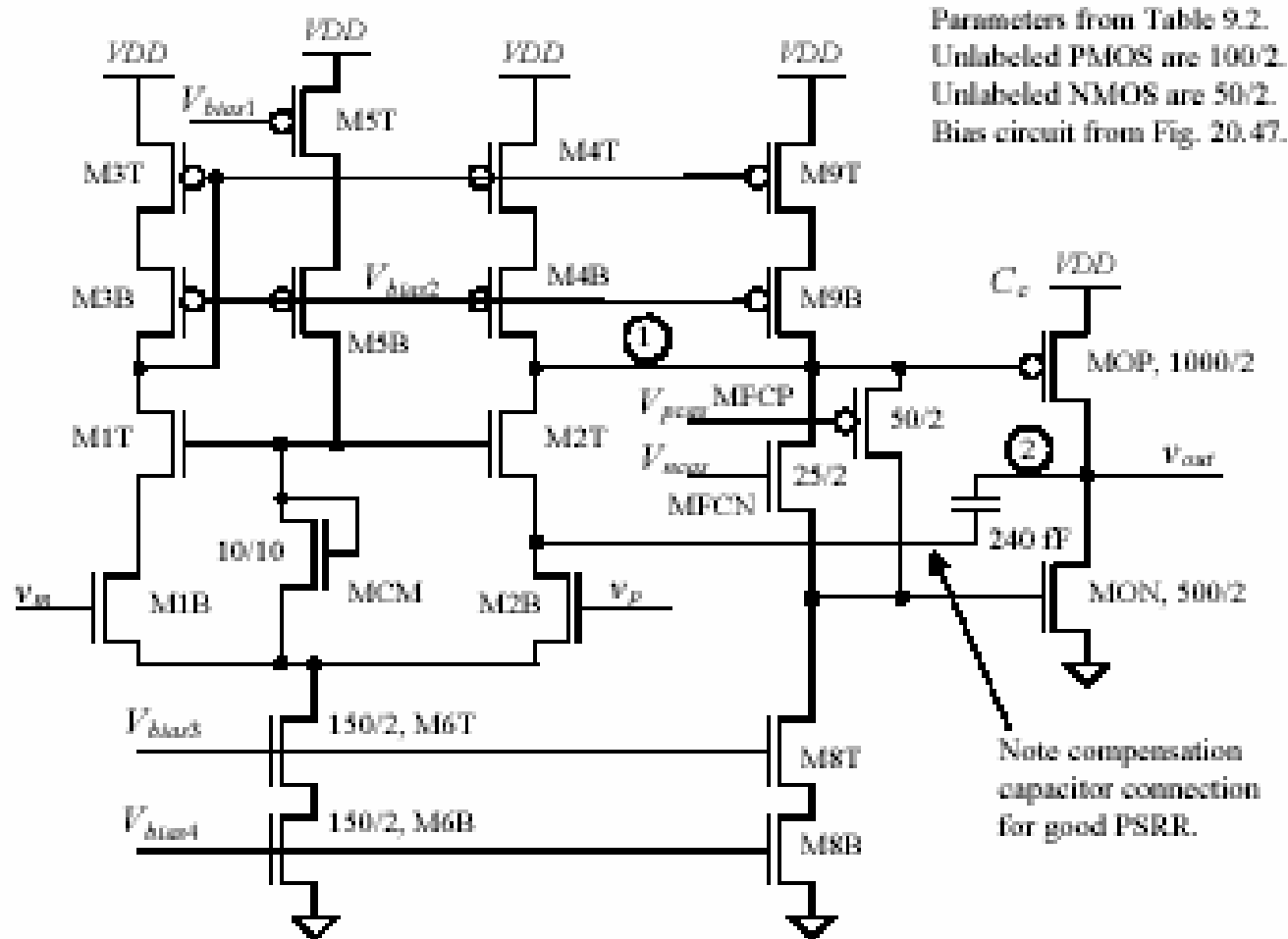
Step Response
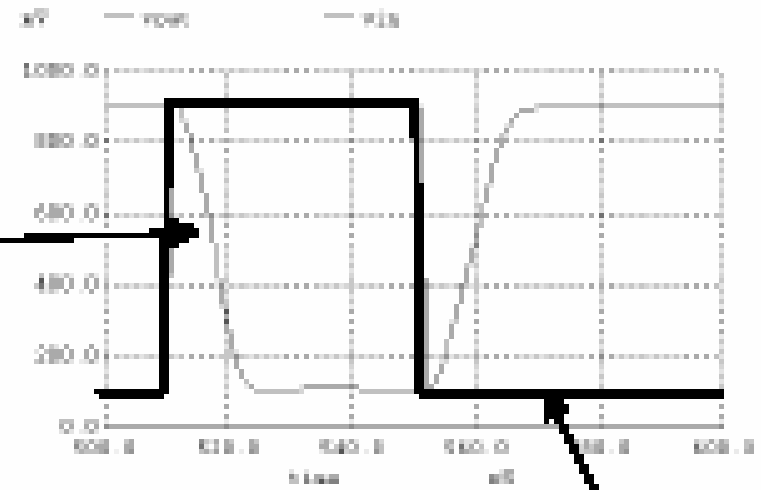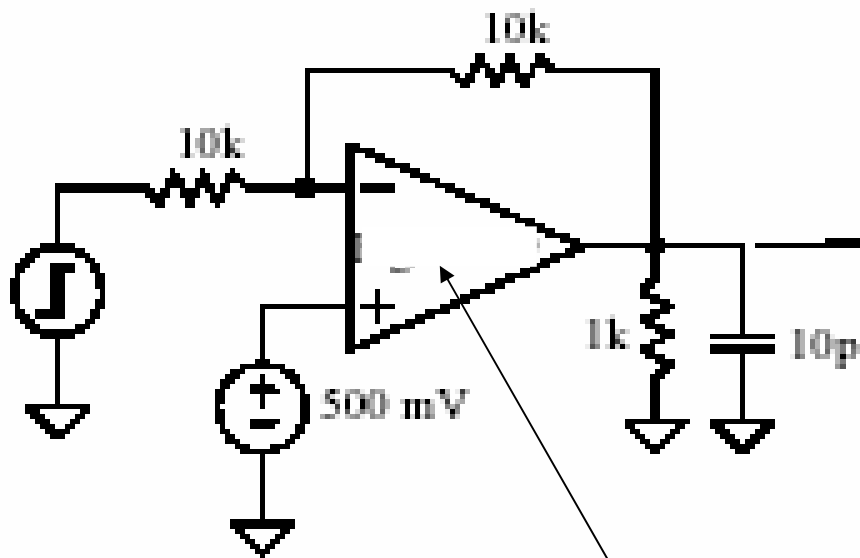
Previous page

Input pulse from 100 to 900 mV.

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Comments

- We were careful to select overdrive voltages for a specific speed (transition frequency)
  - Important to avoid adding a low-frequency pole in the transfer function and thus having a non-optimized design
  - Fiddling with widths while not keeping the overdrive voltages constant is a path to low-quality designs
  - In general, only vary lengths of MOSFETs in DC circuits

- To push f_2 to a higher frequency we increase the widths of the output stage (g_{m2} and current in output stage are increased)

- Reducing C_c causes the gain-bandwidth product, f_{un}, to increase (and move towards f_2).

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Bad Output Stage Design

- Not controlling current in the output stage leads to:
  - □ Bad input-referred offset
  - □ Potential for large power dissipation
  - □ Not controlling output stages gm (and thus stability)
- Don't let SPICE fool you into thinking you can actually set the current in an output buffer without using current mirrors (you can't!)

Example (bad) Output Stages
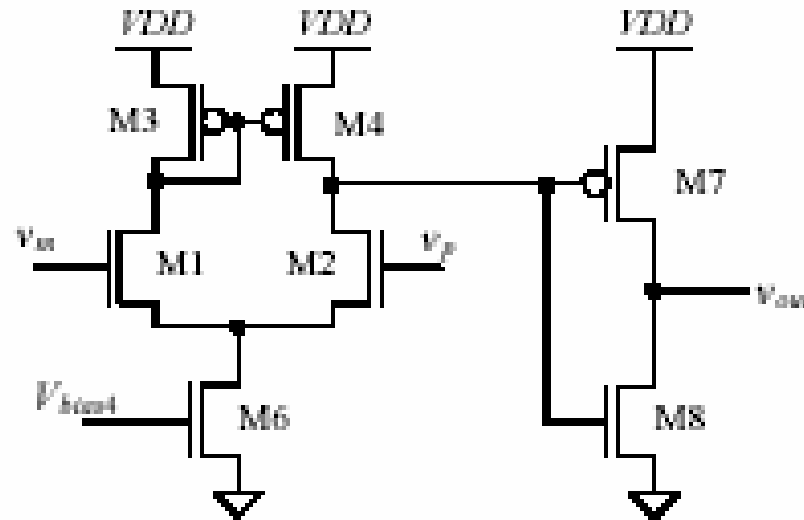
If M7 mirrors current in M4 then M8 triodes and the gain drops.
The gate of M7 will have to drop, with the negative feedback
around the op-amp (so M8 operates in saturation). The result is a
huge current flowing in the inverter output stage.

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Bad Output Stage Design Cont'd

Source-follower level-shifter
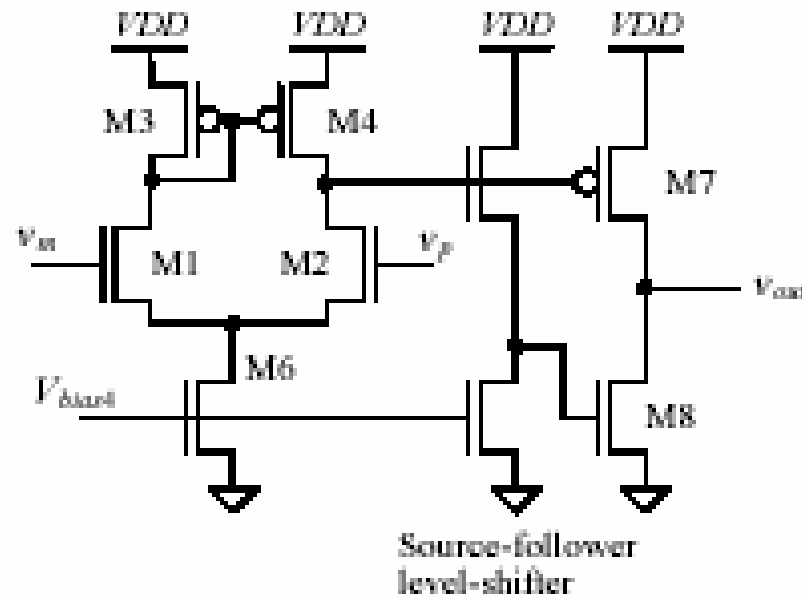
Source follower is used to allow the gate of M8 to drop to a lower voltage so that, hopefully, it can remain in saturation during normal operation. Again, however, we are not controlling the current in the output stage. It may be small, big, or exactly what we want (again, don't let SPICE fool you into thinking this type of design is okay (it's not!)

Bad Diff-Amp Biasing

- Never design a diff-amp where the PMOS current sources fight against NMOS current sources. The outputs will float up or down causing some MOSFETs to triode.

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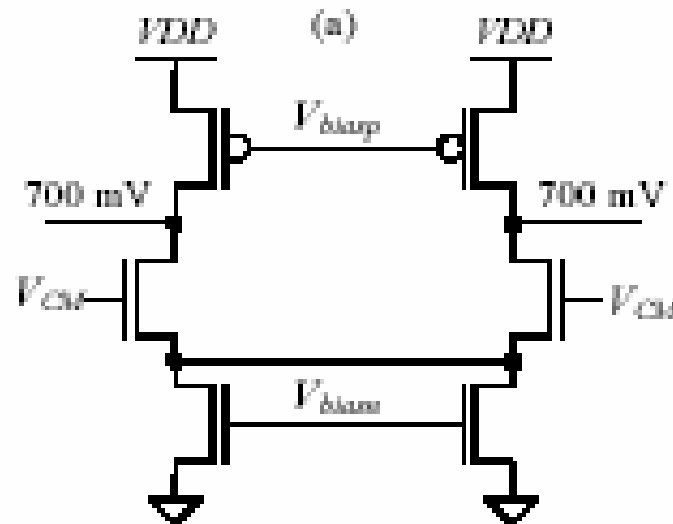
Add Control to a Diff-Amp to Set Currents

- The added control ensures the current sourced by the PMOS equals the current sunk by the NMOS. Controls common-mode output voltage via common-mode feedback (CMFB).


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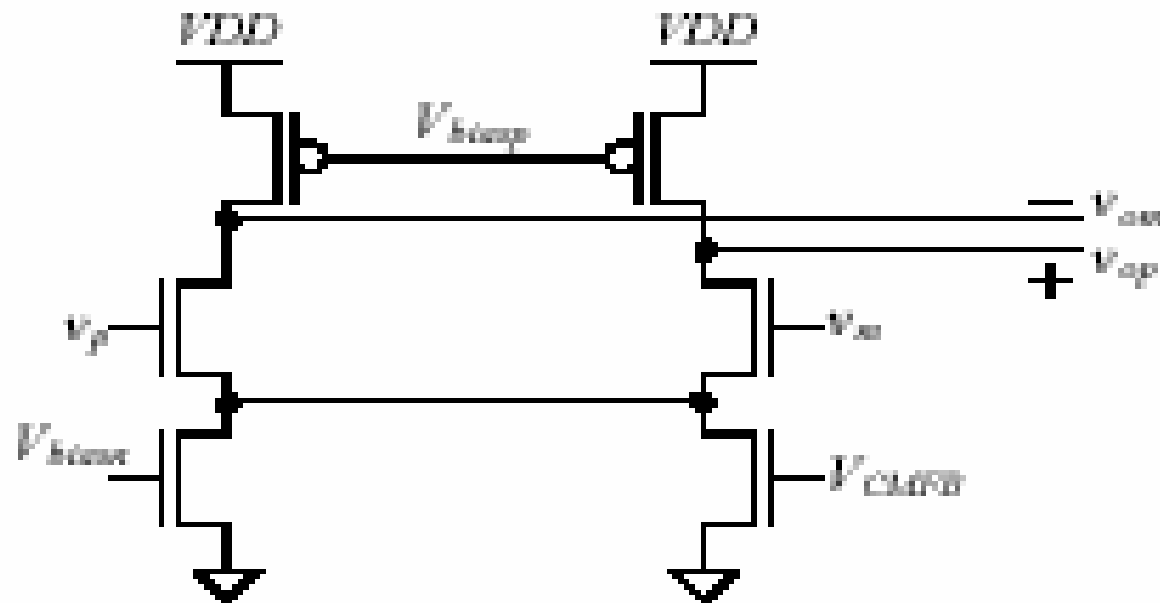
Op-Amps in Signal Processing

- Use fully-differential inputs and outputs
  - Reduces the common-mode noise
  - Need to employ common-mode feedback (CMFB)

- Our examples here will use switched capacitor CMFB and two stage op-amps (for the lowest power and highest speed)

- Fully-differential topologies offer the benefit that class AB output buffers can be implemented without floating current sources
  - Don't need the additional bias circuits

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Basic Fully-Differential Op-amp

PMOS are 20/1
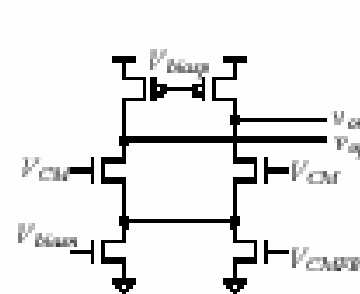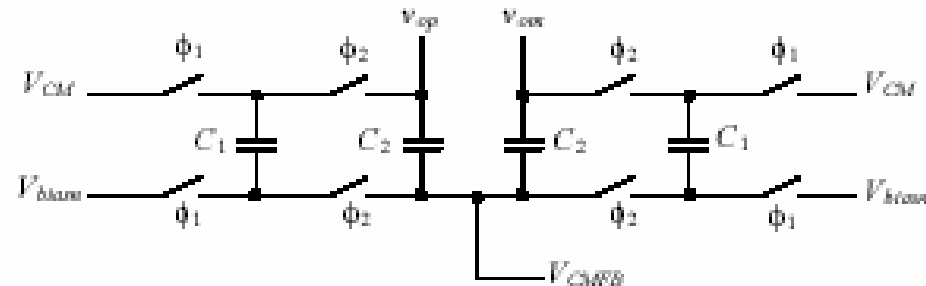NMOS are 10/1

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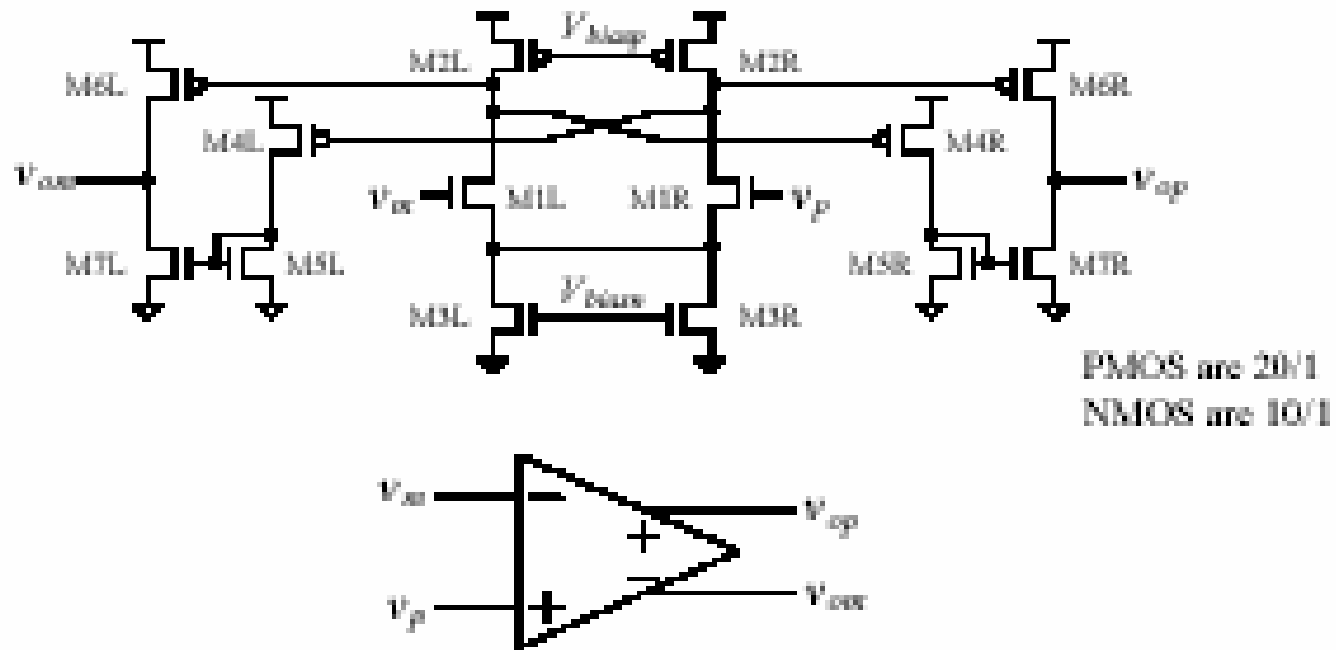
Need to set output common-mode level

(a)

(b)
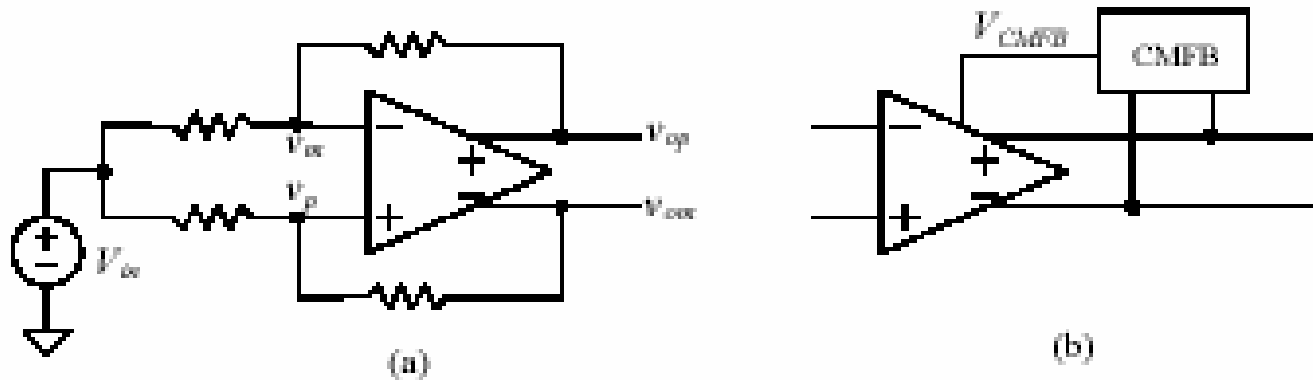
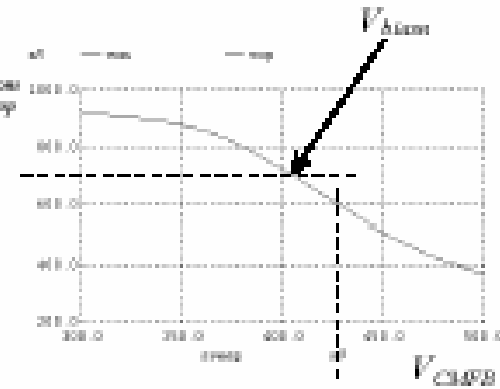# Switched-Capacitor CMFB

NMOS 10/1
PMOS 20/1
Bias circuit from Fig. 26.3

Value of CM feedback voltage
when the outputs are 600 mV.

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Use of SC-CMFB

- For the most robust design used SC-CMFB around each stage
  - The outputs of the diff-amp are set to bias the output buffer
  - The outputs of the buffer (the op-amp outputs) are balanced around the common-mode voltage, V_{CM}
- SC-CMFB provides wide operating range
  - Low power consumption
  - Small loading
  - Robust operation

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Example: a S/H amplifier

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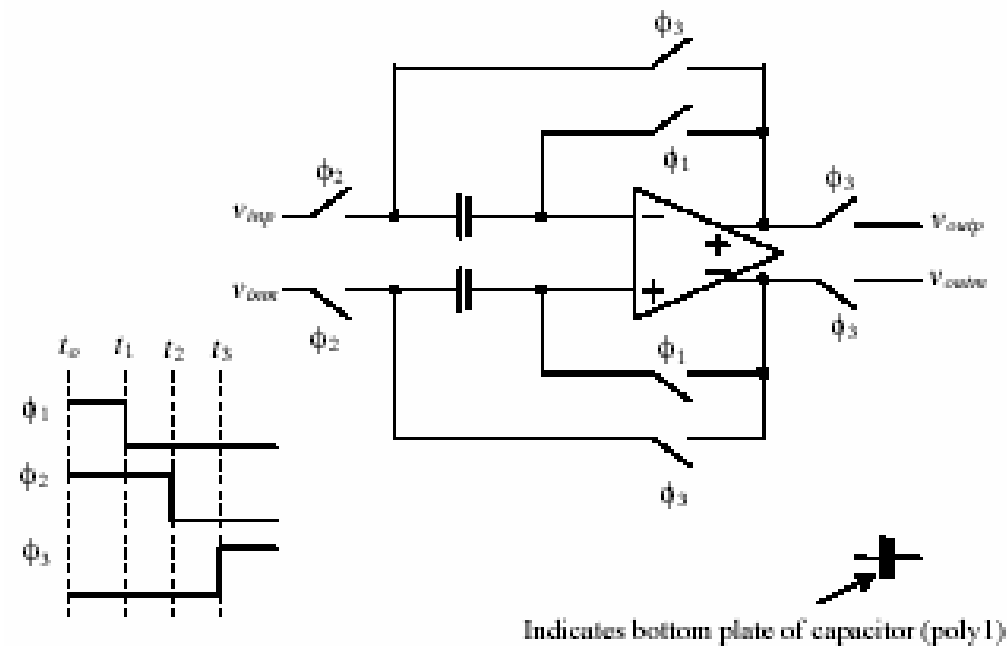
Input Diff-Amp
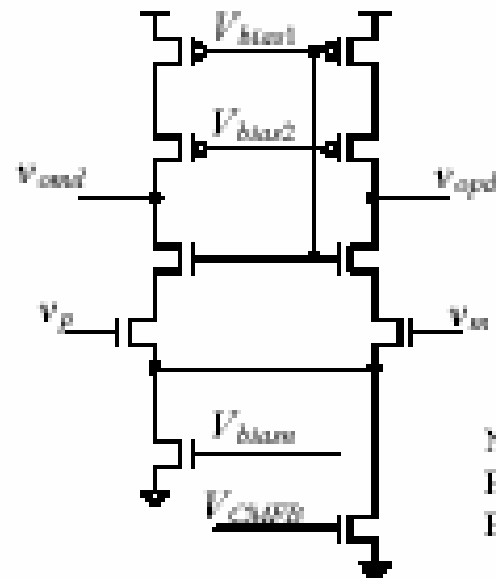
NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.52

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Setting the Output CM Level – method to get proper biasing with horrible offsets

NMOS are 10/1
PMOS are 20/1 (TGs use 10/1)
Bias circuit in Fig. 26.52

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Output Stage

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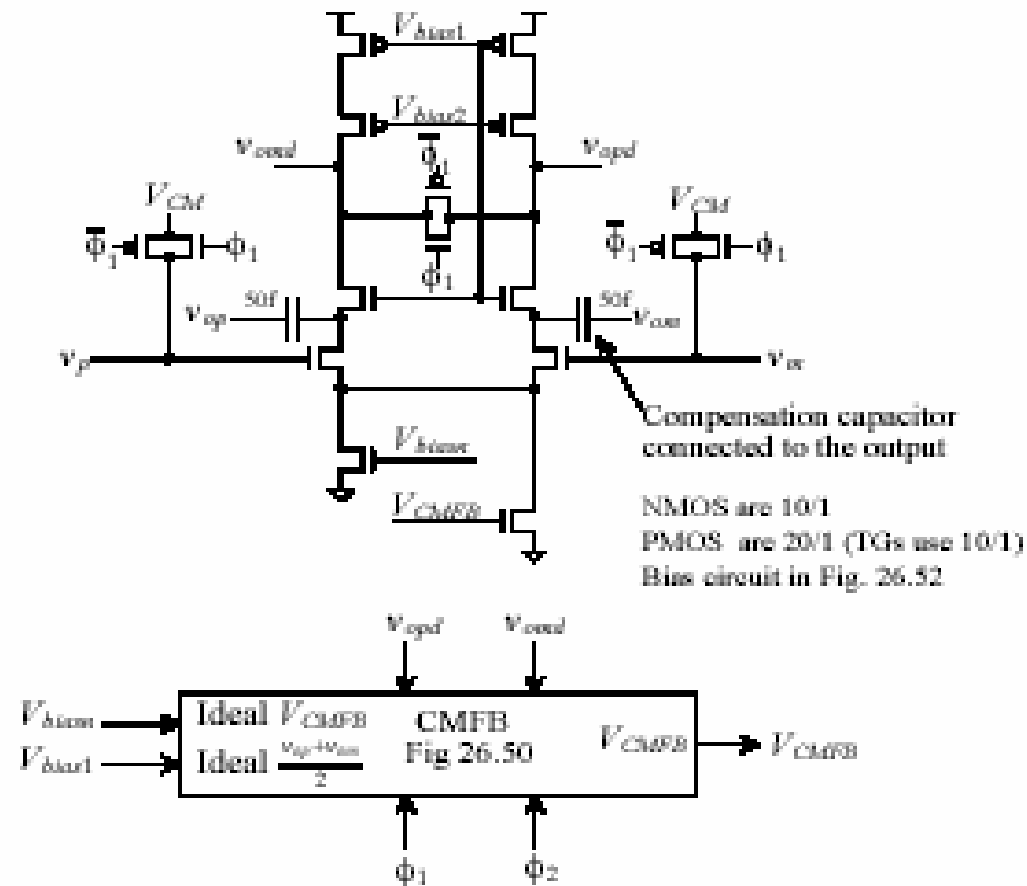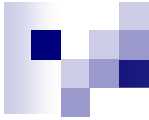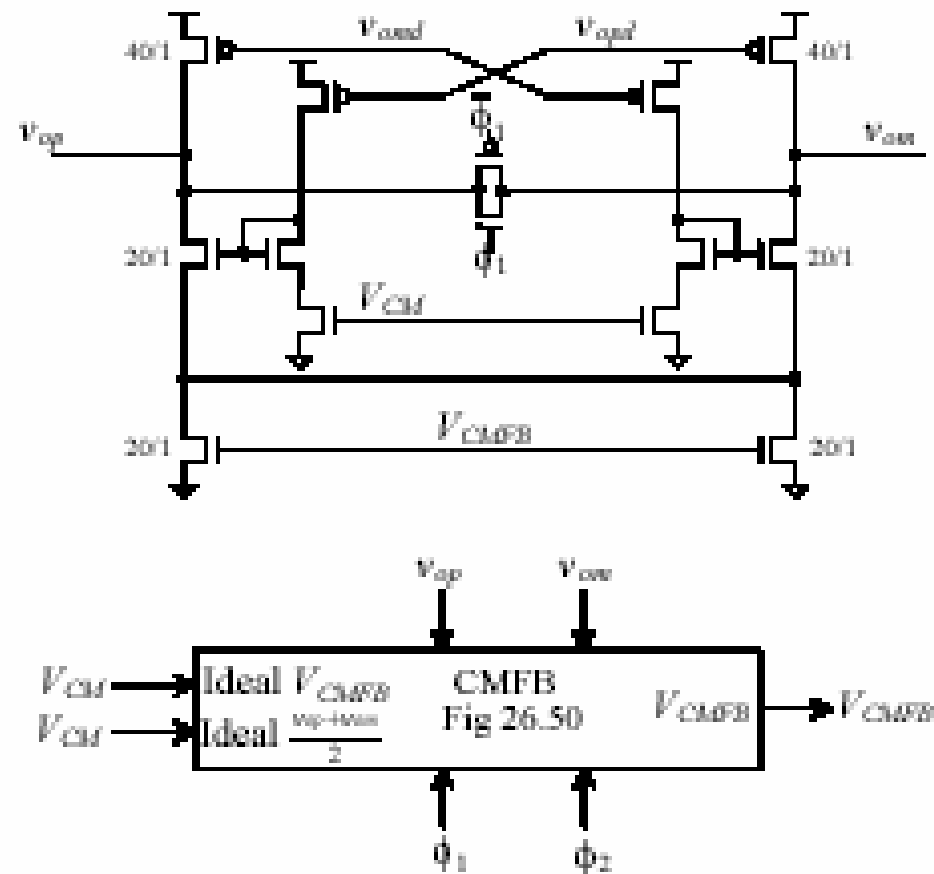
Simulating the Op-Amp's Operation

- No compensation capacitance (unstable in some cases), settling approx. 6 ns
  - Note that these simulation results are directly from Fig. 26.60 in my CMOS book, see http://cmosedu.com

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Increasing Compensation Cap to 50 fF

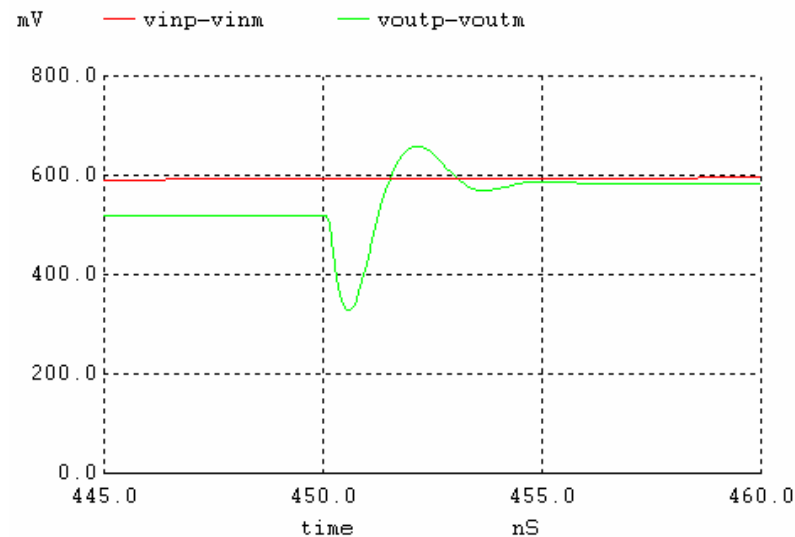- The settling time is approximately 5 ns. Note the stability is, of course, better.
  - Direct sim of Fig. 26.60 except the rise/fall times of the clock signals was reduced from 2 ns to 200 ps (this slows the simulation time)

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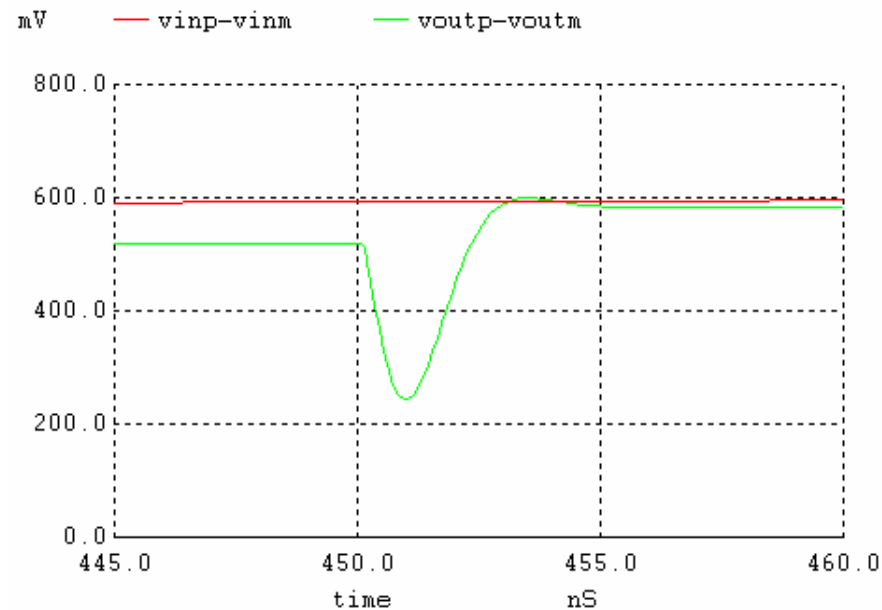
Increasing Compensation Cap to 150 fF

- Better stability but longer settling time. What do we do?

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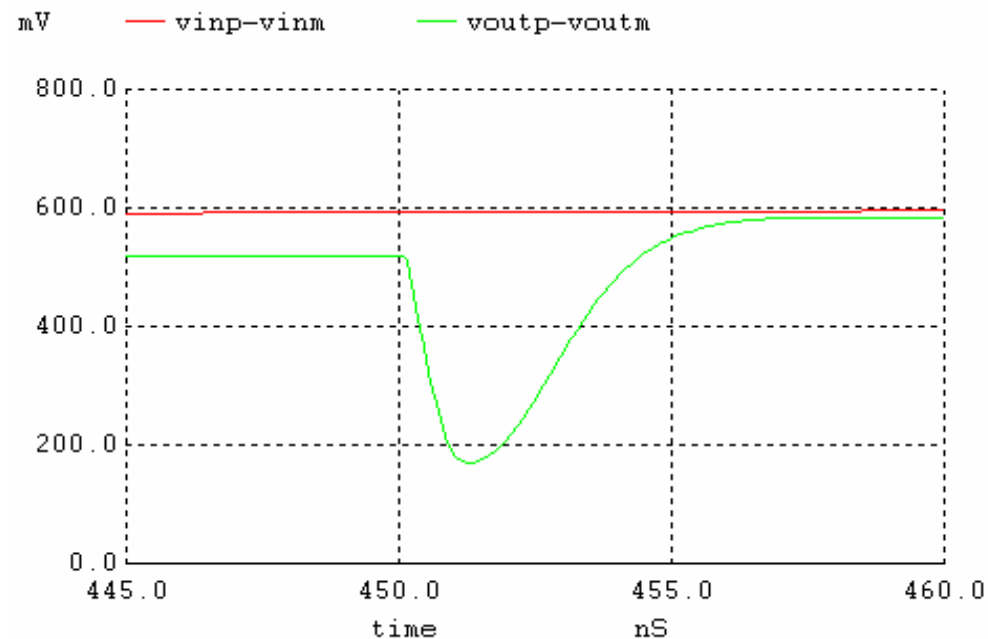# Increasing speed (decreasing settling time)

- **We need to increase the gain bandwidth product of the op-amp**
  - The only ways to do this are to decrease the compensation capacitor and/or increase the diff-amp's transconductance, $f_{un} = g_m/2\pi C_c$
  - The problem with this, as just shown, is stability (the pole, f_2 associated with the output of the op-amp is comparable to f_{un})
  - Need to push f_2 to a higher frequency by increasing the output buffers g_m
  - We do this by increasing the widths of the devices in the output buffer
    - Note this results in larger current flowing in the output buffers keeping overdrive voltages constant (important)
  - To increase the g_m of the diff-pair we increase their widths

Increasing Speed

- Use a 12.5 fF capacitor for C_c (1/4 of the 50 fF seen before)
  - □ Note that we are designing in a 50 nm process
- Increase g_{m2} by 4 by increasing the widths in the output buffer by 4
  - □ Cost is additional power dissipation in the output buffer
- Settling time drops to 2 ns (now we're cooking with gas!)
  - □ Op-amp power is 200 µW quiescent

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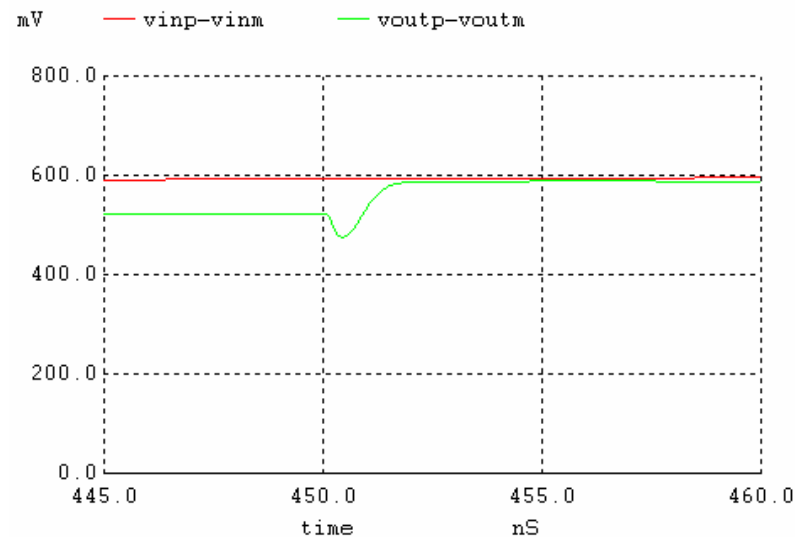
Conclusions: Further Increases in Speed (comments)

- Why didn't we try to increase speed by increasing the diff-pair's g_m (by increasing the pair's widths)?
    - This causes the overdrive voltages of the diff-pair to decrease unless we increase the diff-pair bias current (which would require increasing the widths of other devices in order to maintain the overdrive voltages). The drop in the widths of the diff-pair cause (low) parasitic poles in op-amp's frequency response.
    - Small increases in diff-pair width are okay. We used a factor of 3 in the sims here, that is, the diff-pair were 30/1 while other NMOS were 10/1.

- Note, again, that we attempt to design with fixed overdrive voltages to keep the design optimized for speed

Conclusions: Further Increases in Speed (comments continued)

- Looking at these results we might ask, "Why not multiple the sizes in the output buffer by 8 and divide the compensation capacitor by 8?"

- We run into a brick wall. The parasitic poles of the devices limit further increases in speed.

  □ To obviate this limitation we must increase the device's transition frequency (by increasing the overdrive voltages…change the bias circuit)

  □ Note we are assuming minimum L devices (absolutely necessary for high-speed design)

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