The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society

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Abstract – Memory technology development, in particular dynamic random access memory (DRAM), has been the greatest driving force in the advancement of solid-state technology for integrated circuit development over the last 40 years. The origin of DRAM circuits and technology can be traced to Dr. Dennard’s Patent (Number 3,387,286) granted on June 4, 1968. This truly visionary work, using a single transistor and capacitor (the 1T1C), is one of the most manufactured devices in the history of mankind. This talk will review the impact of his invention and discuss the brilliance of Dr. Dennard for conceiving the invention of the 1T1C cell prior to the maturity of metal oxide semiconductor (MOS) technology and in the face of critics that may have likely asked “why in the world would we want a memory, DRAM, that forgets its’ contents!”
Let’s Step Back in Time

What are the following (hint: they were found in your local supermarket in the 50s, 60s, and early 70s)

Photos taken from ebay.com
Semiconductor-based Electronics were still new during this period of time

Does anyone remember the birth of the transistor radio?

Below is seen the 2-transistor Furtura transistor radio (ca. 1955)

- Note the output is via an earphone
- Also note the schematic (not many, if any, consumer electronics products today come with a schematic)

Photos taken from ebay.com
These were a big deal both because they were portable (something not practically possible with vacuum tube radios) and because they used a new technology (solid-state devices that didn’t wear out)
Growing Complexity

- Note the use of bipolar junction technology to replace vacuum tubes
What was going on with memory storage during this time?

- Dominated by the magnetic core memory seen below
- During the 1960s solid-state memory was developed based on the BJT
  - Ultimately wasn’t successful (compared to MOS-based memory)
So why is Dr. Dennard’s invention such a big deal?

- During the excitement of bipolar technology replacing vacuum tubes in most electronic devices he filed an invention disclosure on July 14, 1967 that
  - Used metal-oxide-semiconductor (MOS) technology
  - Proposed a memory, the one-transistor, one-capacitor (1T1C cell), that forgets its contents!
- Why is using MOS technology such a big deal over bipolar?
  - MOS technology is scalable!
  - Another significant contribution from Dr. Dennard’s is scaling theory.
- Why is a memory that forgets its contents such a big deal?
  - It’s small!
  - It’s fast!
Dennard’s Scaling Theory*

- Predicted that MOS devices would continue to shrink in size (scale) over time
  - Higher density
  - Faster
  - Low power

- Also discussed how interconnect would scale
  - RC times of the lines don’t scale but as distances shrink delays drop

Scaling Theory

Scaling from Dennard’s paper

- Device and Circuit Scaling
- Interconnect Scaling
- Scale parameter is about 1.4 ($1/\kappa = 0.7$)

<table>
<thead>
<tr>
<th>Device or Circuit Parameter</th>
<th>Scaling Factor</th>
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<tbody>
<tr>
<td>Device dimension $t_{ox}, L, W$</td>
<td>$1/\kappa$</td>
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<td>Doping concentration $Na$</td>
<td>$\kappa$</td>
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<td>Voltage $V$</td>
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<td>Current $I$</td>
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<td>Capacitance $\varepsilon A/t$</td>
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<td>Delay time/circuit $VC/I$</td>
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<td>Power dissipation/circuit $VT$</td>
<td>$1/\kappa^2$</td>
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<td>Power density $VI/A$</td>
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<th>Parameter</th>
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<tr>
<td>Line resistance $R_L = \rho L/W t$</td>
<td>$\kappa$</td>
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<td>Normalized voltage drop $IR_L/V$</td>
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<td>Line response time $R_C C$</td>
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<td>Line current density $I/A$</td>
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The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM) cell

- The array is formed with word (row) and column (bit) lines.
The open array
Folded and Open Arrays

The folded array
The Folded Array
Further Reduction in Cell Size

- Sharing the bitline contact

![Diagram showing sharing of bitline contact](image)
Mbit Pair: Folded Array
Folded Array Cell Size

Bit line pitch: $2F$

Area: $8F^2$
Open Array: $6F^2$

$F$ is feature size, which is half the bit line pitch; that is, $F = \text{pitch}/2$. 

Bit line pitch
Array Block

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**RD** Row decoder and driver circuitry

**SA** Sense amplifier and column decoder circuitry.
The 1T1C DRAM Cell

1-transistor, 1-capacitor (1T1C) DRAM Cell
SEM Photo of a Modern DRAM Array
How is DRAM used today?

**Workstations**
- Units: 1.69M
- DRAM: 5,741MB/unit average
- DRAM Revenue: $1,164M
- Source: iSuppli

**Personal Digital Assistants**
- Units: 8.9M
- DRAM: 65MB average
- DRAM Revenue: $698M
- Source: iSuppli

**Notebook Computers**
- Units: 51M
- DRAM: 510MB
- DRAM Revenue: $3,105M
- Source: iSuppli

**PC Servers, Enterprise**
- Units: 0.91M
- DRAM: 24,581MB
- DRAM Revenue: $2,684M
- Source: iSuppli

**Desktop Computers**
- Units: 150M
- DRAM: 560MB
- DRAM Revenue: $10,048M
- Source: iSuppli

**Memory Upgrades**
- Units: 87M
- DRAM: 295MB
- DRAM Revenue: $3,060M
- Source: iSuppli

**Printers**
- Units: 112M
- DRAM: 35MB
- DRAM Revenue: $156M
- Source: iSuppli
Communications and Networking Market

**Cellular Phones**
- Units: 740M
- DRAM: 5MB
- Flash: 87MB

**Set-Top Boxes**
- Units: 62M
- DRAM: 56MB

**Cable Modems**
- Units: 15.7M
- DRAM: 8MB
- Flash: 2MB

**DSL Modems**
- Units: 55M
- DRAM: 8MB
- Flash: 2MB

**Cellular Base Stations**
- Units: 0.35M
- DRAM: 256MB
- Flash: 5112MB

**LAN Switches**
- Units: 113.5M
- DRAM: 15MB

**Low-End to Mid-Range Routers**
- Units: 1.5M
- DRAM: 406MB

Sources: iSuppli, Gartner, Portelligent, Instat
DRAM Demand by End-Use Application

*Other Data Processing includes mainframe servers, enterprise servers, workstations, handheld PCs, storage cards, printers, and internet appliances.
Worldwide DRAM Shipments by Type
DRAM Technology Trends
DRAM Density Trends

Source: IDC, Isuppli, Gartner, IC Insights Q106
Historical PC Market Growth

Units in Millions

Year over Year Growth

Grand Total

Grand Total

0
-10%
-15%
Historically Price per Bit has declined by an average of 9% every quarter (1974–2005)
Americas DRAM Unit Shipments by Density

- 1Mbit
- 4Mbit
- 16Mbit
- 64Mbit
- 128Mbit
- 256Mbit
- 512Mbit
- 1Gb
- 2Gb
- 4Gb
- 8Gb
256Mb Equivalent Unit DRAM Shipments

256Mb Equivalent Units Shipped
(K Units)

Total 256Mb EU

12/12 Growth
DRAM Applications with the Highest Unit Growth Rates

(CAGR 2004 – 2008)

- Entry-Level PC Servers
- Internet Appliances
- Mobile PCs
- Wireless LAN Client Access
- Wireless LAN Access Point/Bridge
- SAN Switches
- MP3 player
- Flash Storage Cards
- Digital TVs
- DVD Video Recorder

0% 10% 20% 30% 40% 50% 60%
Fastest Growing DRAM Consumption

(CAGR 2004 – 2009)

- Mobile Handsets: 90%
- Remote Access RAC & RAS: 70%
- Internet Appliances: 50%
- Workstations: 40%
- Entry-Level PC Servers: 40%
- Deskbound PCs: 40%
- Mobile PCs: 40%
- Handheld Computers: 40%
- Upgrade Module: 40%
- Enterprise Servers: 40%

Baker
DRAM chips are found in virtually every computer in use today. Looking at the simplicity of the 1T1C cell one might wonder about the significance of this invention by modern day standards. However, if it is remembered that this idea was conceived back in the 1960s before MOS technology had matured enough for production or the idea that circuits could be “dynamic” (only operating correctly for a short period of time) the significance of the invention becomes clear. What is usually not mentioned when talking about Dr. Dennard’s contributions to the 1T1C memory cell is his contributions of seeing this idea to product (the true test for any practical electrical engineer). The MOS process development (and the concerns for defects and reliability which have a drastic effect on the dynamic operation of MOS circuits) and supporting circuitry are also extremely important contributions that Dr. Dennard made while at IBM. In summary, Dr. Dennard cut the path for modern DRAM memory chip developments.