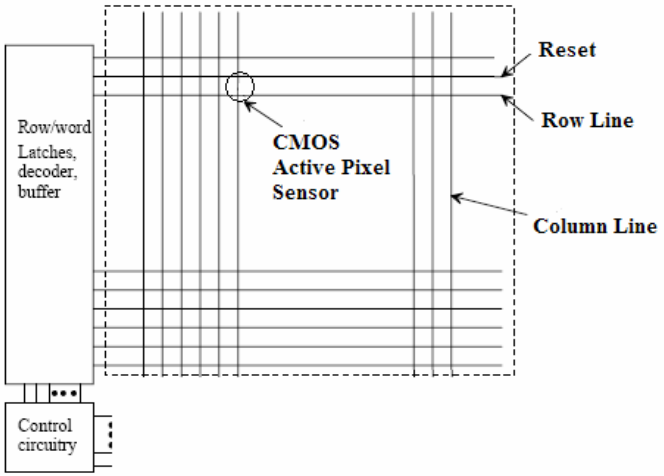
Sensing in CMOS Imagers using Delta-Sigma Modulation

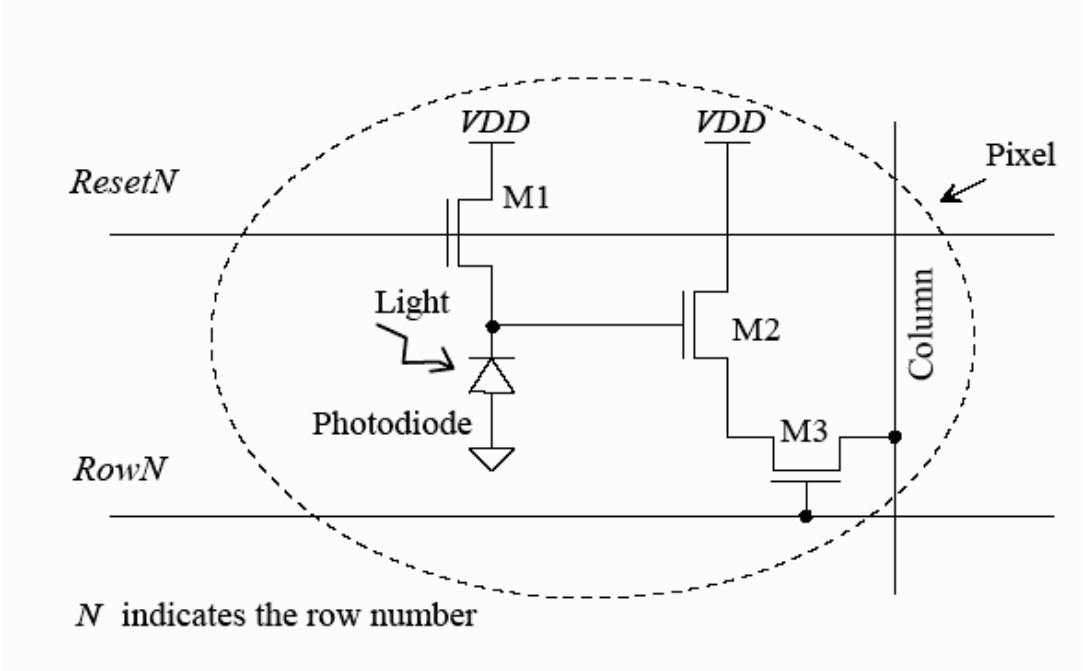
Mark Hadrick and R. Jacob Baker
Department of Electrical and Computer Engineering
Boise State University

Imager Pixel Array



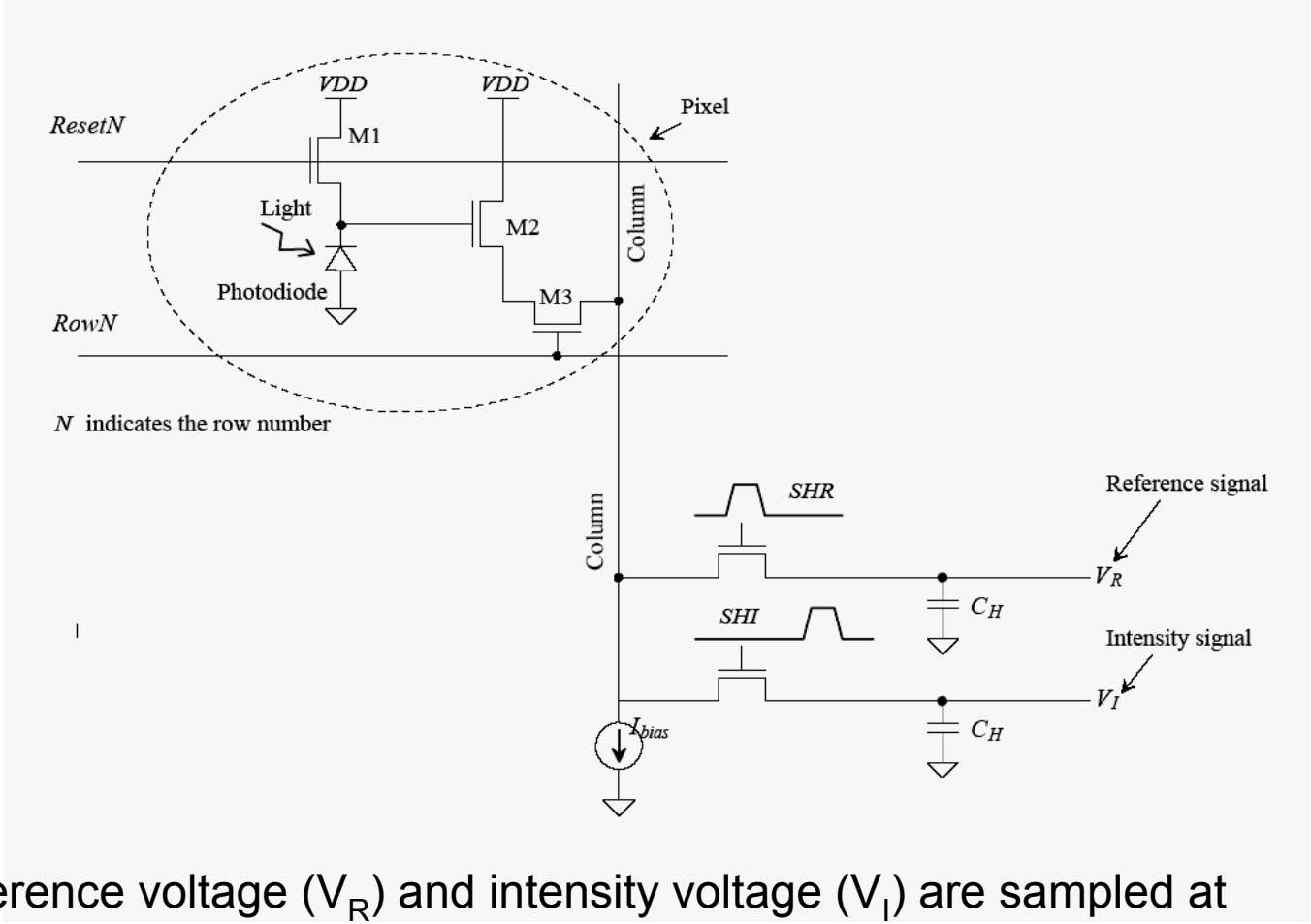
- An imager consists of an array of pixels, each with a row reset and select. When a row of pixels is active, their voltages are put on the corresponding column lines and sampled.
- By selecting all the rows in turn, the entire array of pixels can be sampled, their data concerning the intensity of light can be sensed, and the captured image can then be stored or recreated.

A Single CMOS Active Pixel Sensor



In order to acquire an image, each pixel is first reset to a reference voltage (i.e. the gate of M2 is set to VDD), and a voltage is developed on the column line. The photodiode is then exposed to light, conducting current to ground, lowering the voltage on M2's gate in proportion to the light's intensity. After the aperture time, this voltage is put on the column line.

Sampling the Reference and Signal Voltages

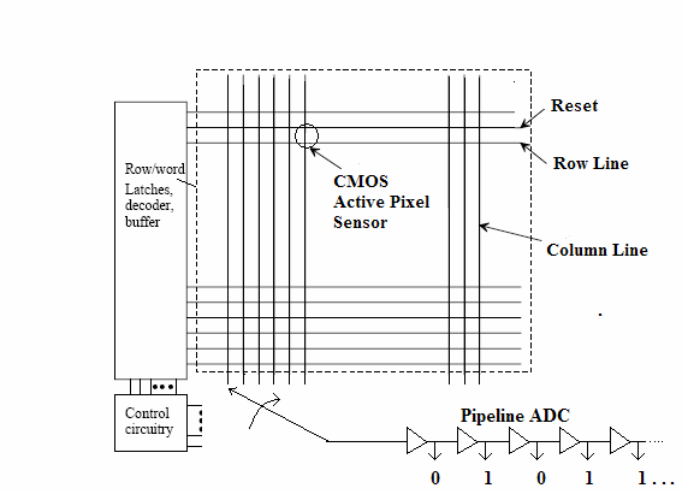


The reference voltage (V_R) and intensity voltage (V_I) are sampled at different times on the column line and then stored on hold capacitors. The sensing circuit must determine the difference between these two voltages.

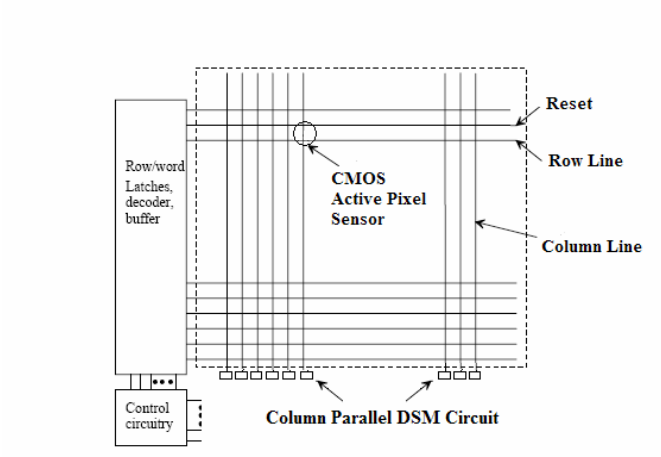
$(V_R - V_I)$

- Using the reference voltage (V_R) allows "standardization" between the different individual pixels in the imager array.
- The difference between ($V_R - V_I$) is proportional to the intensity of the light hitting the diode.
- The sensing circuit must determine this difference and convert it into a digital signal

Pipeline vs Parallel Sensing Circuits



Pipeline ADC Sensing Circuit



Column Parallel DSM Sensing Circuits

- Pipeline ADC – all columns share a single sensing circuit that reads each column sequentially
- Column Parallel DSM – each column has its own sensing circuit, all sensing circuits reading their column simultaneously

Benefit of Pipeline ADC

- Single sensing circuit common to all data so offsets and nonlinearities are consistent

Problems with Pipeline ADC

- Must sense each column line in the array sequentially. Larger arrays introduce limitations (time, charge sharing, etc.)
- High power circuit
- Precision circuit – long design time and designs are not transferable (or scalable) between semiconductor processes
- Noise issues

  1) Noise set by kT/C, so each stage of ADC must use large capacitors (thus the ADC has a large layout size)

  2) Large capacitors result in charge sharing error between sample and hold capacitors and ADC.

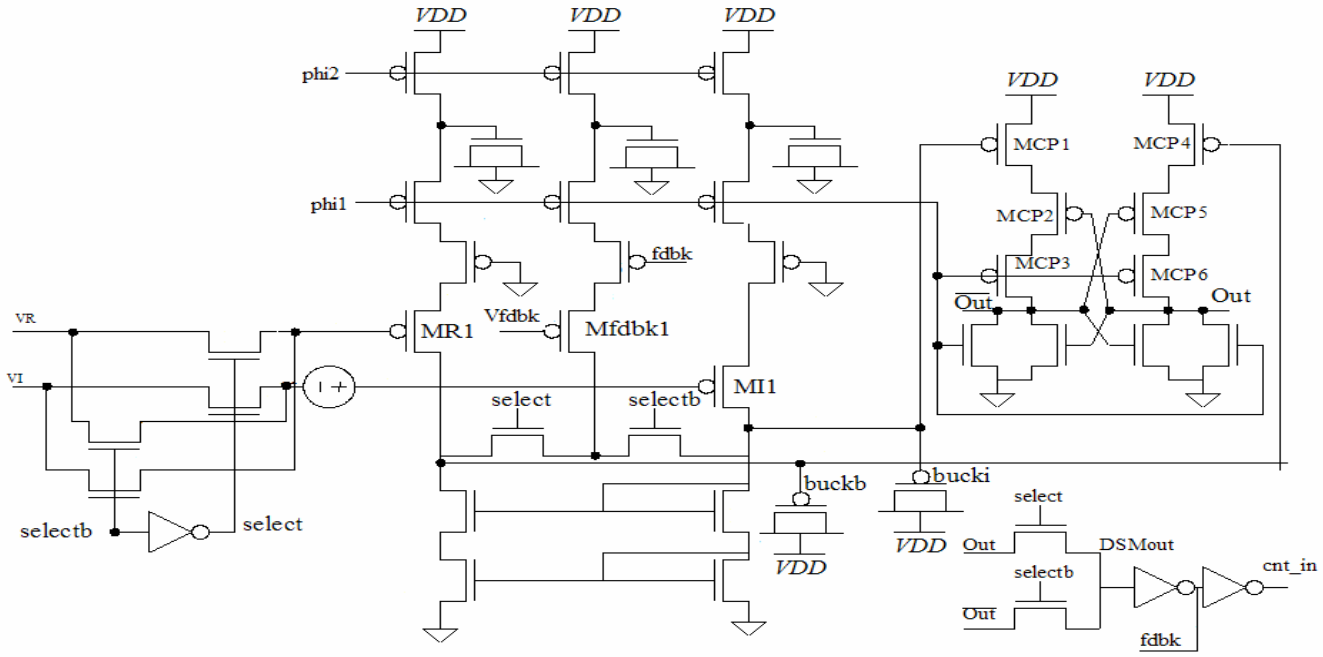
Benefits of Column Parallel DSM

- All columns sensed simultaneously by dedicated sensing circuit, so larger image arrays are possible
- Low power
- Design easily transferable (scalable) between semiconductor processes
- DSM noise set by kT/NC, where N is the number of clock pulses during the sense – the longer the sense, the smaller the required capacitors

Problems with Column Parallel DSM

- Since each column has a separate circuit doing its sense, variations between individual DSM circuits are a big concern.
- Column offsets and offsets within the DSM circuits must not interfere with the value sensed at each column

DSM Circuit



- The DSM sensing circuit presented here will accurately sense the pixel's light intensity despite variations in column offset
- It also corrects for any offsets within the DSM circuit itself.

DSM Circuit

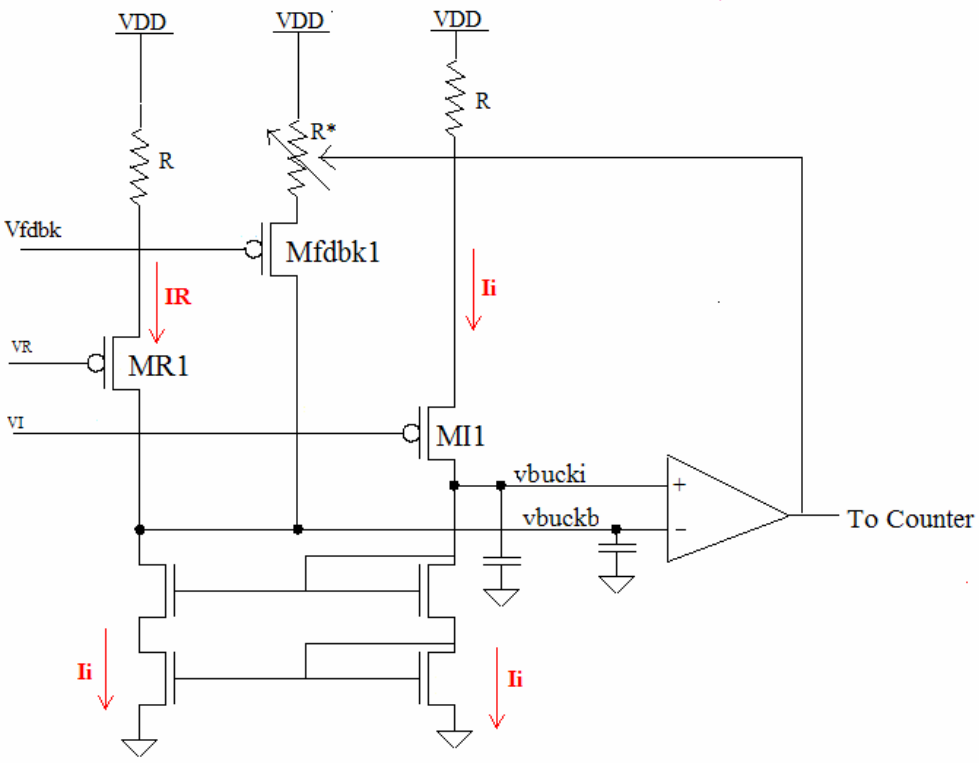
The difference between the currents I_R and I_i is proportional to (V_R-V_I).

These currents are summed by the voltage on the capacitor (Vbuckb).

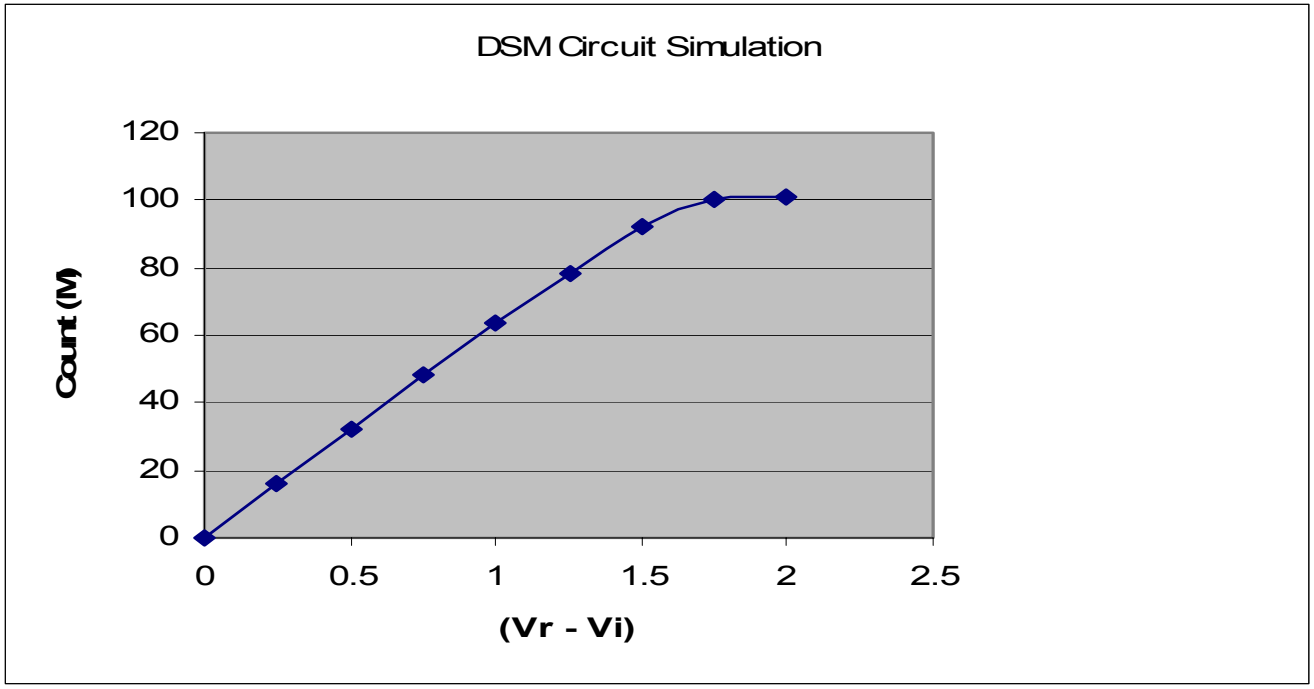
The comparator acts to keep the currents feeding both capacitors the same by enabling the feedback path.

A counter keeps track of the number of times the comparator fires.

The DSM's output is the count, which is proportional to (V_R-V_I).



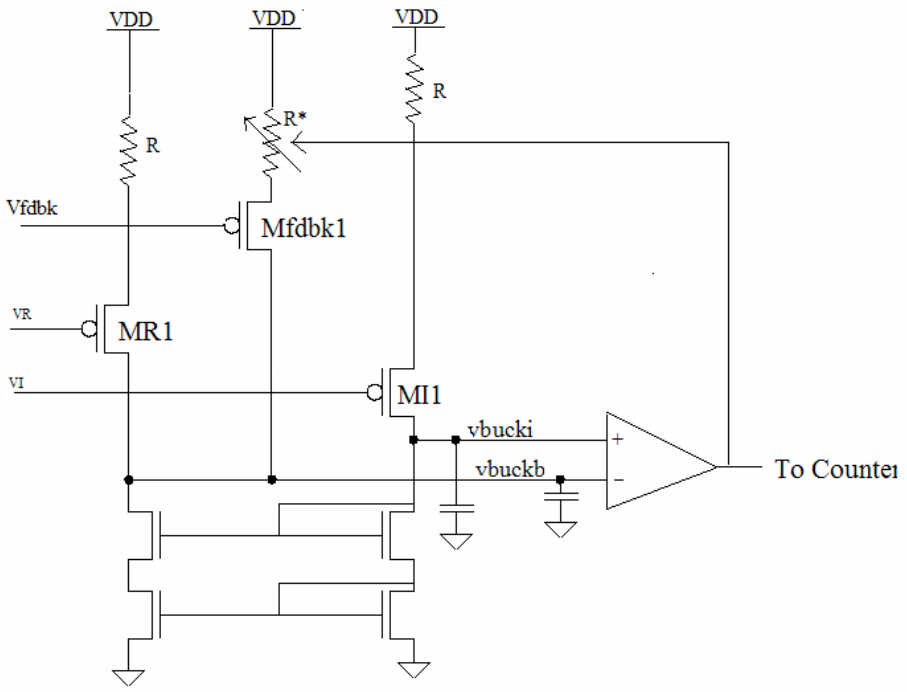
DSM Circuit Simulation Results



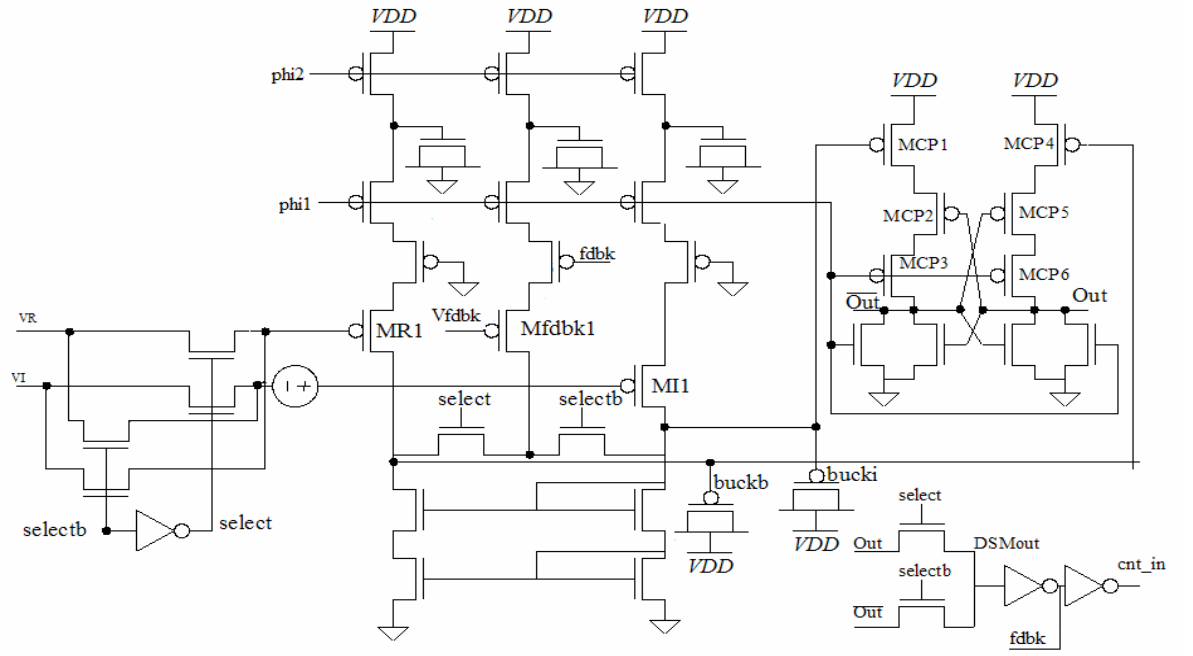
- The graph shows the DSM circuits output for (V_R – V_I) ranging from 0 to 2V.
- The circuit's output is linear over the range of 0-1.5V

Path Offset

- Because there are separate paths within the DSM sensing circuit for V_R and V_I, there is the potential for mismatch within the circuit.
- Examples of potential mismatch include:
  - Slightly different threshold voltages for MR1 and MI1.
  - Small differences in the capacitance values at Vbucki and Vbuckb
  - Differences in the two current mirror paths or the switched capacitor resistor paths

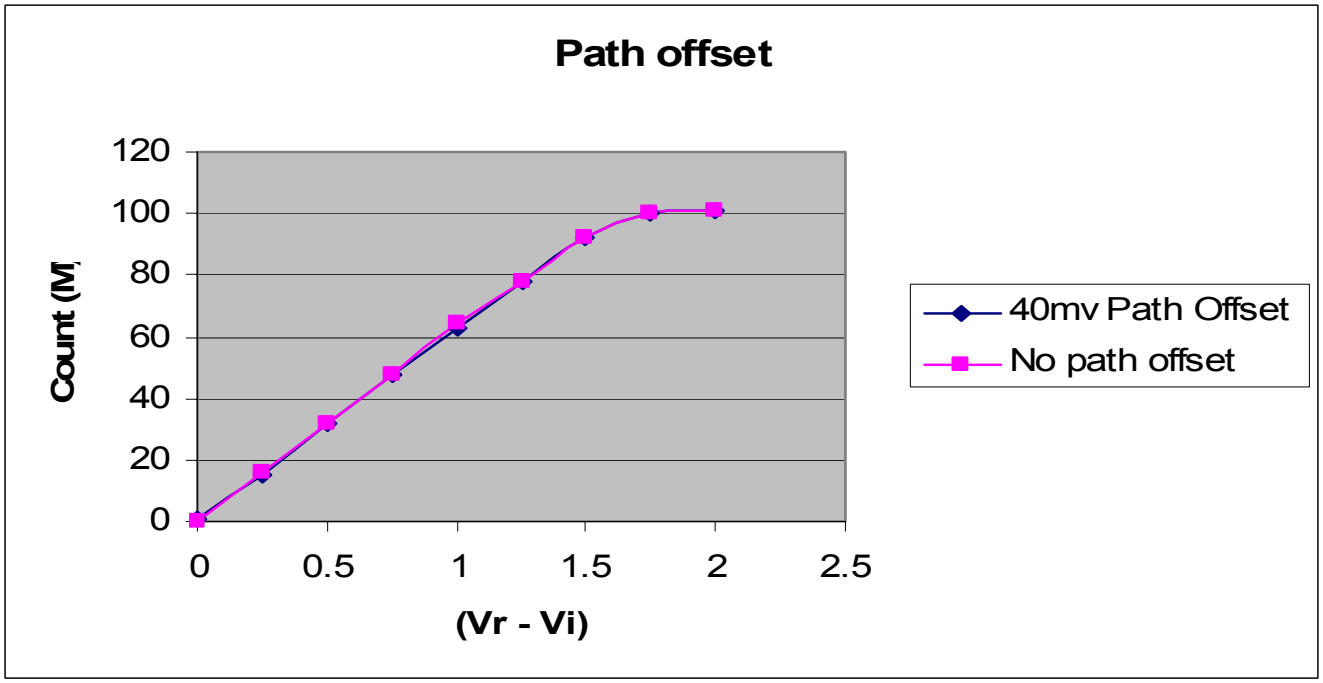


Path Offset



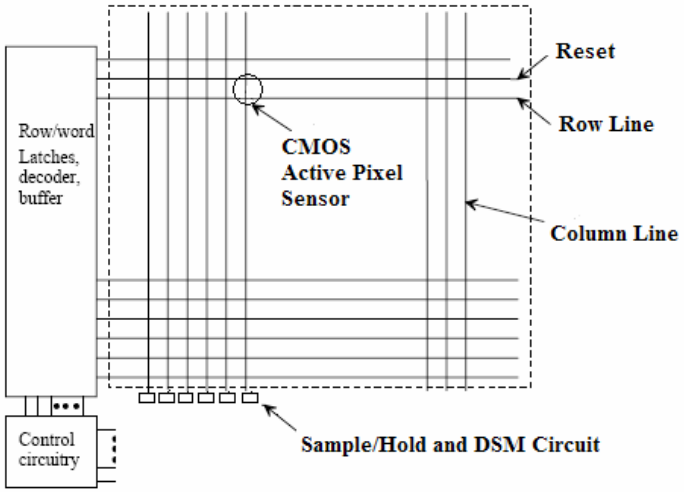
- To reduce the effects of mismatch on the sense, the circuit switches the paths of the two inputs (V_R and V_I) midway through the sense.
- Switching the paths averages the effects of any path mismatch between VR and VI.

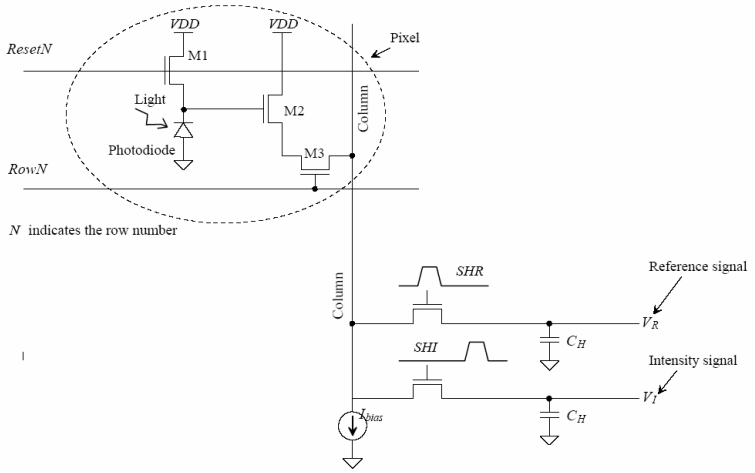
Path Offset



- The graph shows simulation results for the circuit with and without a path offset of 40mV
- The path offset does not affect the output of the circuit.

Column Offset

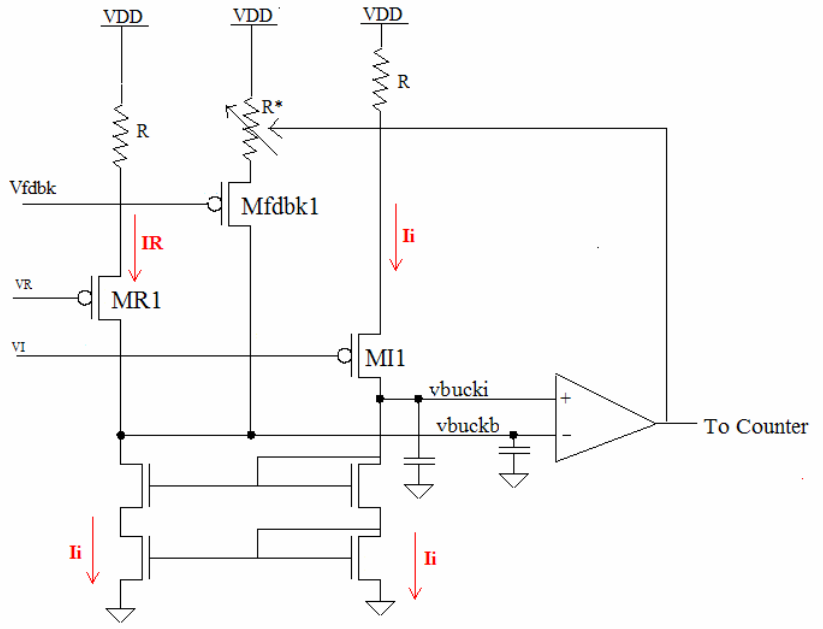




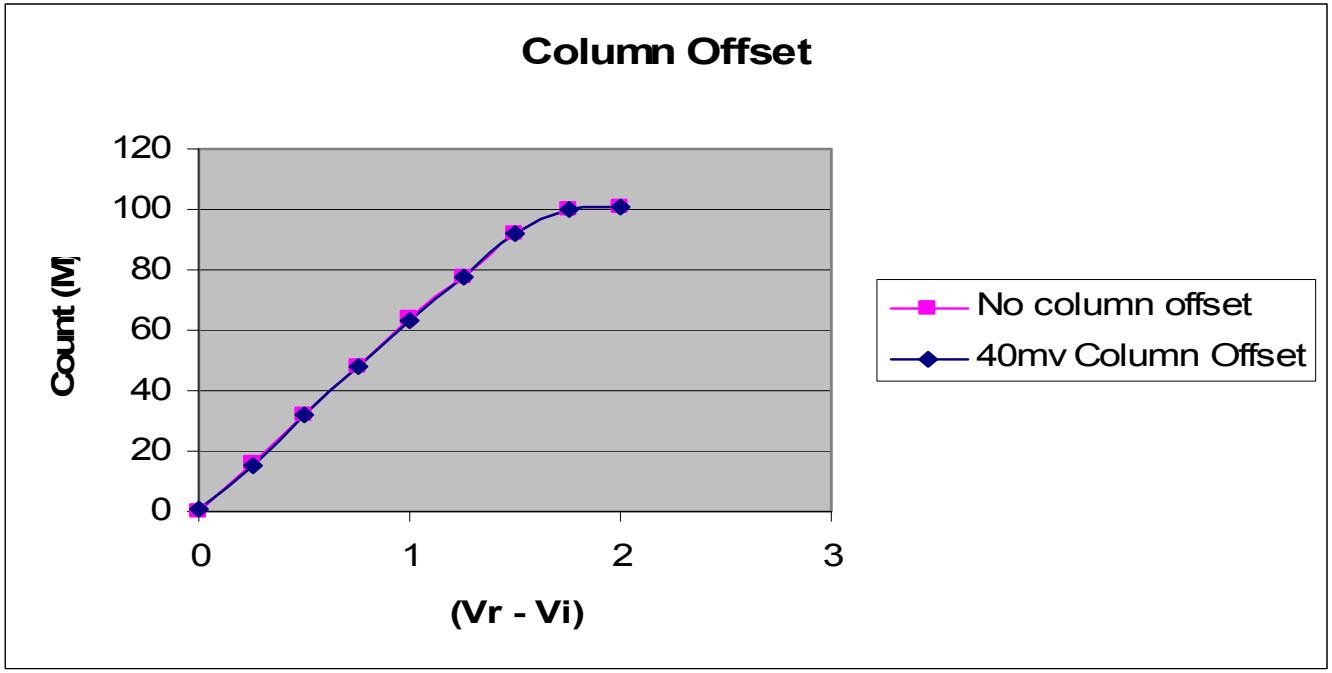
- Since the imager has many columns, there is the potential for mismatch between the columns. Mismatch between columns results in the values for both V_R and V_I for one column being shifted relative to another column's. This mismatch, if not corrected for, will result in vertical streaks in the resultant image.
- A potential source of mismatch between columns includes variations in the average of the threshold voltages of, for example, M2, between columns

Column Offset

- To reduce the effects of column mismatch on the sense, all the DSM sensing circuits use a common independent **reference voltage** (Vfdbk) in their feedback path.
- Since Vfdbk is unaffected by the column variations, the current in the feedback path will accurately reflect the difference between V_R and V_I, regardless of whether both values are shifted by the column offset



Column Offset



- The above graph shows the circuit's simulation results both with and without a column offset of 40mV
- The column offset does not affect the output of the circuit.

Summary

Compared to traditional pipeline ADC sensing circuits, the DSM Sensing Circuit presented here will:

- Reduce layout size
- Allow for larger array size
- Require less power
- Allow for faster design turn-time
- Lower noise (increased SNR) sense

Summary, cont'd

In addition, this circuit corrects for the two problems inherent in column parallel processing of data:

- It accurately senses pixel inputs despite variations in the column characteristics across the image array
- It self-corrects for variations within the DSM circuits themselves

The circuits presented in this document have been fabricated; however, we will not present the experimental results at this time because of commercialization concerns.