

University of Nevada

Reno

Applying Power MOSFETs to the Design of Electronic and Electro-optic
Instrumentation

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by

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Abstract

The Power MOSFET is used in the design of electronic and electro-optic instruments requiring signals with amplitudes from several hundred to several thousand volts varying in the nanosecond time regime. The traditional use of the power MOSFET is in power electronics where the load driven is mainly inductive. The loads driven in electronic and electro-optic instruments are capacitive, resistive or a combination of the two. The average power considered is low while the peak power is high. The limitations on switching times and circuit configurations in driving power MOSFETs are discussed. The main emphasis is on circuit design with amplitudes greater than 1000 V and transition times less than 5 ns.

The experimental applications consist of a variable width square wave generator, a 1.4 kV pulse generator, a Marx bank of power MOSFETs, a streak camera ramp generation circuit, a 1.5 kV, 500 ps risetime pulse generator and a 2.4 kV, <150 ps pulse generator. The variable width pulse generator is controlled with a TTL pulse and generates a 500 V waveform into 50 ohms with a rise time of 2 ns and a fall time of 8 ns. The 1.4 kV pulse generator uses power MOSFETs in series with a resulting risetime of 2 ns. The Marx bank generates a 1.8 kV pulse with a risetime of 3 ns from a 400 V supply. The streak camera ramp circuit is used for generating sweeps from less than 5 ns to greater than 300 ns controllable with a DC voltage. The amplitudes of the ramps are ± 2 kV into a 10 pF load. A nonlinear transmission line is used to generate a 1.5 kV pulse with a 500 ps risetime. The last example uses power MOSFETs with an avalanche diode to generate kV level pulses with risetimes under 150 ps.

All of the applications presented represent significant improvements in the state-of-the-art for high voltage fast risetime pulse and ramp generation. Series operation of power MOSFETs without degradation in switching time compared to a single device is one of the significant contributions of this work. Finally, other applications in pulsed power, radar and instrumentation are discussed.

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Chapter 1 - Introduction

1.1 The Power MOSFET

This dissertation is concerned with applying power MOSFETs to the design of electronic and electro-optic instrumentation. Applications requiring pulses, ramps and amplifiers with amplitudes greater than 500 volts and switching times, in general, less than 5 ns are considered. This departs from the traditional use of power MOSFETs in power electronics. The concern in this dissertation is with speed and maximum voltage or current swing. The average power dissipated in most of these applications is low while the peak power is high.

Another difference between the normal use of power MOSFETs in power electronics and their use in the instrumentation in this work is the type of load driven. In power electronic applications the load is almost exclusively inductive, e.g., a transformer or inductor. The load driven in the instrumentation applications presented here is either resistive, capacitive or a combination of the two. Most electro-optic loads are capacitive in nature, e.g. a Pockel's cell, streak tube etc. Other types of capacitive loads found in electronics are vacuum tubes such as the planar triode, thyratron etc. Because an inductor impedes a changing current, any inductance in these high speed circuits must be minimized. This means keeping the lead lengths of the power MOSFETs as short as possible. The MOSFETs used here are packaged in an industry standard package such as a TO-220. The hope is that the results can be reproduced with relative ease by others needing to generate these types of waveforms.

The history of the development of the power MOSFETs is covered in references [1,2]. A brief discussion of the current structure of the power MOSFET with an emphasis on the aspects that will affect circuit design seems appropriate in this introduction.

The majority of power MOSFETs used currently are the n-channel enhancement type. The power MOSFET is actually made up of hundreds of smaller MOSFETs in parallel. The effective channel width of a power MOSFET can be greater than one

meter. The current density is low because of this wide channel width and results in the high power handling capability of the device.

The speed of the device comes from the channel length of typically $1\text{ }\mu\text{m}$. The intrinsic speed of the device is thus limited by the transit time of the carriers across the channel. If the electrons are traveling at their saturation limited velocity of 10^7 cm/s ($10\text{ ps}/\mu\text{m}$) the maximum frequency of operation is greater than 10 GHz . The channel length does not limit the speed of the device, but rather the contact resistance in combination with parasitic capacitance are the limiting factors.

The structure of the power MOSFET is the Vertical Double-Diffused MOSFET (VDMOS) [1-4]. This structure is shown in figure 1. The drain and source contacts are aluminum while the gate contact is polysilicon. Also notice that the source and channel are shorted together providing a parasitic diode between the drain and source.

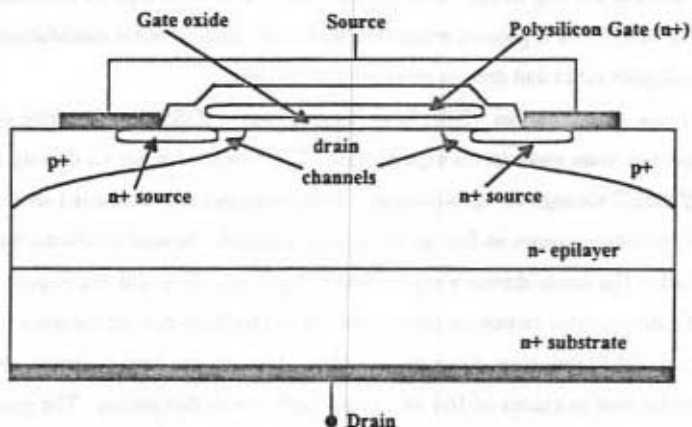


Figure 1 - Outline of a single cell in the VDMOS power MOSFET. The gate metalization is polysilicon. The source and channel are shorted together to form a diode between the drain and source.

The resistivity of the heavily doped polysilicon is ten to thirty times higher than aluminum. The contact resistance is typically several ohms and is the main factor in limiting the speed of the device. If the gate-source capacitance is 2000 pF and the gate contact resistance, R_g , is $2\text{ }\Omega$ then the resulting time constant is 4 ns . If the Miller effect

is added together with the finite source driving impedance it is easy to see that attaining switching times less than 5 ns will be difficult.

The gate oxide shown in figure 1 is where the majority of failures occur in instrumentation uses. Although the oxide is thicker than used in a typical integrated circuit, a maximum voltage of $\pm 20V$ is recommended by most manufacturers. The large junction capacitance combined with the large voltage changes over the nanosecond time intervals and the lead inductance can induce voltages in excess of 20V between the gate and source terminals. One simple but effective method of protection is the use of a zener diode between the gate and source.

1.2 Literature Search

A literature search on the applications and uses of power MOSFETs shows that power electronics is the main area where they are used. However, lately their use in instrumentation is starting to appear in the literature. The main type of instrumentation using power MOSFETs is physics research instruments, such as beam modulation, gating of photomultiplier tubes and driving electro-optic crystals.

Bernius and Chutjian [5,6] have used power MOSFETs for time-of-flight, coincidence and beam modulation experiments. Their method relies on driving the gate of each MOSFET through an opto-isolator. Both p-channel and n-channel devices were employed. Switching times as fast as 50 ns were realized. Several problems exist with their method. The loads driven were relatively light, i.e., they did not require a large amount of current. Also switching times were limited by their driving circuitry. Driving a heavy load will further slow down the rise time. If a 50 ohm load is driven, switching times could be well in excess of 100 ns causing high power dissipation. The gate circuit was their limiting factor. Since each gate of every MOSFET used is driven, circuit complexity is high, reliability is low and switching times are long.

One solution to the problem of driving a power MOSFET was discussed by Baker and Pocha [7]. They used an avalanche transistor to overdrive the gate. Since the output impedance of the avalanche transistor is negative, the switching time is limited by the output circuit, i.e., the type of load driven. The main disadvantage of this technique is repetition rate. The maximum repetition rate is limited to under 1 MHz. This is not a

problem in most uses because the average application does not require repetition rates above one kilohertz. Also if care is not taken, the polysilicon gate can be overdriven to the point of destruction. With proper design this is not a concern.

An 8 kV stack of power MOSFETs [8] was used in a beam modulation experiment. This stack of power MOSFETs was used to switch 8 kV to ground in 230 ns. Again each MOSFET gate was driven, in this case through a transformer with its secondary connected between the gate and source of each MOSFET and its primary connected to a driving circuit. With proper design techniques a simpler more reliable and faster circuit can be developed.

A product line of pulse generators using power MOSFETs is available from a company called Directed Energy Inc., (DEI) [9]. DEI repackages power MOSFETs to lower the lead inductance and improve switching times. Much of the development of this technology was performed at the Lawrence Livermore and Los Alamos National Laboratories by J.A. Oicles and G.J. Krausse [10]. Currently DEI sells pulse generators with risetimes under 10 ns and amplitudes to greater than 6,000 V. The fast switching speed is the result of carefully designed and laid out drivers and the lower packaging inductance.

1.3 Organization of this Dissertation

Chapter 2 of this dissertation discusses power MOSFET operation. Focus is placed on operation of the device germane to circuit design. First, since the threshold voltage of a power MOSFET is determined by the polysilicon gate oxide interface this will be discussed. During switching the device is mainly in the saturation region so frequency characteristics of the transconductance of the device will be presented. This is followed by a detailed analysis of the switching behavior, a discussion of maximum current and voltage ratings and temperature effects. The chapter concludes with a short discussion of SPICE modeling. SPICE modeling is important, because of the difficulty in measuring voltages at various points in the circuit. The high radiated power coupled with the large voltages applied to the probe make measurements with any accuracy almost impossible.

Chapter 3 discusses driving power MOSFETs. This is probably the most difficult aspect of designing instrumentation with power MOSFETs. For example, if the speed of the power MOSFET is limited by the junction capacitance and the contact resistance, the speed can be effectively increased by applying a higher level drive signal. If the device turns on in 10 ns when a 20 V signal is applied between the gate and source applying a 40 V signal will cause the device to turn on in less than 10 ns. Attaining fast turn on is the result of knowing how to design the gate driving circuit. Standard IC drivers are discussed together with discrete and avalanche drivers. The chapter ends with a discussion of the input and output impedance of the power MOSFET. These are important in understanding ringing and oscillations.

Chapter 4 presents basic circuit design techniques. The basic MOSFET switch and high repetition rate pulse generators are discussed. Series operation to increase the breakdown voltage and driving capacitive and resistive loads are addressed. The variation of the transconductance with frequency is used to describe oscillations. Practical aspects of circuit design are emphasized. Resistive and capacitive loads and their affect on circuit design are discussed. The chapter ends with applications and a discussion of the circuit designs investigated.

Chapter 5 presents the experimental results. The circuits presented in this chapter were built and tested. An electronically variable width 500 V square wave generator is presented. Applications of this type of pulse generator are discussed. This is followed by series operation of MOSFETs to attain higher output voltages. The series operation presented is in the form of stacking power MOSFETs to achieve a 1.4 kV pulse generator and a Marx bank configuration for a 1.8 kV pulse generator. These examples are followed with a streak camera ramp design example. The streak camera ramps are ± 2 kV into 10 pF. The ramps are adjustable from less than 5 ns to greater than 300 ns. Using the ramps generated with the power MOSFETs, signals are measured in the 10 ps regime using the streak camera. Because pulses are needed with risetimes less than 1 ns the final two sets of results presented in chapter 5 are subnanosecond pulse generators. The first pulse generator uses a nonlinear transmission line to generate a 1.5 kV pulse with a risetime of 500 ps. This section concludes with a discussion of generating pulses

with amplitudes greater than 3.5 kV and risetimes less than 200 ps. The last example uses power MOSFETs driving an avalanche diode to generate a 2.4 kV pulse with a risetime of 129 ps.

Chapter 6 discusses future work and other applications of power MOSFETs. In particular, power MOSFETs should find uses in radar, pulsed power and other areas of electro-optics.

Chapter 2 - Power MOSFET Operation

2.1 Introduction

This chapter is concerned with the operation of power MOSFETs and in particular the limiting factors influencing their operation. Emphasis is placed on power MOSFET operation from a circuit design point of view, i.e., operation important to attaining high speed rather than operation from a semiconductor physics point of view which is well covered in the literature[1].

2.2 The Threshold Voltage

The threshold voltage is the voltage required between the gate and source which will form a channel between the drain and source causing drain current to start flowing. Figure 1 shows this relationship. There are two major concerns when considering the threshold voltage. The first is that there will be a delay between applying a gate drive signal and the beginning of the drain current flowing. This will be addressed when determining the switching behavior later in the chapter. Second, as the device heats up the threshold voltage will shift to the left as shown in the figure. This becomes important when using low level drive signals especially in linear applications.

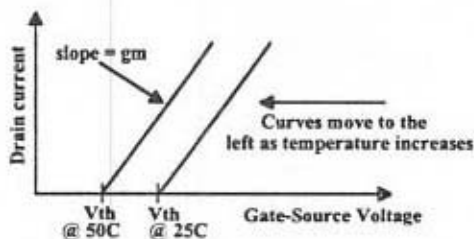


Figure 1 - Gate-source voltage versus drain current. The slope of this curve is the transconductance. The MOSFET is in the saturation region when the gate-source voltage is greater than the threshold voltage and $V_{ds} - V_{th} < V_{ds}$. Notice how the slope of the line is essentially constant, i.e., the transconductance is constant.

As an example, suppose the threshold voltage of a particular MOSFET is 4 V. Now if a 5 V signal is applied between the gate and source, and the drain current is sufficiently

large to cause heating in the device, the MOSFET could actually turn itself off. If the application is to design a linear ramp, this effect alone can cause severe nonlinearities.

2.3 The Power MOSFET in the Saturation Region

During switching the MOSFET must traverse through the saturation region. In linear applications such as amplifiers and ramp generators the operation is mainly in this region. Figure 1 shows how the drain current varies with applied gate-source potential. The power MOSFET is said to be in the saturation region when the gate source voltage is above the threshold voltage and $V_{gs} - V_{th} < V_{ds}$.

2.3.1 Transconductance

The power MOSFET's transconductance is important in circuit design. How the transconductance changes with temperature, frequency and operating conditions is of importance. The transconductance of a MOSFET is given by

$$g_m = \frac{dI_{ds}}{dV_{gs}} = 2K(V_{gs} - V_{th}) \quad (1)$$

where

$$K = \frac{1}{2} \mu \left(\frac{\epsilon_{ox}}{t_{ox}} \right) \left(\frac{W}{L} \right) \quad (2).$$

The ratio of the channel width, W , to the channel length, L , is on the order of 10^6 so the transconductance is very large, often larger than one Siemen. Equations 1 and 2 show that to a first order the transconductance does not depend on temperature unlike the threshold voltage. The variation of the transconductance with temperature will be neglected.

2.3.2 Variation of the Transconductance with Frequency

The variation of the transconductance with frequency is important because it is a major contributor to the change in input and output impedance. This is important when trying to understand ringing and oscillations. Consider the MOSFET circuit shown in figure 2. It is assumed that the MOSFET is operating in the saturation region and all signals in the following analysis are small compared to the operating point. Although most applications of power MOSFETs are in switching, the device still passes through the saturation region.

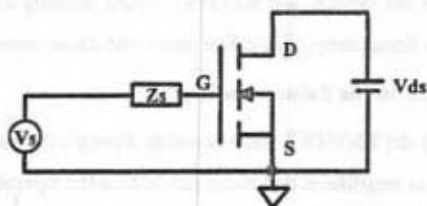


Figure 2 - Circuit used to determine the variation of transconductance with frequency. This method is similar to that used to determine the variation in current gain in bipolar transistors. The source here is a voltage source while that for the BJT is a current source.

The impedance Z_s includes the gate contact resistance, the lead inductance and the equivalent driving source impedance. Under normal operation a load is driven in the drain part of the circuit. This leads to the Miller effect which is an additional capacitance appearing between the gate and source of the device. The impedance Z_s can be modified to include this Miller capacitance. The equivalent circuit diagram for no load is shown in figure 3.

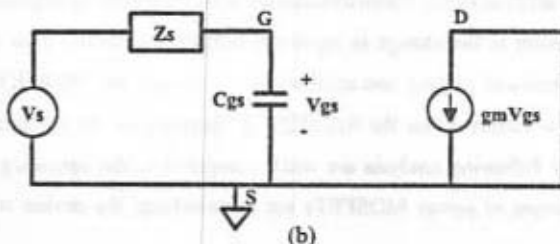
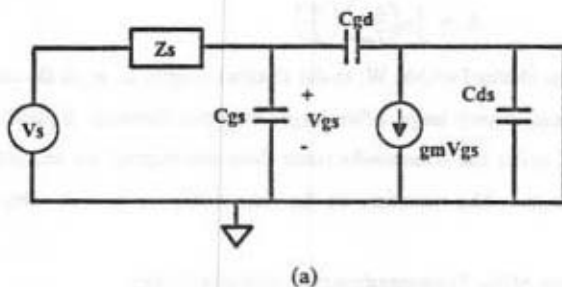


Figure 3 - Power MOSFET models used to describe the variation of the transconductance with frequency. (a) complete model showing all parasitics and (b) simplified model.

The drain-source capacitance, C_{ds} , is shorted while the gate drain capacitance, C_{gd} , is small compared to the gate-source capacitance so C_{gd} will be neglected. The result is shown in figure 3b. The gate-source voltage is given by

$$V_{gs} = \frac{V_i \cdot \frac{1}{j\omega C_{gs}}}{Z_i + \frac{1}{j\omega C_{gs}}} = \frac{V_i}{1 + j\omega C_{gs} Z_i} \quad (3).$$

The drain current is given by

$$i_d = g_m V_{gs} = \frac{g_m V_i}{1 + j\omega C_{gs} Z_i} \quad (4).$$

The dc value of the transconductance is given by the requirement $V_i = V_{gs}$. The effective transconductance as a function of frequency is then

$$g_{mf} = \frac{i_d}{V_i} = \frac{g_m}{1 + j\omega C_{gs} Z_i} \quad (5).$$

It will now be useful to explain the impact of (5) on circuit design. The impedance looking into the source of a power MOSFET is simply $\frac{1}{g_m}$ ¹. If the impedance Z_i is purely resistive, $Z_i = R_i$, then this impedance is given by

$$\frac{1}{g_{mf}} = \text{impedance looking in source} = \frac{1}{g_m} + j\omega \frac{C_{gs} R_i}{g_m} \quad (6).$$

That is, the impedance looking into the source of the MOSFET looks like a resistor of value $\frac{1}{g_m}$ in series with an inductor of value $\frac{C_{gs} R_i}{g_m}$. The impedance looking into the drain of a MOSFET is capacitive. If the MOSFETs are used in series the combination of the source inductance with the capacitance of the drain can cause ringing. If Z_i is inductive the impedance looking into the source will be negative which may result in oscillations. The input and output impedance of power MOSFETs will be discussed further in section 3.4.

2.3.3 Frequency Limitations and Parasitics

The most basic limiting factor in the speed of the device is the transit time of the electrons between the source and drain. This may be written as

$$\tau_{sd} = \frac{\text{length of channel}}{\text{electron velocity}} = \frac{l_c^2}{\mu_e \cdot V_{DS}} \quad (7)$$

where l_c is the length of the channel connecting the drain and the source, V_{DS} is the voltage between the drain and source and μ_e is the electron mobility. If V_{DS} is sufficiently large

¹ This is true for i_d approximately equal to i_s . The impedance looking into the source as frequency increases to infinity is Z_i .

so that the electrons travel at their saturated velocity of 10^6 ps/ μ m and the channel length is 1μ m then τ_{ad} is 10 ps. The cutoff frequency is $f_c = 1/2\pi\tau_{ad} = 16$ GHz. It should be pointed out that this is the cutoff frequency for a single cell. Since a power MOSFET is composed of hundreds or even thousands of unit cells the transit time across the die will be greater than 10 ps resulting in a lower cutoff frequency. To illustrate this consider a 1 cm by 1 cm die. The time it takes one electron to travel from one side of the die to the other is greater than 33 ps (i.e. $1\text{ cm}/(3 \times 10^{10}\text{ cm/s})$). Therefore, the intrinsic transit time of a power MOSFET will never be a concern when determining frequency response.

Another limiting factor is the gate contact resistance. The drain and source contact resistance in general do not have a significant effect on the cutoff frequency. The gate contact is formed using heavily doped polysilicon and the drain and source contacts are formed using aluminum. The drain and gate contact resistances are on the order of one-half ohm while the source contact resistance is typically 0.05 ohms. Because of the large capacitance present at the gate node, a large RC time constant is formed. The time constant encountered due to the drain contact resistance is significantly less. As an example consider $R_s = R_d = 0.5\ \Omega$ shown in figure 4.

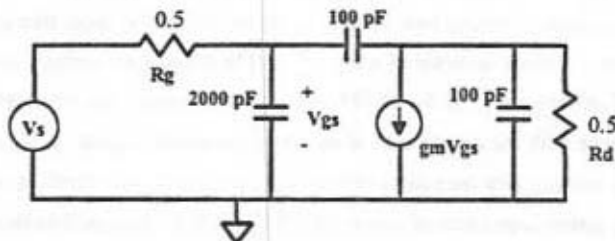


Figure 4 - Circuit diagram used to show that R_g has a more severe effect on the cutoff frequency than R_d . This is especially true when the Miller effect is present.

The input time constant is 1.1 ns (0.5×2200 pF) while the output time constant is 0.1 ns (0.5×200 pF). When a load is present, the time constant difference becomes even more significant. The importance of R_g in circuit design will become more apparent in the next chapter when discussing driving power MOSFETs.

The last limiting factor that will be discussed in this section is the lead inductance. A typical value of inductance in a TO-220 package is 5 nH and in a TO-247

package is 10 nH. The lead inductance is in series with each of the leads as shown in figure 5.

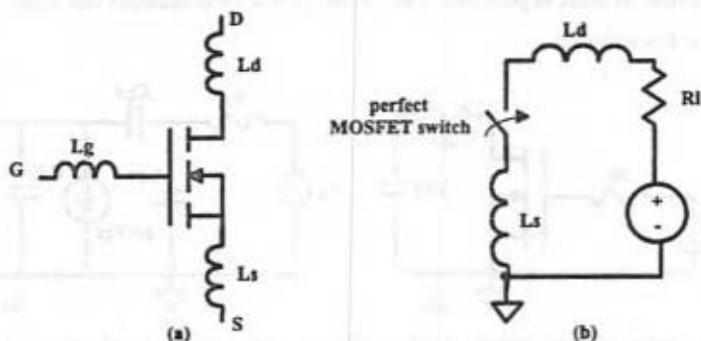


Figure 5 - (a) Shows how the lead inductance's affect the basic model and (b) shows that if the MOSFET switch could close infinitely fast the voltage across the load would rise at a rate of $2.2(L_d + L_s)/R_l$.

Figure 5b shows the most basic limiting effect of the lead inductance, that of slowing the risetime across the load R_l . If the MOSFET is modeled by the perfect switch shown in figure 5b, the risetime of the voltage across R_l is simply $2.2(L_d + L_s)/R_l$. The smaller R_l the slower the risetime due to the inductive effects. If $L_d + L_s = 10$ nH and $R_l = 50 \Omega$ the risetime is 0.44 ns. The main area where the inductance can slow the circuit down is in the gate driver. Especially troubling is the source inductance which acts to subtract from the effective gate driving signal. These effects will be discussed in greater detail in Chapter 3.

2.4 Switching Behavior

The switching behavior of power MOSFETs involves a transition between the cutoff, saturation and linear regions of operation. For the following analysis the following assumptions will be made; 1) when the MOSFET is in the cutoff region the drain current is zero, 2) when the MOSFET is operating in the saturation region the drain current is given by $g_m(V_{GS} - V_{th})$, and 3) the drain current in the linear region is $V_{DS}/R_{DS(on)}$.

The time difference between applying a gate drive signal and the drain current flowing is called the delay time. The delay time corresponds to the time the MOSFET is

in the cutoff region. The time it takes the drain current to transition from 10% to 90% of its final value occurs while the MOSFET is in the saturation region. The power dissipation will be the highest in this time interval so that an effort should be made to keep this time as short as possible. The MOSFET will be considered ON when operation lies in the linear region.

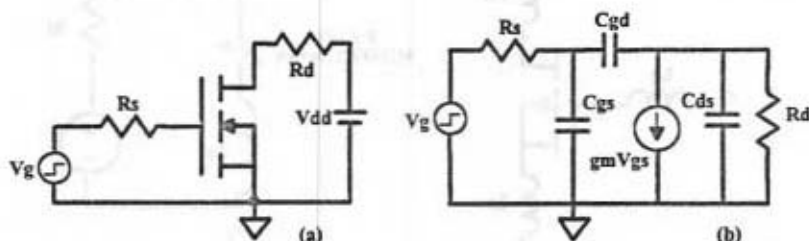


Figure 6 - (a) Circuit used to describe switching behavior and (b) model used in the saturation region.

Figure 6a shows the circuit configuration which will be used to describe the switching behavior. The model shown in figure 6b is used for operation in the saturation region. Before analyzing turn-on and turn-off, the effect of the device capacitances on switching performance will be discussed.

The capacitances in a MOSFET are partially due to the depletion regions present and partially due to the plate overlap capacitances. The depletion capacitances are a function of applied potential. The gate-source capacitance shown in figure 6b is essentially constant with applied drain or gate potentials. The gate-drain capacitance, C_{gd} , however is not. For a typical MOSFET switching circuit the potential across C_{gd} can range from 500 V to -20 V. The -20 V occurs when the MOSFET is on ($V_{ds} = 0$ and $V_{gs} = 20$). If a typical value of C_{gd} at 100V (gate to drain potential) is 50 pF then a typical value at -20 V may be 1000 pF. This becomes even more significant when the Miller effect² is considered. This increase in capacitance causes the pulse to "dribble up" to its final value. In other words the switching time (10% to 90%) of the circuit may be 3 ns

² The Miller effect may not be a concern when the drain-source potential is less than 20 V because the MOSFET may be entering the linear region (the gain decreases). With heavy loads, those requiring high currents, the Miller effect starts to decrease as the gate-drain capacitance increases.

while the pulse does not reach a steady state value until 50 ns. Usually with heavy loads this "dribble up" is not a problem.

Most manufacturers describe the above phenomena using the required charge, Q , to change from cutoff through saturation to the linear regions. The charge, Q_{g1} , required to change from the cutoff to the saturation region is given by

$$Q_{g1} = C_{gs} \cdot V_{th} \quad (8)$$

where V_{th} is the threshold voltage and it was assumed that $C_{gs} \gg C_{gd}$. The input capacitance C_{in} when the MOSFET is in the saturation region is given by

$$C_{in} = C_{gs} + C_{gd} \cdot \left(1 - \frac{\Delta V_{ds}}{\Delta V_{gs}}\right) \quad (9)$$

where the second term is the Miller capacitance. The main problem with this equation is that C_{gd} is not constant. However, if the range of operation is limited to between the 10% and 90% points C_{gd} is approximately constant. The charge, Q_{g2} , required to traverse this region is then

$$Q_{g2} = C_{in} (V_{g2} - V_{th}) - Q_{g1} \quad (10)$$

The gate voltage when the V_{ds} is 90% of its final value is V_{g2} . The gate charge required to cause the output to change from 90% to 100% of its final value is given approximately by

$$Q_{g3} = V_{gs} \cdot (C_{gdmx} + C_{gs}) - Q_{g2} \quad (11)$$

where V_{gs} is the peak driving signal and C_{gdmx} is the gate-drain capacitance with -20V drain to gate potential.

One last concluding remark concerning power MOSFET capacitance is that the power MOSFET data sheet does not usually contain numerical values for C_{gs} , C_{gd} , and C_{ds} . These capacitance's are given in terms of measured capacitances C_{iss} , C_{rss} and C_{oss} where

$$C_{iss} = C_{gs} + C_{gd}, C_{ds} \text{ shorted} \quad (12)$$

and

$$C_{rss} = C_{gd} \quad (13)$$

and

$$C_{oss} = \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} + C_{ds} \approx C_{ds} + C_{gd} \quad (14)$$

2.4.1 Analysis of Turn-on

The turn on delay time (figure 6b) is simply the time it takes V_g to charge C_{gs} through R_g to the threshold voltage. This time is given by

$$t_{delayon} = R_g C_{gs} \ln \left(\frac{V_g}{V_g - V_{th}} \right) \quad (15).$$

The risetime is given by

$$t_{rise} = R_g C_{gs} \ln \left(\frac{V_g - V_{th}}{V_g - V_{gs2}} \right) \quad (16).$$

This assumes that the R_d and $C_{ds} + C_{gd}$ time constant is much smaller than the input time constant. In most applications this will be the case. For example if $R_g = 5$ ohms, $R_d = 50$ ohms, $C_{gs} = 1000$ pF, $C_{gs} = 50$ pF, $C_{ds} = 50$ pF, $V_g = 20$ V and $V_{ds} = 500$ V then the input time constant is on the order of 10 ns while the output time constant is 0.5 ns.

2.4.2 Analysis of Turn-off

The turn-off delay is given by

$$t_{delayoff} = (C_{gdmx} + C_{gs}) R_g \ln \left(\frac{V_g}{V_{gs2}} \right) \quad (17)$$

and the falltime is given by

$$t_{fall} = C_{ds} R_d \ln \left(\frac{V_g}{V_{gs2}} \right) \quad (18).$$

These equations are approximations. To determine the delay, rise and fall times, experimental measurements offer the best results.

The results derived in this section are based on approximations and assumptions on the values of the junction capacitances. The results offer a quantitative explanation of power MOSFET switching. The best method of determining the characteristics of a MOSFET switching circuit is to build and test the circuit.

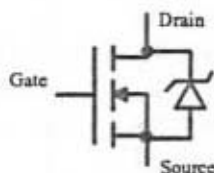


Figure 7 - Power MOSFET schematic symbol showing zener diode protection.

2.5 Maximum Voltage and Current Ratings

As was mentioned in Chapter 1 the source and channel are purposely shorted together to form a diode between the drain and the source. The diode acts as a zener diode protecting the MOSFET from overvoltages. The power MOSFET is often drawn schematically as shown in figure 7.

Overvoltages occur when the electric field, which extends between the drain and source while the device is in the saturation region, reaches a critical level such that impact ionization occurs (or in other words avalanche multiplication begins). If the external circuit load line is such that an abundance of current can flow when avalanche multiplication occurs the power dissipated may be enough to damage the device.

The maximum current rating of the device is limited by current crowding effects in the channel region. When the current density is large the α pinch effect will occur causing a constriction of current resulting in filaments and possible damage. Also large current densities combined with high electric fields cause over heating, damage and the drain to source ON resistance to increase.

One positive aspect of the drain to source ON resistance increasing is that it acts to lower the drain current by having a negative feedback effect and hence protecting the device. However, this effect has the undesirable consequence of increasing the i^2R power dissipation of the device.

2.6 Temperature Effects

The two main temperature effects of concern are the increase in $R_{\text{ds(on)}}$ and V_{th} with temperature. The decrease in the drain current with temperature can be related to both of these effects. The breakdown voltage also changes with temperature but the variation is usually negligible.

The increase in the drain-source resistance, $R_{\text{ds(on)}}$, causes the drain current and efficiency to decrease. Very little can be done to lower $R_{\text{ds(on)}}$ other than paralleling additional MOSFETs. When selecting a power MOSFET, $R_{\text{ds(on)}}$ will be a significant factor in the choice.

The variation of the threshold voltage with temperature will cause nonlinearities. As a simple example consider the design of a constant current source. If a constant gate-source voltage is applied, ideally the drain current will also be constant. However since the threshold voltage is a function of temperature and the device junction temperature is a function of drain current and drain-source voltage the drain current will not be constant. If a gate drive signal is applied which biases the MOSFET on the boundary between the linear and the saturation regions, heating of the MOSFET will cause the operating point to enter the saturation region. The result is a pulse with droop. Using the circuit shown in figure 6b with a marginal drive signal the voltage across R_d will look as shown in figure 8.

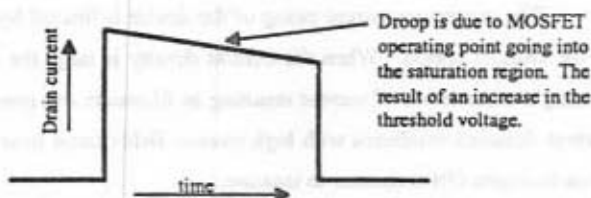


Figure 8 - Pulse resulting from a gate drive signal that does not force the MOSFET to stay in the linear region for all variations of the threshold voltage.

2.7 Modeling the Power MOSFET using SPICE

The main difference between the standard SPICE model and a model used to simulate power MOSFETs is the need for a more accurate representation of the device capacitances, inclusion of a drain-source intrinsic diode and the inclusion of lead inductances[11,12]. International Rectifier[11] even goes as far as listing model parameters on the data sheet. The standard SPICE model is used with the addition of the lead inductance, a capacitance in series with a voltage dependent voltage source between the gate and source and a diode between the drain and source (figure 9).

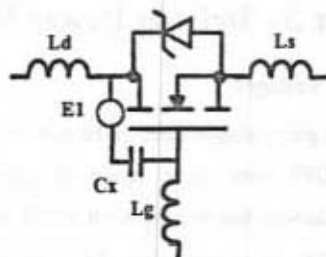


Figure 9 - Schematic diagram of SPICE power MOSFET model. The lead inductances, diode, capacitor C_x and voltage dependent voltage source are external to the intrinsic spice MOSFET model shown.

The need for the inclusion of the lead inductance and the diode are obvious from the physical construction of the device, however the inclusion of the voltage source and capacitor are not obvious. The drain gate capacitance becomes very large for small values of V_{ds} as was mentioned earlier. The majority of instrumentation applications of power MOSFETs can be accurately simulated using the lead inductance alone.

Chapter 3 - Driving Power MOSFETs

3.1 ON/OFF State Gate Voltages

The ON/OFF state gate voltages refer to the gate-source voltages required to keep the MOSFET ON or OFF over some range of drain-source voltage or device temperature. Chapter 2 showed that turning a MOSFET ON or OFF required a certain amount of charge supplied to the gate terminal. The gate drive signal will be modeled as shown in figure 1[1].

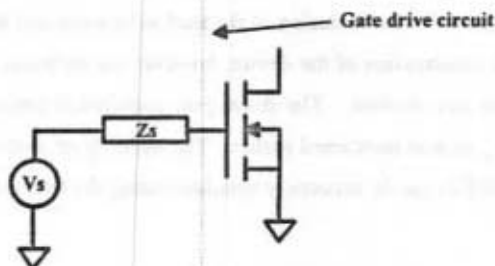


Figure 1 - The model used to describe the gate drive circuit of a power MOSFET. The source impedance Z_s may be a positive or negative resistance in series with an inductor or capacitor.

The ON state voltage should be low to maintain a high reliability while not so low that the MOSFET departs from the linear region into the saturation region. Selecting the ON state voltage is equivalent to selecting the steady state peak value of V_g . When the MOSFET is ON, V_g should be equal to the gate-source voltage V_{gs} . When this is not the case, the gate oxide has probably been damaged resulting in a large gate leakage current. The MOSFET may still function, as long as the gate driver can supply the needed current, but the device performance will be poorer. Often to obtain fast turn-on the drive signal has a significant overshoot on the leading edge to supply the needed charge to traverse the saturation region. The steady state value of the drive signal should be below the maximum gate-source voltage set by the manufacturer.

The OFF state voltage should be low enough that any transients occurring in the circuit do not cause the gate-source voltage to increase above the threshold. As an example consider the circuit in figure 1. If a large step voltage is applied to the drain of the MOSFET a voltage divider exists between the gate-drain capacitance and the source impedance Z_s . If Z_s is sufficiently large, the voltage on the gate may rise above the threshold voltage. This can be compensated for by lowering the minimum value of V_g . The penalty is longer turn-on delay time and possibly the need for a power supply voltage not available.

3.2 Problems and Limitations

The two factors limiting the switching speed of the power MOSFET are the input and the output time constants. The intrinsic speed of the MOSFET is negligible. The load is usually a fixed impedance (resistor, capacitor or combination of the two). The output time constant can be lowered by decreasing the load impedance. This in turn causes the MOSFETs to source more current. If a larger MOSFET is used to source the current needed by decreasing the load impedance the junction capacitances increase. When driving a $50\ \Omega$ load the output time constant is usually much smaller than the input time constant. The result is that in almost every case the input time constant is the speed limiting factor.

3.2.1 Lead Inductance

One major factor in limiting the switching speed on the input side of the circuit, other than the gate contact resistance and input capacitance time constant, is the source lead inductance. Consider the simplified schematic of the input structure shown in figure 2. The changing drain current will induce a voltage across L_s which will effectively subtract from the gate drive signal, assuming $\sqrt{R_s^2 + \frac{1}{\omega^2 C_s^2}} \gg |j\omega L_s|$.

As an example if the MOSFET must supply 20 A in 5 ns and the source inductance is 5 nH, then the induced voltage across L_s is 20 V. If the source driving voltage is a 20 V step then the effective voltage applied to the gate-source capacitance is zero. Of course if V_{gs} is zero then the drain current will not rise to 20 A in 5 ns but this example shows how the source inductance can slow the rate of charge transfer.

One solution to lowering the effect of the source inductance is to repackage the power MOSFET die. Directed Energy, Inc. [9] does this using a microwave type package and two source bonding wires that are mutually coupled. The two bonding wires gives a lower source inductance than the TO-220 package. One bonding wire is used for the source driving ground connection while the other is used for the load ground connection. The mutual coupling lowers the bonding inductance slightly, but this effect is usually negligible.

It will be shown that nanosecond switching times can be achieved using standard TO-220 and TO-247 packages if the gate driving circuit is designed properly.

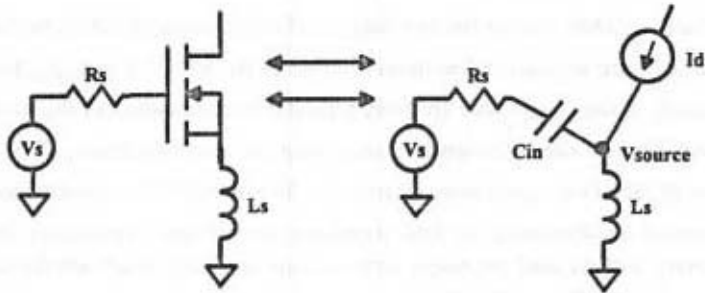


Figure 2 - Used to show the effect of the source lead inductance on the switching performance. The voltage induced across the source inductance subtracts from the gate drive signal.

3.2.2 Overdriving the Gate

The speed limitations due to the source resistance, input capacitance and source inductance can be eliminated by overdriving the gate. The input capacitance will charge to a higher value so the gate-source voltage needed for a specific drain current will occur earlier in time. The feedback effect due to the source inductance will subtract from a larger voltage so the maximum gate-source voltage will not be exceeded. Following the example given in the last section, if the peak voltage of the input signal source is 40 V then the actual applied signal is 20 V, which is sufficient to turn the MOSFET ON quickly (assuming the RC input time constant is small).

The major drawback of overdriving the gate is reliability. As the gate-source voltage is increased the lifetime decreases. The solution to the gate drive problem is to use a step signal with a significant amount of overshoot. The actual gate-source voltage will never reach the maximum of 20 V although the peak amplitude of the driver may be greater than 40V.

Consider the circuit shown in figure 3. This circuit is a representation of the impedance looking into the gate of the MOSFET. At low frequencies the effects of the capacitor dominate while at high frequencies the inductor impedance dominates.

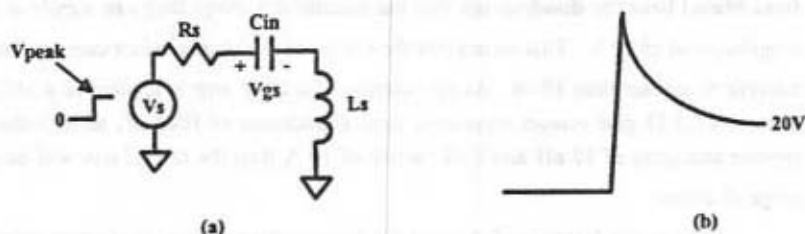


Figure 3 - (a) Circuit used to describe the input impedance of the power MOSFET and (b) the best type of drive pulse for fast turn-on. The gate-source voltage never increases above 20 V due to the charging of the gate-source capacitance and the feedback due to the source inductance.

When the source voltage switches high, the instantaneous voltage across R_s and C_{in} is zero while the voltage across L_s is V_{peak} . This causes a large constant current to flow in L_s . As time proceeds the voltage across L_s will decrease and across C_{in} will increase until it reaches V_{peak} . If the waveform shown in figure 3b is applied the gate-source capacitance will charge even faster.

3.3 Gate Drive Circuits

Gate drive circuits can be classified into four different categories; 1) integrated circuit drivers, 2) discrete circuit drivers, 3) linear drivers and 4) avalanche drivers. Integrated circuit drivers use commercially available integrated circuits to drive the power MOSFET. These integrated circuits are specifically designed to provide large amounts of current with a low source impedance, which is required for driving power MOSFETs. Discrete gate drive circuits use discrete transistors and possibly other

integrated circuits for driving the MOSFETs. Linear drivers may be integrated or discrete but are used for non-switching applications, i.e., amplifier or ramp generation. Avalanche drivers are popular because of their simplicity [7,13]. These drivers employ Avalanche transistors which have a negative output impedance during switching. The following subsections expand on the strengths and weaknesses of each of the above drivers.

3.3.1 Integrated Circuit Drivers

Integrated circuit drivers such as the DS0026 from Motorola and the MIC4420 from Micrel have the disadvantage that the maximum voltage they can supply is in the neighborhood of 20 V. This means that the effects of the source inductance can limit the risetime to greater than 10 ns. As an example, if a 20 V step is applied to a MOSFET gate with 0.5 Ω gate contact resistance, input capacitance of 1000 pF, series inductance (source and gate) of 10 nH and load current of 10 A then the rate of rise will be in the range of 10 ns.

Another disadvantage of the integrated circuit driver is the propagation delay time which can be as high as 50 ns with some drivers. Instrumentation usually requires low pulse jitter. Since pulse jitter is a function of delay the lower the delay the less jitter. Integrated drivers should be used when the risetimes required can be slower than 10 ns and simplicity is needed, i.e., small parts count. Generally speaking high performance instruments will not use IC drivers alone or will use them with other circuitry, such as an avalanche driver.

3.3.2 Discrete Gate Drive Circuits

The most common discrete gate drive circuits employ one or more emitter followers as shown in figure 4. Discrete drivers can suffer from the same low voltage problem as IC drivers and are often used with the IC driver to further lower the output impedance.

Although the output impedance of an emitter follower is low at low frequencies, as the frequency increases the impedance increases. This is due to the roll off of the transistor current gain with frequency. The current gain of a transistor is given by

$$\beta(f) = \frac{\beta_o}{1 + j\frac{f}{f_\beta}} \quad (1)$$

where β_o is the DC current gain of the transistor and ω_β is the frequency when the current gain is 3 dB down from the DC value. The output impedance of an emitter follower is

$$Z_{outEF} = \frac{1}{g_m} + \frac{Z_s}{\beta(f)} \quad (2)$$

where $g_m = I_c/0.026$ and Z_s is the source impedance. If Z_s is resistive then the output impedance looks like an inductor in series with a resistor. The impedance of the inductor can cancel the impedance of the capacitor for frequencies below resonance of the input capacitance of the MOSFET and the output inductance of the BJT. If the driver of Q1 in figure 4 is purely resistive then the output impedance of Q1 is inductive.

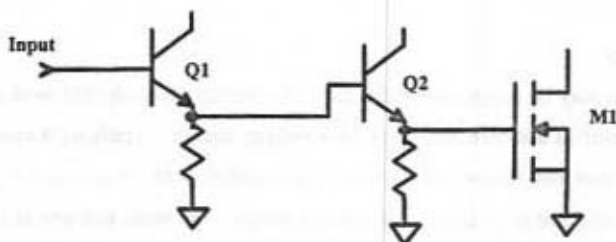


Figure 4 - Discrete gate drive circuit employing emitter followers. Care must be taken to avoid oscillations due to the possible negative output impedance of Q2.

Driving an emitter follower with an inductive source impedance gives a negative output resistance. Since the driving impedance of Q2 is inductive, the output impedance of Q2 has a negative component, that is, if the output impedance of Q1 is of the form $R_o + j\omega L$ then the output impedance of Q2 is

$$Z_{outEF2} = \frac{1}{g_m} + \frac{1}{\beta_o} \left(1 + \frac{j\omega}{\omega_\beta} \right) (R_o + j\omega L) \quad (3)$$

which is equal to

$$\frac{1}{g_m} + \frac{R_o}{\beta_o} + j\omega \left[\frac{R_o}{\beta_o \omega_\beta} + \frac{L}{\beta_o} \right] - \omega^2 \frac{L}{\omega_\beta} \quad (4).$$

The negative resistance is a function of frequency so that for very fast drive signals the source may look negative and cause ringing or oscillations. As the number of emitter followers increases the likelihood for problems increases as well. Often the solution to

oscillations or ringing is to add series resistance with the gate. Since the emitter follower is used to lower the source impedance, this resistance in series with the gate defeats the original purpose of using the emitter followers. In general, two emitter followers should be the maximum used.

Another discrete method of driving the gate is to use MOSFETs. A MOSFET is selected with a lower power rating and thus lower capacitance. Since the transconductance of the MOSFET is much lower than that of the comparable bipolar junction transistor the MOSFET driver requires more stages. This in turn increases the delay time through the driver. The next chapter will present the circuit design techniques used to design a MOSFET driver. The performance of these drivers in general is the best.

3.3.3 Linear Drivers

Linear drivers may be integrated or discrete. For instrumentation uses most often the linear driver consist of a switch and a constant voltage source. Applying a constant voltage between the gate and source will generate a constant current. A constant current can be applied to a capacitor to generate high voltage ramps. The main concern in linear applications is the variation of the transconductance with temperature. This may cause the drivers to change from a constant voltage source to one with a slight positive slope.

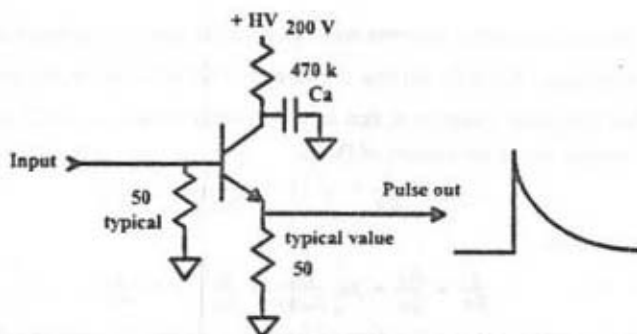


Figure 5 - Basic avalanche pulse generator.

3.3.4 Avalanche Drivers

Avalanche drivers are the most frequently used driver in instrumentation applications. Figure 5 shows the basic avalanche transistor pulse generator. Typical resistor values are listed as well. The avalanche transistor collector-base junction is in avalanche breakdown, typically 120 V for a 2N3904, with a small leakage current flowing through the junction. The large collector resistor limits the current flowing through the junction. The capacitor C_a charges up to the breakdown voltage of the transistor and is used to supply the charge needed to the MOSFET load when switching takes place.

When the base-emitter junction becomes forward biased the collector current will increase. Since the collector-base junction is avalanching, the increased collector current will be multiplied by the avalanche effect. The result is second breakdown [13] and a very quick (< 1 ns) decrease in collector-emitter voltage. If the circuit shown in figure 5 employs a 2N3904 transistor the risetime across the $50\ \Omega$ load will be less than 2 ns with an amplitude greater than 100 V.

With the help of figure 6a an understanding of the avalanche driver may be gained.

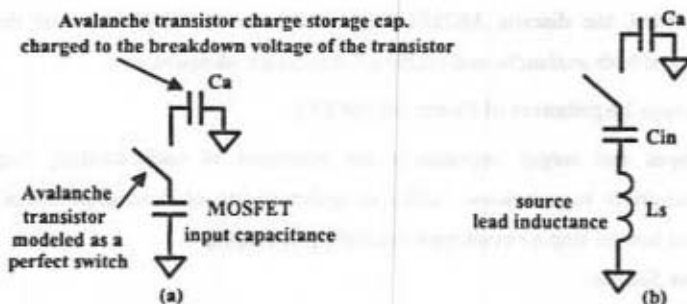


Figure 6 - (a) Basic capacitive voltage divider where the avalanche transistor is treated like a perfect switch and (b) adding the effect of L_s causes the effective voltage applied to C_{in} to increase.

To calculate the voltage across the MOSFET input capacitance, assuming C_a has an initial voltage of V_B (the breakdown voltage of the avalanche transistor), a capacitive voltage divider is used, or

$$V_{in} = V_B \cdot \frac{\frac{1}{j\omega C_{in}}}{\frac{1}{j\omega C_{in}} + \frac{1}{j\omega C_a}} = V_B \cdot \frac{C_a}{C_a + C_{in}} \quad (5).$$

Solving this equation, the correct value of C_a may be picked to limit the gate drive to less than 20 V. If the source inductance is added as shown in figure 6b the added impedance will cause the voltage applied to the gate to increase. The voltage across the gate source oxide will remain below 20 V. The avalanche transistor, in effect, compensates for the lead inductance. This coupled with the fact that the output impedance is negative make the avalanche transistor extremely useful for fast switching. The main drawback is a limit on the repetition rate for avalanche transistors. Because second breakdown can be destructive, the amount of energy the transistor delivers is limited.

Another problem is the tendency for the gate to discharge back through the avalanche transistor emitter resistor. This problem can be solved by using an integrated circuit driver with an avalanche driver. In general, if simplicity is needed the avalanche transistor is the preferred driver however, if reliability, repetition rate and pulse width control are needed, the discrete MOSFET driver is desirable. With proper design switching times of both avalanche and MOSFET drivers are identical.

3.4 Input/Output Impedances of Power MOSFETs

The input and output impedances are important in understanding ringing, oscillations and driver requirements. Often an understanding of these impedances will tell the designer how to stop a circuit from oscillating or ringing.

3.4.1 Common Source

The common source input impedance is mostly capacitive. When the MOSFET is in the cutoff region the input capacitance is C_{gs} . While in the saturation region the input capacitance is $C_{gs} + (g_m R_L + 1)C_{gd}$. The value of C_{gd} in the saturation region is fairly constant and much less than C_{gs} . When the MOSFET enters the linear region the input capacitance is approximately $C_{gs} + C_{gd}$. Where C_{gs} and C_{gd} are approximately the same.

The output impedance is capacitive as well. The value of capacitance is $C_{gs} + C_{ds}$. Both C_{gs} and C_{ds} increase dramatically as the drain source voltage becomes small, (the depletion regions become narrow), which typically occurs below 20 V. The biggest effect is the decrease in the turn-off time. Also any inductances present in the circuit can cause oscillations in the presence of these large capacitances.

3.4.2 Common Gate and Common Drain

The impedance looking into the drain of the common gate or drain configurations is capacitive. The value of this capacitance is $C_{gs} + C_{ds}$ and is the same as the common source case. The big difference comes from the impedance looking into the source. This is the input impedance for the common gate case and the output impedance in the common drain case. This impedance is inductive and a function of the source driving resistance. This impedance was shown in section 2.3 to be

$$Z_o = \frac{1}{g_m} + j\omega \frac{C_{gs}R_s}{g_m} \quad (6)$$

assuming the source driving impedance is purely resistive. If a MOSFET source follower is driving a common source amplifier, the result will be a tank circuit as shown in figure 7. This setup will make attaining clean waveforms difficult. Often to avoid ringing in the output pulse a series resistor is added which decreases the Q of the resonator.

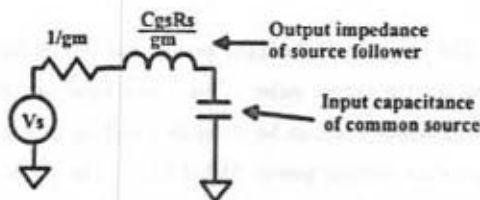


Figure 7 - This circuit shows that the output impedance of an source follower driving a common source amplifier will look like a series resonant circuit with the resonance a function of the source impedance.

At the resonant frequency the source will drive a resistor of value $\frac{1}{g_m}$ and the LC tank will look like a short.

Chapter 4 - Circuit Design

4.1 The Basic Switch

The basic MOSFET [7] switch using an avalanche driver is shown in figure 1. When an input trigger is applied to the circuit, the 2N3904 operating in the avalanche mode dumps the charge stored in the collector capacitor into the gate of the MOSFET and the $510\ \Omega$ load at the emitter.

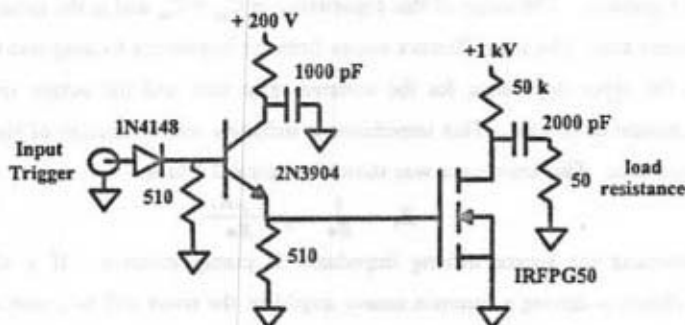


Figure 1 - The basic MOSFET switch using an avalanche driver. The $510\ \Omega$ resistors are picked so that the leakage through the transistor is not large enough to cause a significant voltage drop at the base or the emitter.

The charging of the input capacitance in this fashion rapidly turns the MOSFET ON creating the output pulse. The lower limit on the load impedance is set by the amount of power that can be dissipated without destruction. The upper limit is not a concern when driving power MOSFETs. The value of the collector capacitor was determined using the method presented in the last chapter. The output of this pulse generator is an 800 V pulse with a risetime of 3 ns [7].

4.1.1 Selecting the Package

There are basically two types of packages in which power MOSFETs are sold; 1) the TO-220 and 2) the TO-247. The advantage of the TO-247 package is better heat dissipation. This means that the thermal problems discussed earlier are less significant when compared with the TO-220 package. The higher power MOSFETs are generally

packaged in the TO-247. The main disadvantage of the TO-247, compared to the TO-220, is the larger lead inductances (typically 10 nH for the TO-247 and 5 nH for the TO-220).

Power MOSFETs can also be purchased from Directed Energy, Inc. with lead inductances about 3 nH area at a much higher cost. Generally speaking, it is more cost effective to buy the TO-220 or TO-247 package and design around these inductances.

4.1.2 Board Layout

There are two main concerns when laying out a printed circuit board for a MOSFET pulser. The first is the inductance connecting the leads of the MOSFETs. The bottom of the MOSFET package should sit snug with the top of the board in order to minimize the lead inductances. The MOSFETs should be placed as close together as possible to minimize the trace inductance between the devices. Also a good ground plane is mandatory for any high speed circuit, especially when high power is used.

The second concern is power dissipation. It may be necessary to fasten the MOSFETs to the board so that the board can be used as a heat sink. The stray capacitive effects are negligible due to the large parasitic capacitances of the MOSFET. However, if a very large area of the board is used as a heat sink and the board contains a ground plane then this stray capacitance may not be negligible.

4.2 High Repetition Rate Pulse Generation

Pulse generators using avalanche drivers are generally limited to repetition rates less than 1 MHz. To attain higher repetition rates integrated circuit or discrete drivers must be used with lower junction capacitances and lower lead inductances. Since lowering the junction capacitance would mean using a lower power MOSFET and the rating of the MOSFET is usually set by the output current drive requirements, this is not possible. Also using a repackaged MOSFET is expensive and therefore undesirable. One solution is to use a cascode configuration. A lower power MOSFET is used to control the current through a higher power MOSFET. The lower power MOSFET may have an input breakdown voltage rating of 60 V and thus much lower junction capacitance. The problem of the lead inductance is solved by introducing a delay

between the low power MOSFET turning on and the high power MOSFET turning on. If the transients in the low power MOSFET have died out before the high power MOSFET starts to turn on the high power MOSFET will switch on in a time limited only by the inductance of its drain lead and the output time constant.

4.2.1 The Cascode Configuration

The cascode configuration [14] can be used to attain switching frequencies approaching 50 MHz. The main limitation in most cases is the driver and not the MOSFETs themselves. The basic cascode MOSFET pair is shown in figure 2.

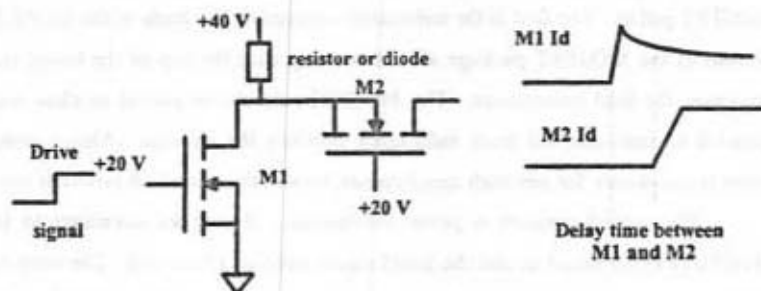


Figure 2 - Cascode configuration. The drain current in M1 rises and peaks before the drain current in M2 starts to increase. Since there are no current transients across the source inductance of M1 no voltage is induced. The main criteria is that the drain current in M1 be larger than the final drain current of the pair before M2 starts to turn-on.

When the cascode configuration is in steady state, the source of M2 is at a 40 V potential while the gate is at 20 V, i.e., the gate-source potential is -20 V. When M1 starts to turn on it sees the large gate-source capacitance of M2 as its load. The drain current in M1 will increase as fast as its source inductance will permit. If the drain current in M1 reaches a constant value larger than the final value of the drain current before M2 starts to turn on, the source inductance of M1 will have no effect on the switching time. Also because a current is being drawn through the source inductance of M2 which is larger than the final drain current, this inductance will have no negative effect. The only inductance which will affect the risetime will be the drain inductance. If the right MOSFETs are picked, the 40 V bias is needed only to protect the gate-source

oxide of M2, i.e., the capacitive voltage divisions will cause the source of M2 to increase above the 40 V maximum recommended by manufacturers (20 V between the gate and source). An example of a cascode pulse generator is given in section 5.2.1.

4.3 Series Operation

Figure 3 shows a reliable method of stacking power MOSFETs [15,16]. The resistor values are not critical and are used to set the dc operating voltages. Since the main cause of failure when using power MOSFETs is exceeding the maximum gate-source voltage specification (typically ± 20 V) care must be taken when using the MOSFETs in series. The circuit shown in figure 3 relies on a voltage division between the effective gate source capacitances of M2 and M3 with the voltage across C2 and C3 to stay below 20 V. A properly designed circuit will force all of the MOSFETs to turn on at the same rate.

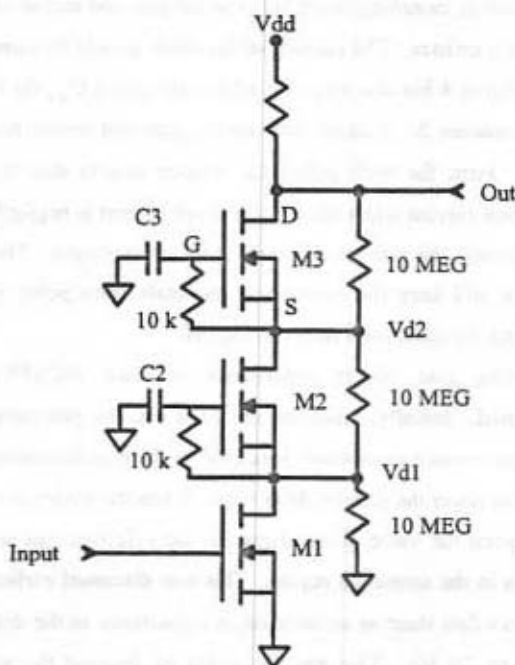


Figure 3 - Reliable method of stacking power MOSFETs.

When M1 turns on the voltage change on the drain divides across the effective gate source capacitance of M2, C'_{gs2} , and the capacitor C2. The change in voltage between the gate and source of M2, ΔV_{gs2} , is given by

$$\Delta V_{gs2} = \Delta V_{d1} \cdot \frac{C_2}{C_2 + C'_{gs2}}, \quad (1)$$

where C'_{gs2} is given by

$$C'_{gs2} \equiv C_{gs2} + A_{V2} \cdot C_{gsd2} \quad (2)$$

The gain, A_{V2} , is determined by the ratio of the change in drain-source voltage to the gate-source voltage change. Similar equations may be written for M3 with the main difference being $V_{d2} = 2V_{d1}$. This results in $C3 \equiv \frac{1}{2} C2$. If four MOSFETs are used then $C4 \equiv \frac{1}{3} C2$, or in general $Cn = \frac{1}{N-1} C2$. Most data sheets supply values for C_{gs} , C_{gd} and C_{oss} and as noted before for power MOSFETs $C_{gs} \approx C_{gs}$ and $C_{gd} = C_{gsd}$.

A zener diode or switching diode between the gate and source of M2 and M3 can be used in place of a resistor. The cathode of the diode should be connected to the gate of the MOSFET (figure 4 but also note that when calculating C'_{gs2} the diode capacitance will be added in equation 2. A diode between the gate and source has two advantages over the resistor. First, for wide pulses the resistor acts to shut the devices off by drawing a conduction current while the diode leakage current is negligible. Secondly, a zener diode will protect the gate-source oxide from overvoltages. The disadvantage of the diode is that it will keep the gate-source terminals from going negative and thus hindering or keeping the stack from fully turning off.

The effective gate source capacitance of each MOSFET changes with drain-source potential. Initially, when the device is off, the gate-source capacitance is simply the static gate-source capacitance specified on the manufacturers data sheet. This smaller value acts to lower the turn-on delay time. When the device is on the capacitance increases well beyond the value given above for the effective gate-source capacitance while the device is in the saturation region. This was discussed earlier and can be seen on the manufactures data sheet as an increase in capacitance as the drain-source voltage becomes smaller (< 20 V). This has the effect of limiting the voltage across the

gate-source oxide resulting in a built in protection mechanism, i.e., equation 1 will automatically limit ΔV_{gs2} to less than 20 V even for poorly picked gate capacitors.

For the circuit of figure 4, the gate capacitor current and the MOSFET gate electrode current are the same. This same current flows into the gate of each MOSFET in figure 4, while the current flowing in each of the capacitors has changed. If the current flowing into the MOSFET gate is I , then a current $2I$ flows through $2C$, $3I$ through $3C$ where C is determined by the method given above. The advantage of this configuration is a simpler board layout and a relaxed specification on the working voltage of the gate capacitors.

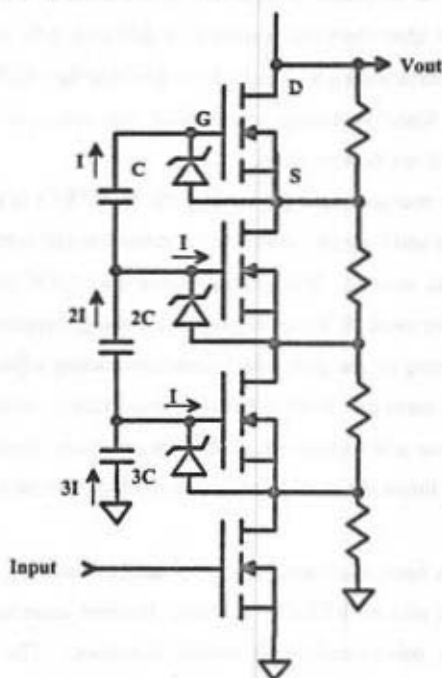


Figure 4 - Alternate method of stacking power MOSFETs.

As an example, an 8 kV MOSFET stack was recently described [8] for re-referencing the beam potential in ion beam experiments. Using the method presented

above (figure 3, to perform a similar function would require gate capacitors with working voltages up to 8 kV. This type of capacitor may not be readily available in the capacitance value needed for the design. With the design presented here 1 kV ceramic capacitors can be used. These are available in a wide variety of values. An alternative would be to parallel a single value of capacitance until the desired value is reached. Also, since the MOSFETs must be arranged in a stack, the gate capacitors in a stack do not complicate board layout.

The main disadvantage of this method occurs when trying to apply it to linear applications, e.g. ramp or amplifier design. In practice each MOSFET has slightly different current-voltage characteristics resulting in differing gate currents which will lead to different drain source voltages. The end result is that the MOSFETs will not turn on at the same rate. Since switching applications are nonlinear the differences in drain-source voltages will not be a problem.

The value of the resistors used for biasing the MOSFETs is not critical, but the wattage is. The wattage and type of the resistor is related to the maximum voltage that can be applied across the resistor. When using higher than 500V MOSFETs, one watt carbon resistors should be used. It is best to place the biasing resistors between the drain and source to avoid biasing on the gate side. Gate side biasing adjusts the drain source voltage as the MOSFET turns on. It should also be noted that no additional protection is needed between the drain and source due to the integral body diode present in power MOSFETs. This diode limits the maximum potential which can be applied between the drain and source.

This method has been used successfully to design many different types of high voltage pulse generators with no MOSFET failures. In some cases the MOSFET strings can be used to replace tubes performing similar functions. The advantages of the MOSFET when compared to a tube are unlimited lifetime when properly operated, lower power dissipation and faster switching speed. This represents a new area for follow-up yet to be explored.

4.3.1 Linear Amplifier

When using the series configuration of power MOSFETs the main concern is forcing the power MOSFETs to all turn on at the same rate. This is important for linearity. Since the MOSFET will be in a linear range for gate source voltages greater than 10 V, in general, the design procedure given in the previous section must be modified. This means using 10 V for the maximum gate-source voltage rather than the 20 V typically used for switching applications.

4.3.2 Causes of Oscillations

Because typically the impedance looking into the source looks inductive when driven with a resistive load and the impedance looking into the drain of a power MOSFET looks capacitive, series operation of MOSFETs tends to cause ringing on the output pulse. One solution to this problem is to add series gate resistance to dampen the ringing (lowers the Q of the resonant circuit). A better solution is to insure that the gate capacitors have a very good ground connection and short lead lengths, and to insure that the MOSFETs are very close together. Lowering the inductance present will push the resonant frequency up. This combined with the other reactance present in the circuit should keep ringing from becoming a problem.

4.4 Capacitive and Resistive Loads

The type of load driven will in general be the deciding factor for the power MOSFET used. For a resistive load ohms law is used to determine the peak current sourced. For a capacitive load $i = C \frac{dv}{dt}$ is used to determine the peak current needed. For example, if a 10 pF load is to be driven to 2,000 V in 2 ns the current needed is 10 A.

It is a good idea to put a resistor in series with a capacitive load. The resistor helps to damp the ringing that might occur when connecting to the capacitor through a wire. The value of the resistor is picked such that the needed risetime is much less than the $2.2RC$ risetime associated with the series resistor and load capacitor. Also the resistor helps protect against short circuit destruction of the last MOSFET in the stack. In other words since the load capacitance and the interconnecting inductance form a resonant circuit the output MOSFET may drive a short circuit during switching. If the MOSFET stack is driving 2 kV into the capacitor the resulting current sourced by the last

MOSFET in the stack may be enough to destroy the device. Adding the series resistor simply limits the amount of current the stack can source. Generally speaking 50 ohms is a good value.

4.5 Nonlinear Transmission Lines

There are many applications which require pulses with amplitudes greater than several hundred volts and risetimes in the picosecond regime. However, many instruments are limited in their measuring capabilities by the speed of the gating or sampling pulse used. This section presents a technique by which nanosecond risetimes can be changed into picosecond risetimes while maintaining the general shape of the pulse. This will increase the bandwidth of measuring systems by allowing shorter gating and faster turn-on time. The output of a power MOSFET pulse generator is fed to a nonlinear transmission line (NLTL) [21-25] and sharpened to the desired risetime.

4.5.1 Review of Nonlinear Transmission Line Operation

The basic idea behind a NLTL[21] is that the velocity of propagation at a point on the NLTL depends on the voltage at that point. Referring to figure 5, if the velocity of the wave at the 10% voltage point is slower than the velocity at the 90% point, where the risetime is the time difference between these points, the 90% point "catches up" with the 10% point, in effect speeding up the rising edge of the pulse.

The velocity of propagation along a transmission line is $\frac{1}{\sqrt{LC}}$ where L and C are the inductance and capacitance per unit length of transmission line. Consider the circuit shown in figure 6a and its equivalent circuit shown in figure 6b. The diodes are always reverse biased. The capacitance of a diode is a function of the reverse potential across it and for an abrupt junction is given by $C_d = \frac{C_p}{\sqrt{1 + \frac{V_d}{\phi}}}$ where C_p is the zero bias depletion capacitance, V_d is the magnitude of the reverse voltage across the diode and ϕ is the junction potential. The capacitance of the diode at the 10% and 90% voltage points will be called C_{d10} and C_{d90} respectively. Therefore the velocity of the pulse at the 10% point is $\frac{1}{\sqrt{LC_{d10}}}$ and at the 90% point $\frac{1}{\sqrt{LC_{d90}}}$. Similarly the decrease in risetime per section (DRPS) is equal to the delay difference at the 10% and 90% points or

$\sqrt{LC_{d90}} - \sqrt{LC_{d10}}$. Note that if this were a normal transmission line where the capacitance and inductance per section were constant the DRPS would be zero. If the delay is 20 ps/section (one section consisting of a single inductor and diode) and it is desired to change a 1 ns risetime pulse into a 500 ps risetime, then 25 sections are needed. The DRPS can be increased by using larger value inductors or selecting a diode with a large $C_{d10} - C_{d90}$.

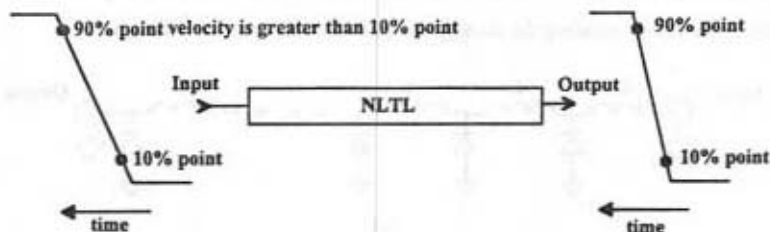


Figure 3 - Shows that if the velocity of the wave at the 90% point is greater than the velocity at the 10% point the output risetime will decrease.

This periodic structure has a Bragg cutoff frequency [22-24], f_c , given by $\frac{1}{\pi\sqrt{LC_p}}$.

This cutoff frequency puts an upper limit on the DRPS. The minimum risetime is $t_m = 0.35/f_c$ at the Bragg cutoff frequency, and there will be significant ringing in the output pulse. When generating an impulse this ringing can be used to generate larger amplitude signals then would be achieved if f_c were not the dominant effect. In general, for clean pulses, the output risetime should be at least twice as long as t_m .

Another concern is the diode series resistance and junction capacitance time constant. The diode series resistance consists of the ohmic contact resistance and the resistance of the lightly doped region between the p- and n-type semiconductors. The contact resistance is typically less than 0.3 Ω while the resistance of the lightly doped bulk region is typically 10 Ω . When the diode capacitance is 20 pF a small signal time constant of 200 ps is introduced. In practice the diode cutoff frequency has little effect when sharpening high voltage signals due to the small value of junction capacitance (on the order of 1 pF) at the 10 % voltage point of the pulse. Because the resistance of the

lightly doped bulk region will decrease with increasing reverse potential the practical time constant of the diode is 20 ps.

One practical limitation on this technique is the breakdown voltage of the diodes used. It is difficult to find diodes with breakdown greater than 1.5 kV and a low series resistance. The pulse traveling on the NLTL tend to have overshoot and ringing. The overshoot can cause the potential on the line to become several hundred volts larger than the input signals. The result is breakdown and destruction at various points on the line. When this occurs locating the damaged diode or diodes can be difficult.

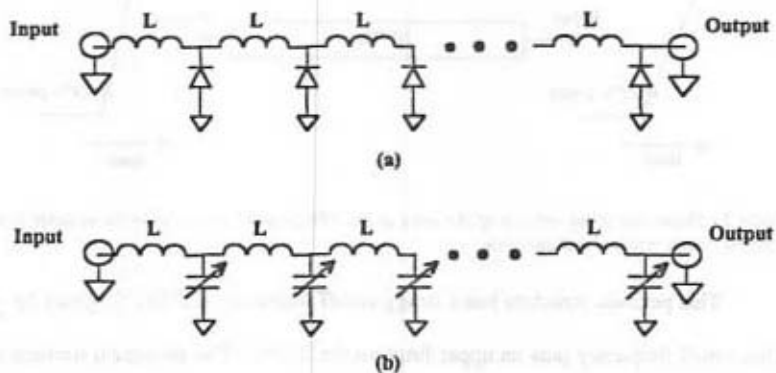


Figure 6 - (a) Circuit diagram of the nonlinear transmission line and (b) equivalent circuit when the diode behaves like a variable capacitor.

4.6 Designing a Nonavalanche Power MOSFET Driver

Several of the pulse generators presented in Chapter 5 use avalanche drivers. This is due to the simplicity of the avalanche driver. Drivers using discrete transistors can be used as well. The drawback to these drivers is more complicated circuit design and the need for more than one supply voltage.

From the discussion of gate drive circuits given in Chapter 3 the peak voltage applied to the gate lead must be larger than 20 V to attain <5 ns switching times. This means to protect the gate-source oxide, some sort of capacitive voltage divider must be used so that when the source lead inductance effects have decreased the gate voltage is below 20 V.

Consider the circuit shown in figure 7. The bipolar junction transistor holds the input of the DS0026 at approximately 5 V. The input high current of the DS0026 is 15 mA. Since the output of the DS0026 is the logical opposite of the input the output of the device is approximately 0 V. The drain of M1 is 100 V and the drain of M2 is 0V.

Applying a 5 V pulse to the input of the driver causes Q1 to turn-on. The input of the DS0026 goes low causing the output to go high. The 20 V pulse out of the DS0026 causes M1 to turn-on, this in turn causes M2 to turn-on, generating an output drive pulse.

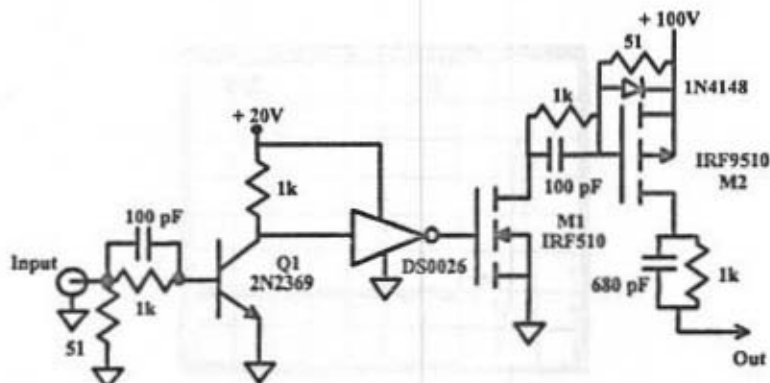


Figure 7 - Discrete MOSFET driver without avalanche transistors.

The capacitors between MOSFETs are picked as discussed before. For example, suppose the effective input capacitance of the power MOSFET that will be driven is 2,000 pF then 100 V divided between 680 pF and 2,000 pF will limit the drive signal to 20 V. The DS0026 can be replaced with a PNP transistor. This may be desirable if low propagation delay and the generation of narrow pulses is required. That is to say since the DS0026 stops working with an input pulse less than 20 ns in width it may often need to be replaced.

The output of the circuit shown in figure 7 driving an IRF740, i.e. the gate of the IRF740, is shown in figure 8. Notice how the source inductive effects cause the initial voltage to increase well beyond the 9 V steady state level. This large initial pulse causes

a large current to flow in the source inductance helping to speed up the turn-on. Note at no time is the actual gate-source voltage above the 20 V maximum.

The driver shown in figure 7 works well for turning a power MOSFET on, but does not work well for turning the MOSFET off. A mirror image of this driver with opposite polarity MOSFETs and supplies may be used to turn the power MOSFET off. The advantage of this type of circuit is that very high voltage square pulses can be generated and then controlled with a 5 V pulse.

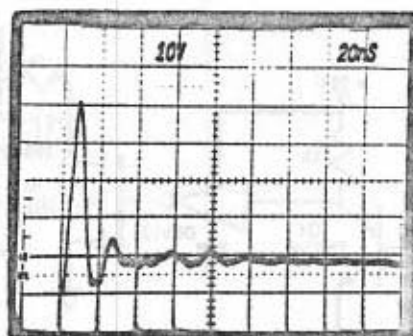


Figure 8 - Voltage waveform at the gate of a power MOSFET. Initially the gate potential is zero volts. The 30 V pulse is the result of the source lead inductance increasing the input impedance of the power MOSFET. Notice how the steady state voltage is approximately 10 V.

Chapter 5 - Experimental Results

5.1 Introduction

This chapter presents the experimental results of this dissertation. The chapter differs from the preceding chapters in that it is based solely on results from circuits that were built and tested. The designs presented here are based on the theory presented earlier. The circuit designs are original and were picked to represent the general applications of power MOSFETs to the design of electronic and electrooptic instruments. Inductance in these circuits were avoided by keeping lead lengths short. Average power dissipated was low to avoid thermal problems.

One of the major advantages of power MOSFETs is their linearity. The first section presents a variable width 500 V pulse generator. The width is varied by a +5 V pulse from a logic gate or some other low voltage pulse generator. In the past a pulse forming line was used to determine the pulse width in tube based pulse generators. To change the width of the pulse required changing the length of the pulse forming line.

Sections 5.3 and 5.4 present higher voltage pulse generators. These pulse generators are finding more and more uses in electro-optics [18]. The width of the pulse generated in these cases can be varied by following the techniques presented in chapter 3.

Because of the widespread use of these circuits, the majority of the results in this chapter have been published by the author elsewhere [14-18].

5.2 Variable Width Square Wave 500 V Pulse Generator

Before presenting a 500 V variable width pulse generator, applications of this type of pulse generator will be discussed. Many pulsed power sources are tubes. The thyratron is a good example of a tube used to generate very high voltages and/or currents. The thyratron requires a high level drive signal, greater than several hundred volts in most cases. Using tubes such as the spark gap or krytron limit applications to nonlinear uses, i.e., switching only. The MOSFET driver is a good replacement in some cases for these driver signals. Another area where this pulse generator may find use is in gating microchannel plate image intensifier (MCPI) tubes. The MCPI is a device which

accelerates and multiplies an incident electron producing many more electrons. An MCPIC can be used as a high speed shutter for high speed photography. The pulse generator is also used in beam modulation experiments [5,6].

5.2.1 Cascode Connected Power MOSFETs

Figure 1 shows a schematic diagram of a pulse generator using cascode connected power MOSFETs M1 and M2 [14]. The output of this generator into a $50\ \Omega$ load is shown in figures 2 and 3. The leading edge transition duration is 2 ns, while the trailing edge transition duration is 8 ns. A grounded source configuration using the IRF840

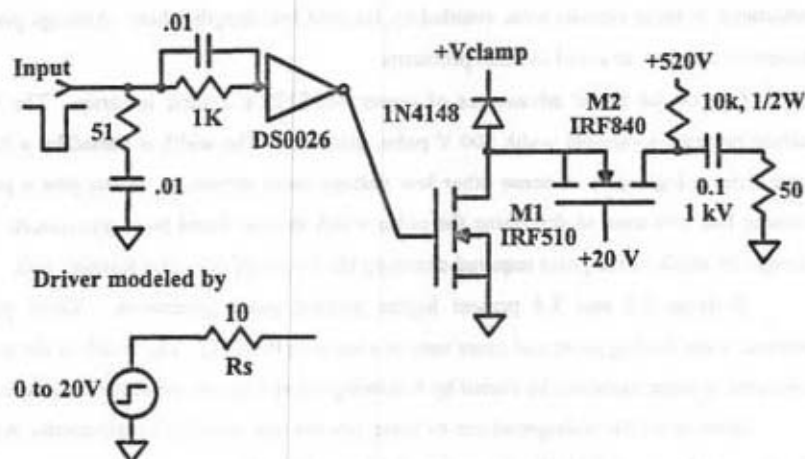


Figure 1 - Pulse generator using cascode connected power MOSFETs. The DS0026 is a common integrated circuit for driving power MOSFETs. The DS0026 is modeled by a 20V step generator with 10 ohm series resistance.

alone produced switching times of 18 ns and 65 ns for the leading and trailing edges respectively. The cascode connection reduces the input capacitance which must be driven. This is accomplished by (1) using and driving a lower breakdown voltage FET, and thus lower input capacitance and (2) eliminating the Miller effect.

The operation of the circuit is as follows. The driving source voltage, which is modeled by the 0-20 V step generator with 10 Ω source resistance¹, switches on and

¹ The DS0026 risetime is rated at 20 ns into a 1000 pF capacitor. If $t_r = 2.2RC$ the R is determined as approximately 10 ohms. This assumes the driver and capacitive load can be modeled by a simple one-pole circuit.

starts charging the input capacitance of M1 (~ 200 pF) through R_s (10Ω). This causes the drain current of M1 to increase. If the drain potential of M1 is 40 V, M2 will start to turn on a finite time after the drain current in M1 increases. Establishing a

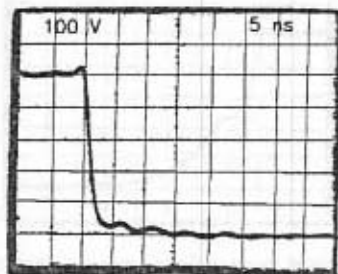


Figure 2 - Output of cascode circuit in figure 1. The leading edge is approximately 2 ns while the vertical is 100 V/div and the horizontal is 5 ns/div.

large drain current in M1 before M2 switches on can be used to cause M2 to switch on in a time limited approximately by the devices lead inductance. The cost for faster

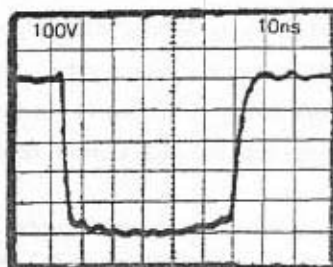


Figure 3 - Same trace as figure 2 except longer sweep.

switching time is longer delay. The delay between M1 turning on and M2 turning on can be adjusted using V_{clamp} . Connecting the diode clamp to +20 V, that is to the gate of M2, gives an output as shown in figure 4.

The main cause of failure in power MOSFETs is perforation of the gate source silicon dioxide layer. This failure occurs when the gate source potential exceeds the

manufacturer's specification (typically $\pm 20V$). For the circuit shown in figure 1 the drain of M1 should be at a potential of less than or equal to 40 V.

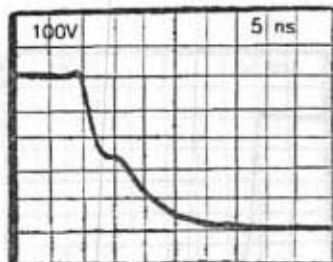


Figure 4 - Output of cascode pulser shown in figure 1 with V_{supply} tied to +20 V. The hesitation shown is the result of the drain current in M2 catching up with the drain current of M1.

5.2.2 Switching Analysis

Figure 5 shows an approximate circuit model for the circuit shown in figure 1. The transconductance is assumed linear for each MOSFET past its threshold voltage. The capacitances are nonlinear functions of applied voltage, but for this analysis will be assumed constant. The voltage on the drain of M2 after power is applied will be given, to a first order, by the voltage division of r_{ds1} and r_{ds2} . If these two resistance's are approximately the same, this voltage is limited by the breakdown voltage of M1, or approximately 100V. In either case, the diode clamp is needed to protect the gate-source SiO_2 interface of M2.

The current flowing in the pair after switching takes place is 10 A (500 V/50 Ω). Establishing a drain current of 15 A in M1 before M2 switches on will cause M2 to switch on limited only by the inductance of its drain lead and the output time constant. This figure of 1.5 times the final drain current was determined through experimentation and simulation. MOSFET M2 starts to switch on when the gate-source voltage becomes greater than V_{th} , assumed in the following to be equal to 4 V, i.e., when the drain of M1 becomes less than 16 V.

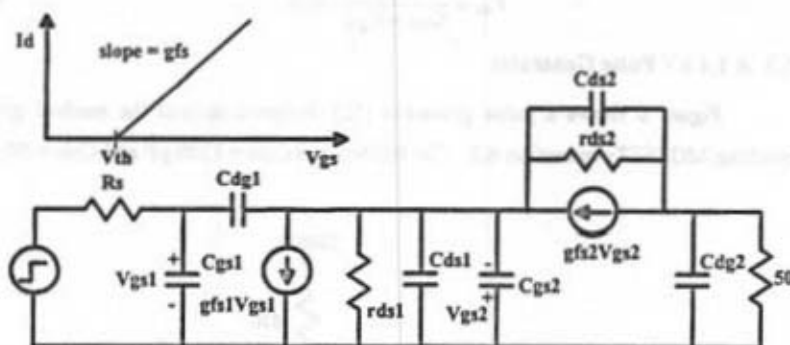


Figure 5 - Model used to describe switching behavior of cascode pulse generator shown in figure 1. The transconductance is assumed linear beyond the threshold voltage.

To calculate the minimum value of clamping voltage, and thus delay needed to establish this 15 A of current, an expression for the drain-source voltage of M1, V_{d1} is needed. First the gate-source voltage of M1 is given by

$$V_{gs1} = V_s \left[1 - \exp \left(\frac{-t}{R_s(C_{gs1} + 2C_{gd1})} \right) \right] \quad (1)$$

For the IRF510, $C_{gs} + 2C_{gd}$ is approximately C_{in} (≈ 200 pF), $R_s = 10 \Omega$ and $V_s = 20$ V. The time it takes for V_{gs1} to get to V_{th} (4V) is approximately 0.5 ns. At a time 0.5 ns after the source driving voltage has switched on, I_{d1} starts to increase. Assuming $g_{m1} = 2$ S when $V_{gs} = I_D/g_{m1} + V_{th} = 11.5$ V, the current flowing in M1 will be 15 A and the overall time that has passed will be 1.75 ns. At 1.75 ns, V_{d1} should be greater than 16 V. The voltage on the drain of M1 at 1.75 ns is given by (assuming $C_{gs1} \gg C_{gd1}$ and $C_{gs2} \gg C_{ds1} + C_{ds2}$).

$$V_{d1} = V_{clamp} - \frac{1}{C_{gs2} + C_{gd1}} \int_{0.5\text{ ns}}^{1.75\text{ ns}} g_{fs1}(V_{gs1} - V_{th})dt \quad (2)$$

$$= V_{clamp} - 21.2\text{ V} \quad (3)$$

assuming $C_{gs2} + C_{gd1} = 1200$ pF. If $V_{clamp} > 37.2$ V, M2 will turn on when $I_{d1} > 15$ A.

The rate at which current ceases to flow in the load is controlled by the load output capacitance time constant, or $(50 \Omega)(C_{dg2} + C_{ds2})$. The voltage change will be quick enough that the reactance of C_{ds2} and C_{gs2} is small compared with r_{ds1} and r_{ds2} . In this case V_{d1} is given by

$$V_{d1} = \frac{C_{ds2}}{C_{ds2} + C_{gs2}} \cdot 500. \quad (4)$$

5.3 A 1.4 kV Pulse Generator

Figure 6 shows a pulse generator [15] designed around the method given for stacking MOSFETs in section 4.3. The IRF840 has $C_{iss} = 1300$ pF and $C_{rss} = 50$ pF.

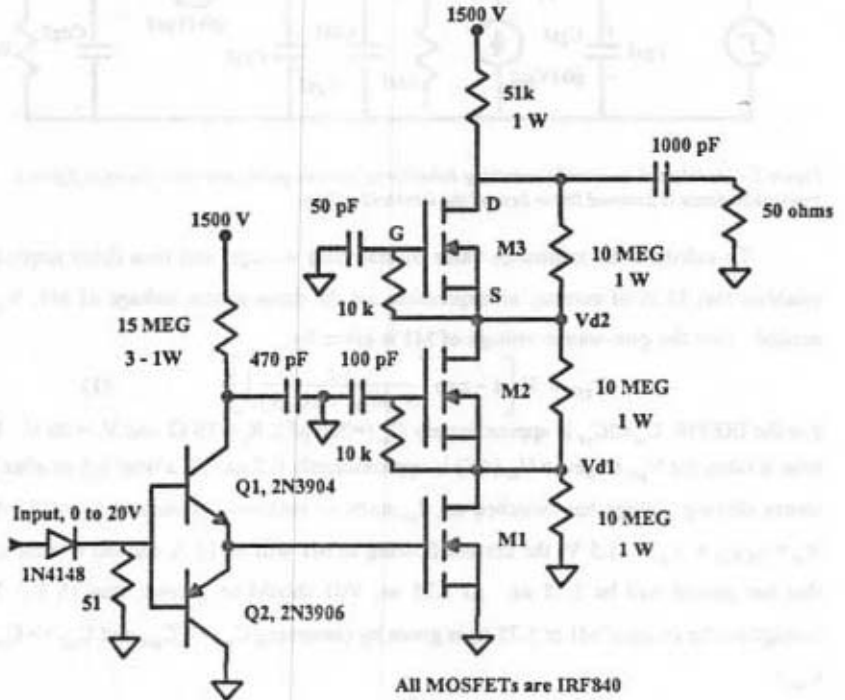


Figure 6 - Pulse generator using stacked MOSFETs. Q1 is operated as an avalanche transistor and charges the input capacitance of M1 very quickly.

Since the drain-source voltage of each MOSFET will change by 500 V while at the same time the gate-source voltage must not exceed 20 V, the voltage gain, A_v , is approximately 25. The equivalent gate-source capacitance of M1, M2 or M3 is 2500 pF (1300 pF + 25×50 pF). For amplifier or ramp design where swing linearity is important,

10 V is a better choice for the maximum V_{gs} . For V_{gs} larger than 10 V, the MOSFET will approach the ohmic region causing distortion.

Transistor Q1 is operated as an avalanche transistor [7] with breakdown voltage of 120 V. When Q1 is triggered by the input signal, 0 to 20 V, it dumps the charge on the 470 pF capacitor into the input capacitance of M1. Assuming the input of M1 is capacitive, a capacitive voltage divider exists between the 470 pF avalanche transistor capacitor and the 2500 pF input capacitance of M1. This voltage division limits the applied gate drive to 20 V. Adding the effects of the lead inductance can cause the gate potential to rise above 20 V. The driver compensates for the voltage induced by the lead inductance by increasing the voltage applied to the gate of M1. When the gate potential rises above 20 V after a delay long enough to charge M1's input capacitance, Q2 turns on and pulls the gate back to 20 V. Since the capacitive divider between the 470 pF capacitor and the input capacitance of M1 should limit the drive to less than 20 V, Q2 is added only for additional protection.

The gate capacitors of M2 and M3 are 100 pF and 50 pF or $\frac{1}{25}$ 2500 pF and $\frac{1}{50}$ 2500 pF. The output of this pulse generator is shown in figure 7. The amplitude is 1400 V with a risetime of approximately 2 ns. There was no noticeable jitter. Several of these circuits were built with no MOSFET failures. The switching time of a single device was 2 ns, approximately the same as the stack.

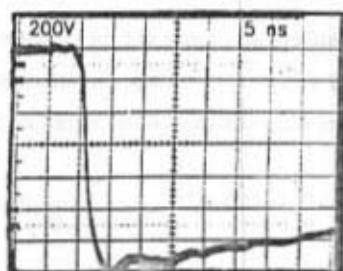


Figure 7 - Output of pulser shown in figure 6. 200 V/div and 5 ns/div.

Another concern when stacking MOSFETs is maintaining the manufacturers specification on peak pulsed current. When selecting a power MOSFET, the peak

current needed will determine the type of MOSFET used while the peak voltage needed will determine the number of devices. In the example given above, three IRF840s, with 500 V and 32 A ratings provide the maximum number that may be used for a 50 ohm load.

5.4 A Marx Bank of Power MOSFETs

Figure 8 shows the basic schematic of a power MOSFET Marx bank [17]. The number of MOSFETs used will determine the output voltage across the load. Ideally if three MOSFETs are used then the output amplitude is $3 \times (V_{dd})$, where V_{dd} is the supply voltage. The transistor Q1 is operated as an avalanche transistor. When Q1 is triggered, it rapidly charges the input capacitance of M1 causing the drain potential of M1 to change from V_{dd} to zero. This in turn causes the source potential of M2 to change from zero to $-V_{dd}$. The source potential of M3 changes from zero to $-2V_{dd}$ and so on down the line. The main concern during switching is keeping the potential difference between the gate and source of each MOSFET below 20 V. If the gate-source potential increases above 20 V, puncturing of the SiO_2 interface may occur leading to MOSFET failure. Since the resistances R_g and R_s are large compared to the capacitive reactances present in the circuit they will be ignored in the following analysis.

The effective gate-source capacitance of any MOSFET in Figure 8 is given by,

$$C_{gseff} = C_{gs} + \frac{dV_d}{dV_g} \cdot C_{gd}, \quad (5)$$

where the second term is the Miller capacitance and the effects of C_{db} have been ignored. For MOSFET M2 in figure 8 a capacitive voltage divider exists between C_{gseff} and C2 during switching. The value of C2 is determined by (assuming 20 V maximum between the gate and source),

$$\Delta V_{gs} = 20 = \Delta V_{d2} \cdot \frac{C_2}{C_2 + C_{gseff}} \quad \text{and,}$$

$$C_2 = \frac{20 \cdot C_{gseff}}{\Delta V_{d2} - 20}, \quad (6),$$

$$C_N \cong \frac{1}{N-1} C_2 \quad \text{for } N > 2, \quad (7).$$

Using equations (5)-(7) a Marx bank circuit can be designed using power MOSFETs.

Resistors R_d , R_g and R_s are used to provide a dc path for biasing. These resistors bias the drain of each MOSFET at V_{dd} and the gate and source at approximately 0 V. The values of R_s , R_g and R_d are typically in the range of several tens of thousands ohms. The two factors which must be considered when selecting these resistances are the leakage current through the devices and the amount of current lost through these resistors during switching. The coupling capacitors C_c must be large compared to the capacitance at each source node to ground (the effective gate-source capacitance in series with the gate capacitor to ground), in order for C_c to have little effect on switching behavior.

5.4.1 An Example of a Marx bank of Power MOSFETs

Using the procedure given above a Marx bank pulse generator will now be designed. Five IRF740 power MOSFETs are used with a voltage supply of 420 V. The IRF740 is rated at 400 V breakdown and 40 A peak pulsed current. The gate-source capacitance is 1300 pF and the drain-gate capacitance is 37 pF. Since the drain-source potential will change by 400V and the gate-source potential will change by 20 V, $\frac{dV_d}{dV_g} = 20$. Using (5) the effective gate source capacitance is $1300 + 20 \cdot 37 \cong 2000$ pF. Using (6) and (7) the gate capacitors are, $C_2 = 100$ pF, $C_3 = 50$ pF, $C_4 = 33$ pF and $C_5 = 25$ pF. The biasing resistors are selected as $R_d = 510$ k and $R_g = R_s = 51$ k. The coupling capacitor $C_c = 4700$ pF. The avalanche transistor Q1 breaks down at 120 V so the capacitance C_1 is 470 pF. This value is determined by treating the avalanche transistor as a perfect switch and using a capacitive voltage divider between C_1 and the input capacitance of M1 (2000 pF). The output of this pulse generator is shown in Figure 9. The amplitude out is -1,800 V (36 A) and the fall time was approximately 3 ns. Pulse jitter was negligible.

Ideally a 2000 V pulse would be generated in the design above. The on resistance of each MOSFET is approximately one ohm, at a drain current of 30 A. As the drain current is increased further, the on resistance increases exponentially. This resistance lowers the output amplitude to a value less than the ideal output amplitude. In this example a 50 Ω load was driven, however the techniques presented here can be

applied to any type of load. The designer must determine the peak current and the peak voltage the circuit must supply to the load. The peak current will determine the type of power MOSFET used while the peak voltage will determine how many devices are needed.

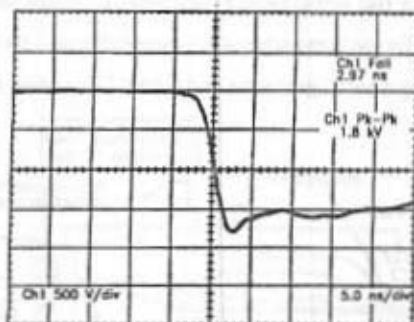


Figure 9 - Output of power MOSFET Marx bank. 500 V/div and 5 ns/div.

5.5 Streak Camera Ramp Circuit

The streak camera is an instrument used for measuring optical signals with time resolutions down to less than 1 ps [19]. The streak camera is composed of the streak tube, sweep electronics, microchannel plate image intensifier and a camera for reading the streaks (figure 10). Input light strikes the photocathode and generates electrons. These electrons are accelerated towards the anode of the streak tube very quickly. The electron beam passes between the deflection plates and strikes the phosphor screen. Since the phosphor will stay illuminated for a time period which is long compared to the time the signal is present, a slow CCD camera or Polaroid film can be used to capture the signal.

The time history of the signal is obtained by knowing the sweep time, i.e., the time it takes the electron beam to traverse from the top of the phosphor screen to the bottom as shown in figure 10. Often a comb generator is used as a time reference to measure sweep linearity and time. The comb generator produces a signal which is a

series of impulses (or rectangular pulses for slower sweeps) separated by a known time. The signal looks like a comb and thus the reason for the name.

The amplitude, or intensity, information is obtained by the brightness of the streak. For example, consider a step function, $u(t)$, applied to the streak camera input when the sweep has traveled half way down the phosphor screen. We will record a streak which is black (no signal exists) until midway across the phosphor and then some constant light level for the remainder of the sweep (figure 11(a)). Figure 11(b) shows the streak obtained using a comb generator and figure 11(c) using a ramp.

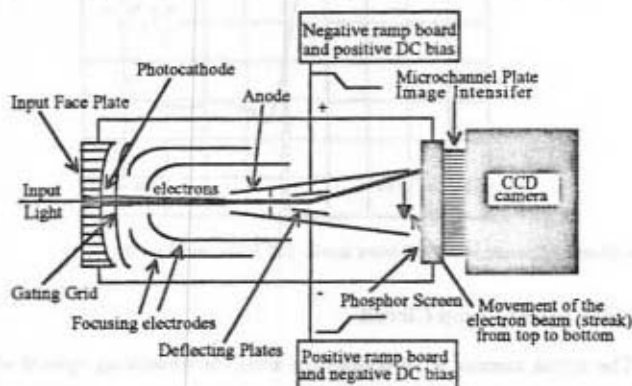


Figure 10 - Diagram of the streak camera.

Another useful feature of the streak camera is the large number of independent data channels that can be recorded. For a streak tube with a 40 mm diameter over 100 channels of data can be recorded. This coupled with the large bandwidths available will make the streak camera useful for measuring simultaneous signals with large bandwidths. For example, a real time electrical oscilloscope with a bandwidth greater than 50 GHz could be built using a Mach-Zender interferometer or non-invasive probing of ICs could be performed utilizing the Pockel's effect.

This section is concerned with the sweep electronics (ramp board) portion of the streak camera. The deflection plates, shown in figure 10 look like a capacitor of value 10 pF (typically). Full deflection, i.e., the voltage required to move the electron beam from

the top of the tube to the bottom, requires approximately 1.5 kV. Initially the electron beam is positioned off the screen, at the top by the applied dc sweep plate voltages. After the sweep is completed the electron beam should be positioned off the screen at the bottom of the tube and held there for a certain time. This means that the ramp voltage must be larger than the 1.5 kV required for full deflection.

To date these high voltage nanosecond ramps have been generated using avalanche transistor strings [20]. Avalanche transistors strings are nonlinear and are difficult to design with due to reproducibility, reliability and stability problems. External pulse shaping must be used because of the nonlinearity of the avalanche circuits. This increases the size and complexity of the sweep circuit and limits the range and number of different sweep times.

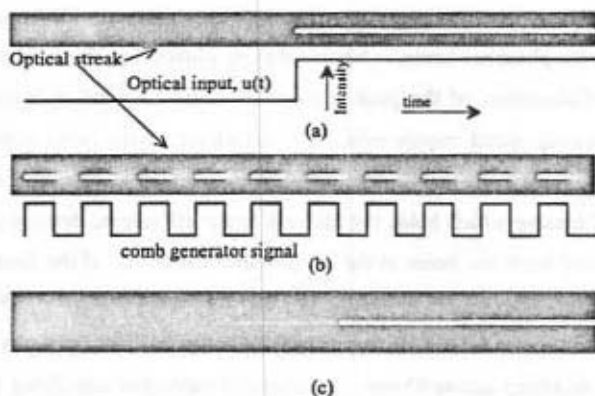


Figure 11 - (a) Shows the optical streak which would be recorded if the step input signal shown is applied, (b) optical streak resulting from the comb generator signal and (c) the streak resulting from an input ramp. The dark area signifies the portion of the phosphor surrounding the streak while the light areas signify light emission resulting from the input signal.

The design presented in the remainder of this section uses power MOSFETs which are operated linearly. A constant current is generated and applied to the deflection capacitance. This produces a linear ramping voltage between the deflection plates. The ramp rate is controlled by changing the magnitude of the current source which is

controlled by the gate source voltage. Series operation of power MOSFETs [15], section 4.3, is used to generate the ± 2 kV ramps needed.

5.5.1 Design Considerations

The 10 pF capacitance of the deflection plates is driven with a constant current. The positive ramp board sources current while the negative ramp board sinks current. In this way two ramps of equal and opposite polarity can be generated.

Consider the simpler design with one of the deflection plates tied to ground and the other being modulated with a ramp. The electric field in the vertical direction, does not change relative to the two ramp case. However, the average potential (sum of the plate potentials divided by 2) between the plates does change. For the case of two ramps the average potential remains constant for any given time. When one ramp is used the average potential is not constant. This causes problems with focusing, i.e., the streak seen on the phosphor becomes blurred thereby eliminating this mode as an option.

Calculation of the peak amount of current needed is accomplished using the fastest sweep speed requirement. The amplitude of the ramp voltage is picked to be 2,000 V. This gives an effective 4,000 V ramp which is more than enough to overcome the DC biasing which holds the electron beam off screen, deflects the beam across the screen and holds the beam at the bottom after the event. If the fastest sweep speed is 5 ns, then the peak current is $10 \text{ pF} \frac{4000 \text{ V}}{5 \times 10^{-9} \text{ s}}$ or 8 A. Since only a portion of the ramp will be used (1.5 kV) the MOSFET current will be lower than this, typically in the range of 3 A for a 5 ns sweep across 40 mm. An alternate method of specifying the sweep rate is the time per mm of phosphor length. A 5 ns sweep across 40 mm corresponds to 125 ps/mm. This is helpful when comparing relative sweep times of streak cameras.

5.5.2 Circuit Design

Since two different ramp boards are needed, it is desirable to have identical circuit designs for each board with one board using positive supply voltages and n-channel devices and the other board using p-channel devices with negative supply voltages. This means we must use complementary high voltage MOSFETs.

The MOSFETs used in this design are the VN0345N2 n-channel and the VP0345N2 p-channel. A simplified schematic of the ramp circuits is shown in figure 12. The bottom MOSFET in the stack controls the current through the other MOSFETs.

If a constant gate source potential is applied between the gate and source of M1 then the drain current is $g_m(V_{gs} - V_{th})$, providing the MOSFET stays in the saturation region. It is desirable to force all MOSFETs to turn on at the same rate to maximize overall linearity. If one of the MOSFETs turns on faster than the others the ramp will have a discontinuity appearing as a change in slope.

The MOSFET gate-drain capacitance is 20 pF and the gate-source capacitance is 550 pF. Following the method given in [15] the gate capacitors are; $C_2 = 30$ pF, $C_3 = 15$ pF, $C_4 = 10$ pF, $C_5 = 8.2$ pF and $C_6 = 5.6$ pF. These capacitors form a capacitive voltage divider with the effective gate-source capacitance of each MOSFET. Their values are picked so that the maximum voltage across the gate-source junction is 10 volts.

Connecting the board to the deflection structure is accomplished using a wire. This jumper and the internal sweep plate connection are inductive. The resistor r_4 is used to lower the Q of the series LC formed by the deflection capacitance and the interconnecting inductance. The value is picked so that the $2.2RC$ risetime associated with the resistor deflection capacitance alone is small compared to the sweep time. In this case 150 ohms is used. This gives a risetime of 3.3 ns for the overall risetime. Faster sweeps can be achieved if this resistor is removed and M1 is driven with a 20 V step. The limiting speed factor is the interconnecting inductance and the deflection capacitance.

The goal in this design was to replace the existing avalanche boards in the EG&G streak cameras. The existing avalanche boards were settable to 5, 10, and 15 ns sweep speeds by replacing a wave shaping module (low pass filter). Unless the camera was taken apart and the waveshaping module replaced, the camera was limited to one sweep speed. This makes it difficult to time complex systems. The new design allows the sweep speed to be changed from 5 to 300 ns with a front panel knob (similar to an oscilloscope time base).

Once the two circuit boards are in place they must be aligned. The delay between the ramps is adjusted as well as the slopes of the ramps. This is accomplished using two high voltage oscilloscope probes (loading of approximately 1 pF each). External delay is added or removed while comparing the mid points on the ramps. The ramps are adjusted to have the same slope. One problem that exists is that although the slew rate of the ramps can be adjusted with the oscilloscope, the actual sweep time must be measured using the streak camera. This is caused by the DC voltages used for biasing the beam off of the screen, i.e., we do not know exactly when the beam will enter the phosphor screen.

The knob controls the DC voltage source V_g which in turn, controls the ramp rate. The source is simply a DC source and a MOSFET switch. When the streak camera is triggered, the DC voltage is applied to the gate of M1.

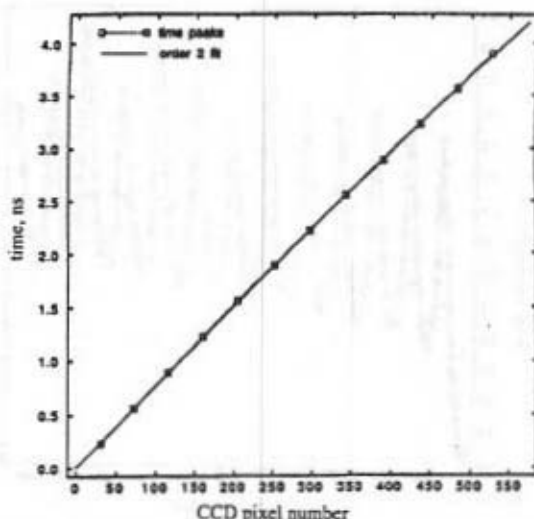


Figure 13 - Shows sweep speed of approximately 4 ns.

The most important attribute of the ramps is linearity. Nonlinearities cause errors in amplitude as well as temporal information. Consider the streak shown in figure 11(c).

Any nonlinearity in the ramp will cause the streak to become brighter in one place and darker in another affecting both the amplitude and time responses. Figure 13 shows the resulting ramps for the fastest sweep rate. The sweep time is approximately 4 ns and the linearity is better than 2%. This sweep time was limited by the speed of the p-channel board. The n-channel board could generate ramps at least two times faster than the p-channel MOSFET board.

The linearity data shown in figure 13 was determined using the 3 GHz comb shown in figure 14. The comb is used to determine the actual sweep speed. If the ramps are perfectly linear the time difference between adjacent peaks in figure 14 will be equal. The differences in the times is used to determine the nonlinearity.

For the 4 ns sweep shown above the MOSFETs are well within the saturation region. As the sweep time is reduced by decreasing the current, the MOSFETs approach

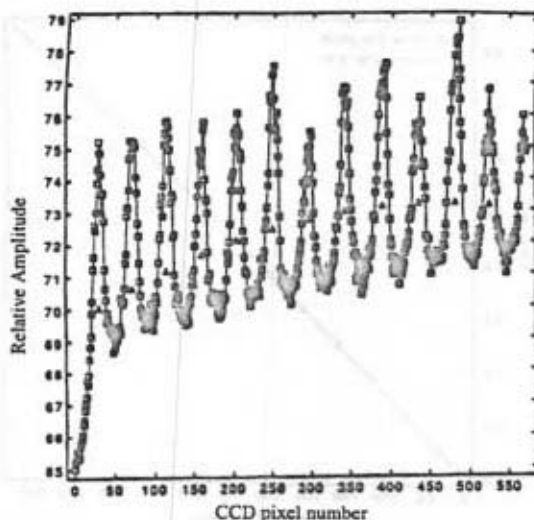


Figure 14 - Shows the shape of the 3 GHz comb used for calculating the sweep time.

the cutoff region. When this occurs the drain current no longer follows the relationship $g_m(V_g - V_a)$ but becomes nonlinear. This causes nonlinearities in the sweep. Figure 15 shows this effect. The sweep here is approximately 160 ns. The linearity is 5 %. As the sweep is lengthened to 300 ns the nonlinearity increases to 10%.

One solution to this problem is to place a capacitor in parallel with the deflection capacitance as the sweeps are lengthened. This can be accomplished with a relay or switch that detects when the capacitor is needed. For the applications required here the longer sweeps were mainly used as a course setting to determine where the signal is in time. The linearity of the fast sweeps is the most important parameter for good data in these measurements.

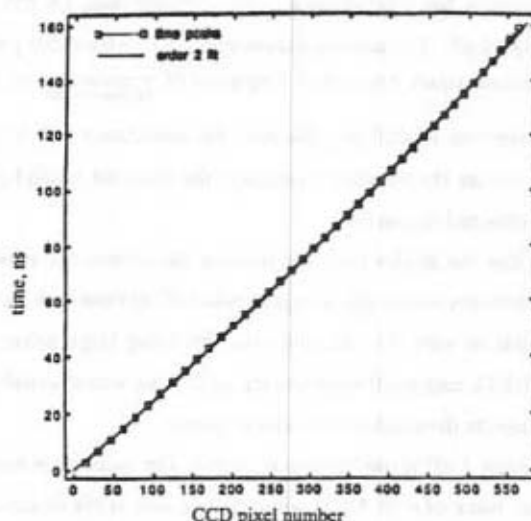


Figure 15 - A longer sweep showing the effect of coming close to the cutoff region.

Although the design presented here is a significant improvement over the previously used methods, there is still need for improvement. It is desirable to have a faster sweep time, for example 1 ns. This could be accomplished using the "brute force" method by increasing the amplitude of the ramps. However, as the amplitude increases

beyond 3 kV, components become more difficult to find, more inductive, and more safety precautions must be taken.

Future work will involve designs for faster ramps, eliminating the difference in time delay between ramps and having automatic slope adjustment between the p and n channel MOSFET boards. The ultimate design goal is to attain a sweep circuit variable from 1 ns (25 ps/mm) to 300 ns with very little alignment required.

5.6 A 500 ps, 1.5 kV Pulse Generator

As another example consider a NLTL which takes a 1.5 kV, 2 ns risetime pulse and generates a 1.5 kV, 500 ps risetime output pulse. The immediate requirement on the diodes is that they have a breakdown voltage greater than 1.5 kV. The 1N4007 diode chosen for this example has a breakdown voltage greater than 1.6 kV. The C_p of the 1N4007 is typically 13 pF. The series inductance internal to the diode package is 2.5 nH. The diode will become series resonant at frequency of $\frac{1}{2\pi\sqrt{2.5\text{nH}\cdot 13\text{pF}}}$ or 883 MHz. This corresponds to a risetime of 400 ps. Because the inductance will begin to offset the diode capacitance before the resonant frequency, the resonant limited risetime is lower than what will be obtained in practice.

To ensure that the diodes limit the risetime rather than the periodic structure, a small inductance between stages and a large number of sections were selected. It would be more economical to vary the inductor value by using large value inductors at the beginning of the NLTL and small values at the end. This would avoid the Bragg cutoff frequency and minimize the number of diodes required.

For this design 3 nH is used between stages. The inductor is constructed using a one-half centimeter piece of # 20 AWG wire. The anodes of the diodes are soldered to a copper ground plane while the cathode is elevated to reduce stray capacitance. The Bragg frequency of this structure is $\frac{1}{\pi\sqrt{3\text{nH}\cdot 13\text{pF}}}$ or 1.6 GHz which corresponds to a risetime of 217 ps, a factor of two below the diode resonant risetime. Assuming $\phi = 1$ the capacitance of the diodes is $C_{d10} = \frac{13\text{pF}}{\sqrt{150}} = 1.06\text{ pF}$ and $C_{d90} = \frac{13\text{pF}}{\sqrt{1350}} = 0.35\text{ pF}$. This corresponds to a DRPS of $\sqrt{3\text{nH}\cdot 1.06\text{pF}} - \sqrt{3\text{nH}\cdot 0.35\text{pF}} = 24\text{ ps}$. Because of stray capacitance per section of approximately 0.2 pF the actual DRPS is approximately 20 ps.

Figure 16 shows the input pulse (trace A) and the output pulses (traces B and C) using 50 sections and 100 sections respectively. The risetime of the measuring system was 850 ps, determined using a 25 ps risetime pulse generated with a tunnel diode. Trace B for 50 sections shows a measured risetime of 1.26 ns. The actual risetime of trace B is $\sqrt{(1.26\text{ ns})^2 + (0.85\text{ ns})^2} = 930\text{ ps}$. This corresponds very closely to the estimated risetime, namely, $(1.9\text{ ns} - 50 \times 20\text{ ps})$ or 900 ps. When 50 more sections are added, the diode limited risetime is encountered with a measured risetime of 500 ps. Adding additional sections did not decrease the risetime confirming that the diodes are indeed the limiting factor.

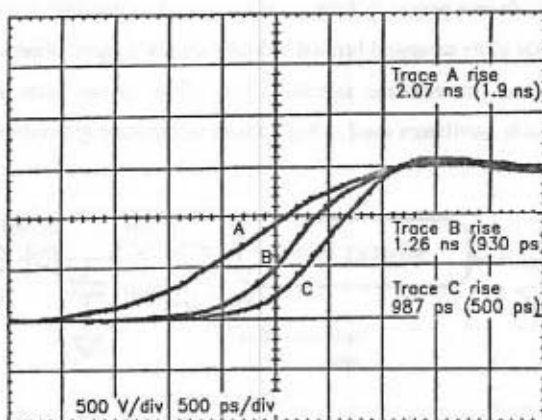


Figure 16 - Trace A is the input to the NLTL and has a risetime, after removing the scope risetime, of 1.9 ns. The risetimes of traces B and C are 930 ps and 500 ps respectively. Trace B corresponds to 50 diodes while trace C corresponds to 100 diodes. The vertical scale corresponds to 500 V/div while the horizontal scale is 500 ps/div.

The diode breakdown voltage and series inductance are the limiting factors in achieving higher amplitude and faster risetime pulses. The breakdown voltage of the diodes can be increased by using glass passivation.

If the diodes cannot be removed from their package then risetime performance is limited by the series inductance. A simple, but effective method to increase both the diode series resonant frequency and the Bragg cutoff frequency is to apply a small

positive dc voltage to the line. For example, if 15 V is applied to the line, the initial capacitance of each diode will decrease by a factor of 4 increasing the resonant limited frequencies by two (causing the resonant limited risetime in the example presented to become 200 ps). The cost for this improvement is a small decrease in the DRPS.

5.7 Picosecond Pulse Generation Using Avalanche Diodes

Avalanche diodes have been shown to be useful for the generation of pulses with risetimes in the 100 ps regime [26-28]. Using power MOSFETs to drive avalanche diodes can produce very good results. Consider the schematic shown in figure 17. If a large current, greater than the threshold current for plasma formation, can be forced through the diode in a period of time short compared to the time it takes a carrier to drift across the diode at its saturated limited velocity then a trapped plasma can be formed and used to generate fast risetime signals. This effect is the same as that found in TRAPATT diode oscillators used in high power microwave generation.

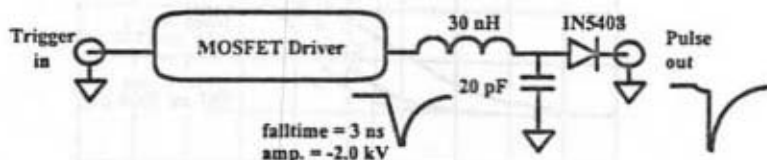


Figure 17 - Simplified schematic of MOSFET pulser driving Avalanche diode.

The purpose of the 20 pF capacitor is to store charge for use when the diode begins to conduct. This charge is available to supply the load with the needed current during switching. The 30 nH inductor has two functions. First, it isolates the driver from the fast edge when switching takes place. Second, it matches the diode and 20 pF capacitor to the MOSFET driver. The diode used here is the 1N5408. The breakdown voltage of this particular diode was 1400 V. The breakdown is sharp, in other words there is a sharp transition from nonconducting to conducting when the IV characteristics

are displayed on the curve tracer. Another important attribute of the diode is its capacitance. A fairly large zero bias junction capacitance must be present, on the order of 100 pF, in order to establish the large diffusion threshold current discussed above. This also puts an upper limit on the load impedance that can be used. Using a large load impedance will lower the diffusion current flowing through the diode capacitance keeping the diode current from reaching threshold before the diode breaks down. The load driven by the circuit shown in figure 17 was 50 ohms.

The MOSFET driver is a Marx bank of power MOSFETs. The driver produced a 2,000 V pulse into 50 ohms with a risetime of 3 ns. The output of the pulse sharpener is shown in figure 18. The risetime is 129 ps with an amplitude of 2.4 kV. The output amplitude is higher than the input amplitude due to the inductive peaking present. Pulse jitter was less than 10 ps.

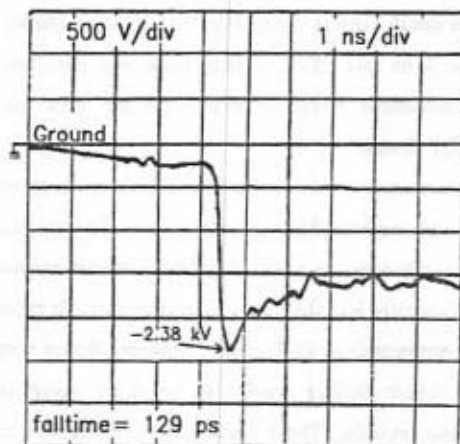


Figure 18 - Output of pulse generator shown in figure 17. The peak amplitude is 2.38 kV with a leading edge transition duration of 129 ps.

Chapter 6 - Conclusion

This dissertation has discussed the basic design techniques and uses of power MOSFETs in instrumentation. It is shown that the power MOSFET will play a major role in high speed electronic and electrooptic instrument design. The innovative contributions of this work include (1) developing MOSFET driver circuits to allow operation with risetimes less than 5 ns, (2) developing series operation of power MOSFETs for high voltage applications (3) applying the series operation to other circuit configurations such as the cascode and the Marx bank circuits, (4) applying the design methods to streak camera instrumentation and (5) demonstrating picosecond pulse generation using nonlinear transmission lines and avalanche diodes.

Because of the inherent speed of optics, electrical instruments which work with or are a part of an optical instrument will be needed more often in the future. The example given in chapter 5 of a streak camera ramp circuit is a good example. Here a ramp with a variable rate down to 5 ns and 2,000 V amplitude was designed. Previous designs employing tubes or avalanche transistor strings do not give the same performance features as the MOSFET design.

Gating of microchannel plate image intensifiers for high speed photography is another area where the power MOSFET is finding uses. To gate this electron multiplier/high speed shutter typically requires a 400 V pulse. The risetime and falltime should be as quick as possible, generally less than 3 ns, and have variable pulse widths down to 10 ns. The pulse width corresponds to the length of time the shutter is open.

Another area where further work can be done using power MOSFETs is modulating electro-optic crystals. The Pockel's effect or Pockel's cell typically requires several thousand volts to modulate. Gating a Pockel's cell on with widths below 5 ns is often desirable. Series operation of power MOSFETs should be able to achieve this performance goal. Other areas where the design techniques presented here would apply are in pulsed power, radar and semiconductor testing. Drivers for high power tubes such as the thyratron are needed. Low jitter and the ability to source large amounts of current in the nanosecond time regime into a capacitive load are desirable.

Generating high power pulses such as those used in impulse radar is another area where power MOSFETs will find use. The duration of the pulse is directly related to the resolving capabilities of the impulse radar system. Using the methods presented in this dissertation 100 kW, 100 ps pulses can be generated and used as an impulse radar source.

One last area where the power MOSFET will find use is in basic research instruments for science. In particular, the modulating of particle beams or modulating electron or ion beams is important in many areas of science.

In conclusion, the basic concerns and techniques needed to design instrumentation with power MOSFETs has been presented. The experimental work presented represents new applications for the power MOSFET. Future work and applications have been discussed showing there is a significant area where this work can be applied.

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