# CMOS transconductor VCO with adjustable operating and centre frequencies

B. Keeth, R.J. Baker and H.W. Li

*Indexing terms: CMOS integrated circuits, Voltage controlled oscillators*

A novel monolithic VCO using a transconductance architecture and with adjustable operating and centre frequencies is presented. Oscillating frequencies from < 1Hz to > 50MHz were attained with external capacitors. Power dissipation from a 5V supply was 150mW driving a 20pF load. The die size was 400 × 1500μm² and was fabricated using a 2μm *n*-well double-metal CMOS process.

*Introduction:* Voltage controlled oscillators are used in a wide array of communication and signal processing applications. VCOs with a large span of operating frequencies allow the flexibility of using one VCO in many types of circuits. As mixed-signal systems increase in popularity, more complex analogue circuitry must be designed in standard digital CMOS processes. VCOs fabricated in CMOS have typically been composed of current-starved ring oscillators [1, 2], which have limited control over the operating and centre frequencies. The VCO presented in this Letter overcomes these limitations through the implementation of a current-steering transconductance amplifier and a current-to-frequency oscillator.

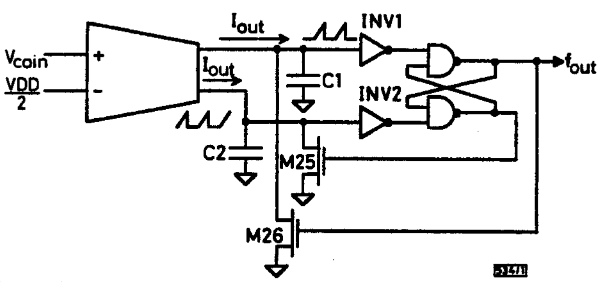


**Fig. 1** *Block diagram of CMOS transconductor VCO*

*Transconductor approach:* The block diagram of the VCO is shown in Fig. 1. $V_{coin}$, the VCO control voltage, is used in part to generate the current $I_{out}$. Two transconductor outputs alternately charge capacitors, C1 and C2. Positive feedback provided from the logic gates ensures that these capacitors are not charged simultaneously.

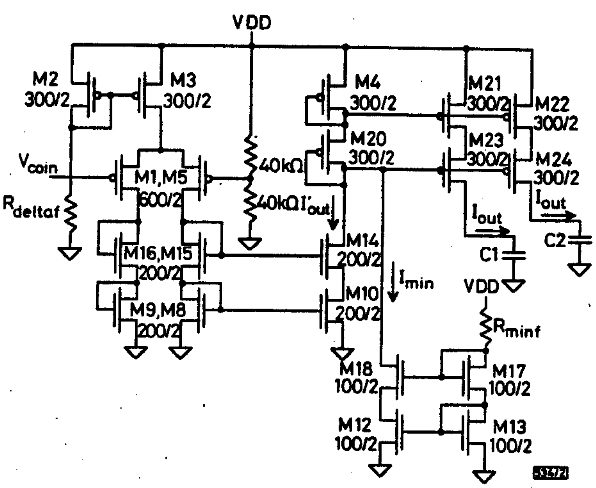


**Fig. 2** *Schematic diagram of transconductor portion of VCO*

The schematic diagram of the transconductor VCO is shown in Fig. 2. MOSFETs M2 and M3 form a current mirror which, when used with external resistor $R_{deltaf}$, sets the range of operating frequencies. Current from M3 is steered through M1 and M5. The gate of MS is set to *VDD*/2. When the controlling voltage on the gate of M1 is *VDD*/2, the current through M3 splits evenly through M1 and M5. M15 and M8 are used to sense $I_{D5}$ and set the current in M14 and M10. Device sizes were chosen so that $I_{D14} = I_{D5}$.

The current mirror consisting of M12, M13, M18, M17 and $R_{minf}$ set the minimum current out of the transconductor stage. During linear operation, $I_{out} = I'_{out} + I_{min}$. Therefore, when $V_{coin} = 0$, $I_{D18}$ ensures that a minimum current flows out of the transconductor stage and sets the minimum operating frequency.

Inverters INV1 and INV2, were designed to have a switching threshold of 1.6 V. The oscillating frequency is given by

$$frequency = \frac{1}{2\left(\frac{1.6C_1}{I_{out}} + t_d\right)}$$

where $t_d$ is the total delay through the logic gates, typically 3.3ns. The range of oscillating frequencies is given by

$$\Delta f = \frac{1}{2\left(\frac{1.6C_1}{I_{min}+I_{out}} + 3.3ns\right)} - \frac{1}{2\left(\frac{1.6C_1}{I_{min}} + 3.3ns\right)}$$

where $I_{min} = I_{D18}$.

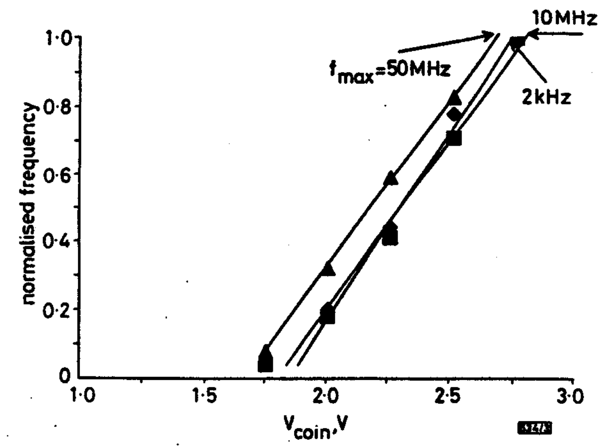


**Fig. 3** *Normalised frequency against VCO input voltage for different values of C1 and C2*

▲ $C_1 = C_2 = 0$
◆ $C_1 = C_2 = 33pF$
■ $C_1 = C_2 = 0.22\mu F$

*Experimental results:* The VCO was fabricated in a 2μm double-metal, *n*-well process and measured 400μm by 1500μm (which included output buffers). Experimental results were taken using $R_{deltaf} = 2k\Omega$ and $R_{minf} = 100k\Omega$. With these values $I_{out}$ can swing from ~70μA to 1.5mA. The normalised frequency against the control voltage is shown in Fig. 3 for three different values of the capacitors. When $C1 = C2 = 0$ the internal depletion capacitances, oxide capacitances, bonding pad capacitance and packaging capacitance (including test fixture) give ~5pF total stray capacitance. The result is a maximum oscillating frequency of 56.5MHz (Fig. 4) adjustable down to 22.6kHz or more than three decades of range. The maximum oscillating frequency was 11.5MHz adjustable to 2.4kHz, and 2.6kHz adjustable to 0.4Hz with $C_1$ = 33pF and $C_1$ = 0.22μF, respectively. This operating frequency range can be made smaller or larger with suitable choices of $R_{minf}$ and $R_{deltaf}$.

*Conclusion:* A transconductor voltage controlled oscillator has been presented. Variable frequency range and centre frequency were obtained by using a voltage-to-current converter and a current controlled oscillator. Experimental results confirmed the versatility of the design compared to a CMOS current-starved VCO.


31 May 1995
*Electronics Letters Online No: 199501001*

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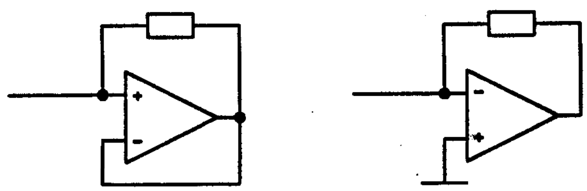
## Comment

## GB-R impedances: New approach to impedance simulation

M. van de Gevel

*Indexing terms: Capacitors, Impedance converters, Inductors, Operational amplifiers*

In [1], Serrano and Carlosena prove that the input impedances of the circuits in Fig. 1*a* and *b* of [1] are independent of $C_A$ and $R_B$, as long as $C_A R_B << 1/GB$. However, this requirement can be fulfilled by making $C_A$ and $R_B$ equal to zero. In this case, two out of three passive components in Fig. 1*a* of [1] and four out of five passive components in Fig. 1*b* of [1] can be eliminated. The opamp on the left hand side of Fig. 1*b* of [1] also becomes redundant, so that the remaining circuit becomes equivalent to that described in [2] (see Fig. 1). Without redundant components, Fig. 1*a* is a simpler implementation of the *R*-active circuit described in Table 2*d* of [3]. Compared with the circuit in [3], Fig. 1*a* (with or without $C_A$ and $R_B$) has the advantage of having no floating nodes in the circuit, which gives it a better chance of working in practice.



a b

**Fig. 1** *Simplified capacitance and inductance simulating circuits*

*a* Capacitance simulating
*b* Inductance simulating

 *24 May 1995*

*Electronics Letters Online No: 19950956*

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## Reply

## GB-R impedances: New approach to impedance simulation

L. Serrano and A. Carlosena

We thank M. van de Gevel for the comment [1], which gives further insight into the circuits we proposed in [2].

We substantially agree with the comment on [2], in the sense that the two circuits proposed are equivalent to, and much simpler than, our circuits for limited $C_A$ and $R_B$ values. We propose design conditions such that $R_B C_A << 1$, and in the particular case $R_B = 0$ and $C_A = 0$, our circuits in Fig. 1*a* and *b* of [2] become the R-Active impedances of Fig. 1*a* and *b* of [1]. However, retaining $R_B$ and $C_A$ in the designs has several advantages:

(i) From a theoretical perspective, R-active impedances (and in general R-active circuits) can be seen as limiting cases of RC active impedances (circuits). GB-R impedances can be regarded as the transition between both cases.

(ii) The impedance range can be extended. In the example of the capacitor, it can take both possitive and negative values, depending on the value of $R_B C_A$, as shown in Fig. 1. For values < 0.1/GB, say, the capacitance value is quite independent of the time constant (and controllable with $R_1$), whereas for larger time constant values $R_1$; $R_B$ and $C_A$ can be used to define the capacitance. Similar arguments can be given for simulated inductances, with only positive values.

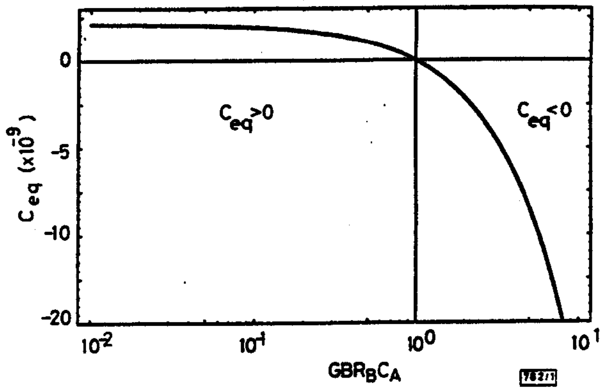


**Fig. 1** *Capacitor value for $R_1$ constant and $R_B C_A$ variable*

(iii) Even for the intermediate $R_B C_A$ region, with a similar capacitance value to that of the R-active impedances, the use of $R_B$ and $C_A$ provides a slightly better frequency response. In the capacitor example, when $GB.R_B C_A = 1/2$, an inherent phase compensation is achieved, for the capacitance value $C_{eq} = 1/(2GB.R_1)$

(iv) In a circuit such as the inductor example of Fig. 1*b* in [2], which uses two opamps, the first opamp can be used for buffering in the case of ladder (simulated) passive filters [3].

 *20 June 1995*

*Electronics Letters Online No: 19950957*

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## Macromodel of CMOS operational amplifier including supply current variation

C. Chalk and M. Zwolinski

*Indexing terms: Analogue circuits, Testing, Operational amplifiers, SPICE*

A SPICE macromodel of a CMOS operational amplifier is described in which the supply current is modelled. This macromodel is suited to multilevel analogue fault simulation. The accuracy of the macromodel is demonstrated by comparison with the full transistor level model. A >3 times increase in simulation speed compared with the full model is possible.