levels, the large change in the carrier density results in both large linear as well as large nonlinear chirp. If an appropriate fibre (i.e. with proper length and dispersion) is used to fully compensate for this large linear chirp, a relatively shorter compressed pulse will be realised (at 1·5 mA, optimal compression was achieved when eqn. 1 was satisfied). Because the fibre compression is a linear technique and it compensates only for the linear chirp, the deviation from the transform limit at low bias levels is mainly due to the uncompensated nonlinear chirp, which is of a significant amount. As the bias level is increased, both Δt and $\Delta\lambda$ of the original pulse decrease, and the different rates of decrease make the ratio $\Delta t/\Delta\lambda$ deviate slightly from the optimal compression condition. This leads to an overcompensation of the linear chirp causing broadening of the pulse. However, because of the smaller change in the carrier density at high bias levels, the proportion of the linear chirp in the narrowed chirped spectrum is enhanced compared to that at lower bias levels. Therefore, at higher bias levels, even though the pulse width is slightly wider due to the overcompensation of the linear chirp, the time bandwidth product drops as a result of the significant reduction of the nonlinear chirp. Hence, to achieve the shortest pulse, biasing the laser far below its threshold is recommended. However, at slightly higher bias levels, but still well below threshold, lower time bandwidth products can be achieved. With an increase in the bias current level, there is also a rise in the optical power level which could be advantageous if these pulses are to be used as soliton sources. The average power measured at a bias level of 1·5 mA (bias level that gives shortest pulses) was around 43 μW which corresponded to a peak power of 120 mW. Whereas at a higher bias level of 4 mA the peak power increases to around 200 mW. We also observed the effect of RF current on the pulse width by slightly varying the RF drive around 27 dBm. However, the change in pulse width was not as sensitive to RF current as that to the DC current.

Conclusion: We have generated a train of gain-switched pulses from a 1·55 μm DFB laser and successfully compressed them to 3·6 ps by fibre compression, which are the shortest pulses generated so far with this technique. We have experimentally studied the changes in the pulse width and time bandwidth product of the compressed pulse at various bias levels and found out that to obtain the shortest pulses, the laser should be biased well below its threshold whereas for achieving nearly transform-limited pulses with high peak power, bias current should preferably be set at slightly higher levels.

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APPLYING THE MARX BANK CIRCUIT CONFIGURATION TO POWER MOSFETs

R. J. Baker and B. P. Johnson

Indexing terms: Circuit design, Pulse generation, Power MOSFETs

Power MOSFETs operated in a Marx bank circuit configuration are presented. This circuit is useful for generating high voltage (greater than 1 kV) nanosecond risetime pulses. After the design procedure is given an example circuit is designed which generates a −1800 V pulse with a 3·0 ns falltime into 50 Ω.

Introduction: At present, the generation of nanosecond risetime pulses with amplitudes in the thousands of volts range relies on tubes such as the planar triode, krytron or thyratron. Power MOSFETs offer an attractive alternative to these tubes in some cases. Unlimited lifetime, lower average power dissipation, smaller physical size and lower on-resistance are some of the benefits of power MOSFETs. The main limitation in using power MOSFETs has been their breakdown voltage (at most 1 kV for commercially available devices). This Letter demonstrates that using the power MOSFET in a Marx configuration can overcome this limitation.

Marx bank circuit: Fig. 1 shows the basic schematic diagram of a power MOSFET Marx bank. The number of MOSFETs used will determine the output voltage across the load. Ideally

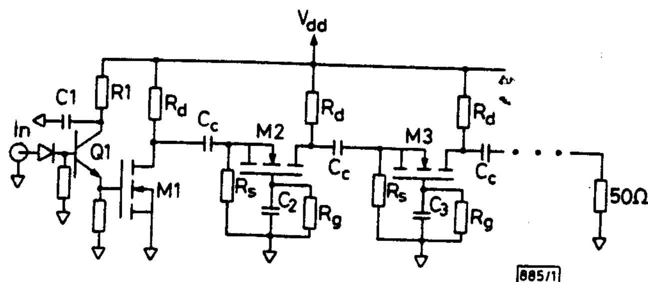

Fig. 1 *Circuit configuration for MARX bank of power MOSFETs*

if three MOSFETs are used then the output amplitude is $3 \times (V_{dd})$, where V_{dd} is the supply voltage. Transistor Q1 is operated as an avalanche transistor. When Q1 is triggered it rapidly charges the input capacitance of M1 causing the drain potential of M1 to change from V_{dd} to zero. This in turn causes the source potential of M2 to change from zero to $-V_{dd}$. The source potential of M3 changes from zero to $-2V_{dd}$ and so on down the line. The main concern during switching is keeping the potential difference between the gate and source of each MOSFET below 20 V. If the gate-source potential increases above 20 V, puncturing of the SiO_2 interface may occur leading to MOSFET failure. Because the resistances R_g and R_s are large compared to the capacitive reactances present in the circuit they will be ignored in the following analysis.

The effective gate-source capacitance of any MOSFET in Fig. 1 is given by

$$C_{gseff} = C_{gs} + \frac{dV_d}{dV_g} \cdot C_{gd} \tag{1}$$

where the second term is the Miller capacitance and the effects of C_{ds} have been ignored. For MOSFET M2 in Fig. 1 a capacitive voltage divider exists between C_{gseff} and C2 during switching. The value of C2 is determined by (assuming 20 V maximum between the gate and source)

$$\Delta V_{gs2} = 20 = \Delta V_{s2} \cdot \frac{C2}{C2 + C_{gseff}}$$

and

$$C2 = \frac{20 \,.\, C_{gseff}}{\Delta V_{s2} - 20} \tag{2}$$

where ΔV_{s2} is the change in the source potential ($\Delta V_{s2} = V_{dd}$) of M2. For M3, $\Delta V_{s3} = 2 \cdot \Delta V_{s2}$ or for the nth MOSFET in the Marx bank $\Delta V_{sN} = (N-1) \cdot \Delta V_{s2}$. Because ΔV_{s2} is much larger than 20 V the other gate capacitors can be determined by

$$C_N \simeq \frac{1}{N-1} C2 \qquad \text{for } N > 2 \quad (3)$$

Using eqns. 1–3 a Marx bank circuit can be designed using power MOSFETs.

Resistors R_d, R_g and R_s are used to provide a DC path for biasing. These resistors bias the drain of each MOSFET at V_{dd} and the gate and source at approximately 0 V. The values of R_s, R_g and R_d are typically in the range of several tens of thousands of ohms. Two factors must be considered when selecting these resistances: the leakage current through the devices and the amount of current lost through these resistors during switching. The coupling capacitors C_c must be large compared to the capacitance at each source node to ground, i.e. the effective gate-source capacitance in series with the gate capacitor to ground, in order for C_c to have little effect on switching behaviour.

Example: Using the procedure given above a Marx bank pulse generator will now be designed. Five IRF740 power MOSFETs are used with a voltage supply of 420 V. The UIRF740 is rated at 400 V breakdown and 40 A peak pulsed current. The gate-source capacitance is 1300 pF and the drain-gate capacitance is 37 pF. Because the drain-source potential will change by 400 V and the gate-source potential will change by 20 V, $dV_d/dV_s = 20$. Using eqn. 1 the effective gate source capacitance is $1300 + 20 \times 37 \simeq 2000$ pF. The gate capacitors are, using eqns. 2 and 3, C2 = 100 pF, C3 = 50 pF, C4 = 33 pF and C5 = 25 pF. The biasing resistors are selected as $R_d = 510\,\text{k}\Omega$, $R_g = R_s = 51\,\text{k}\Omega$. The coupling capacitor $C_c = 4700$ pF. The avalanche transistor Q1 breaks down at 120 V so the capacitance C1 is 470 pF. This value is determined by treating the avalanche transistor as a perfect switch and using a capacitive voltage divider between C1 and the input capacitance of M1 (2000 pF). The output of this pulse generator is shown in Fig. 2. The amplitude out is −1800 V (36 A) and the fall time is 2·97 ns. Pulse jitter was negligible.

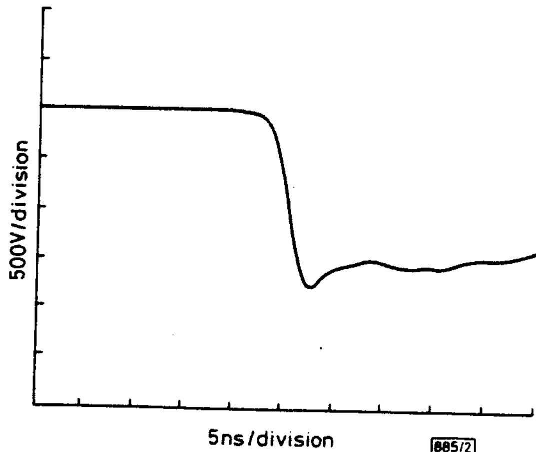

Fig. 2 *Output of power MOSFET Marx bank*

Ideally a 2000 V pulse would be generated in the design above. The on-resistance of each MOSFET is approximately 1 Ω, at a drain current of 30 A. As the drain current is increased further the on-resistance increases exponentially. This resistance lowers the output amplitude to a value less than the ideal output amplitude.

In this example a 50 Ω load was driven, however the techniques presented here can be applied to any type of load. The designer must determine the peak current the circuit must supply to the load as well as the peak voltage. The peak current will determine the type of power MOSFET used and the peak voltage will determine how many devices are needed.

Conclusion: Design procedures for operating power MOSFETs in a Marx bank circuit configuration were presented. Using these procedures a circuit was designed which generates a −1800 V pulse with a 2·97 ns falltime into 50 Ω. This configuration should find applications in streak camera ramp design, gating microchannel plate image intensifiers, gating Pockell cells, pumping lasers and driving thyristors to name a few applications.

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INFLUENCE OF RESISTANCES ON CHARACTERISTICS OF VERTICALLY INTEGRATED RESONANT TUNNELLING DIODES

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Indexing terms: Diodes, Tunnel diodes

An equivalent circuit for vertically integrated resonant tunnelling diodes with different diode area is proposed. Vertical and horizontal current paths through the structure are characterised by resistances which explain the difference between the characteristics of a monolithically integrated and a discrete series connection.

Resonant tunnelling diodes (RTDs) are useful devices for high speed applications with reduced circuit complexity. Special interest is being paid to RTD circuits with multiple negative differential resistance (NDR) regions in the current–voltage characteristic.

There are several ways to produce multiple NDR regions using RTDs. In this Letter we use a monolithic integration of two RTDs whose discrete characteristics are based on the compelled backswitching mechanism [1–3]. This mechanism generates $2^n - 1$ current peaks from a series connection of n RTDs, which is explained in detail in References 2 and 4. The layers for the monolithically integrated series connection of two RTDs are grown by molecular beam epitaxy. Both RTDs consist of a 6 nm GaAs well and 3 nm AlAs barriers. The RTD with the largest PTVR is grown on top. The contact layer between both diodes is highly doped. The larger PTVR of the top RTD is obtained by the inclusion of a 5 nm undoped GaAs layer surrounding the barriers. The bottom RTD has a 1 nm thick $Al_{0.08}Ga_{0.92}As$ layer in front of the one barrier. The mesas are defined by wet etching such that the area of the bottom mesa is the largest.

Measurements on this monolithically integrated structure gave I–V characteristics which differ from the characteristics of the discrete series connection of the RTDs. To model this behaviour, we use an equivalent circuit, given in Fig. 1, with a current path in the direction parallel to the layer structure characterised by a resistance R. This resistance influences the shape of the measured characteristics of the monolithically integrated structure.

The circuit (Fig. 1) is composed of three resistances and in fact of three resonant tunnelling diodes instead of the physical two. This can be explained as follows. The vertical resistances R_{s1} and R_{s2} quantify the contacting layers and the horizontal resistance R describes the horizontal current flow. This resistance is a result of the current spreading in the contact layer between the two RTDs when the top mesa has a smaller area than the bottom mesa. This process mainly causes a division of the area of the bottom RTD resulting in a parallel connection of two RTDs. This is completely different from the series connection of discrete RTDs. This parallel connection will generate two current peaks. The voltage partition between