

A Current-Mode Photon Counting Circuit for Long-Range LiDAR Applications

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Abstract— Photon counting techniques are becoming more critical in fields such as LiDAR, high energy physics (HEP) and positron emission tomography (PET). For space-based aerosol-cloud-ocean (ACO) LIDAR, the total aggregate photon flux signal has a very high dynamic range from a single-photon up to giga-photons per second for a single channel. A current-mode front-end can accommodate this counting dynamic range over a wide range of input signal current pulse amplitudes. A multi-channel current-mode photon counting circuit was designed, simulated, and fabricated in a standard 180 nm SiGe BiCMOS process. This photon counting circuit achieved a maximum count rate of 500 MHz with a 300 ps FWHM pulse width at amplitudes of 5 μ A to 1.25 mA.

Keywords — *readout integrated circuit (ROIC), silicon photomultiplier (SiPM), avalanche photodiode (APD), photon counting, LiDAR, photomultiplier tube (PMT)*

I. INTRODUCTION

The design of photon counting receivers has recently gained considerable interest especially in the development of long-range LiDAR applications [1-3]. An interesting application for LIDAR is for aerosol, cloud and oceanographic (ACO) measurements. In order to achieve stringent dynamic range and timing requirements of these applications, the photodetectors need to output a relatively high amplitude, short length pulse in response to a single incident photon and the read-out circuitry needs to count these short pulses without saturating. The photodetectors used for LIDAR applications are either solid state detectors such as silicon-photomultipliers (SiPM) and avalanche photodiodes (APD); or vacuum detectors such as micro-channel plate photomultiplier tubes (MCP-PMT). The main benefits of using solid-state detectors (SSD) are that they are physically compact and have magnetic immunity that lends to their application in medical imaging scanners like MRIs. Alternatively, MCP-PMTs are physically larger and require high bias voltages but are much less vulnerable to variations in temperature and supply voltage than SiPMs. Moreover, MCP-PMTs have other advantages like lower dark counts and better radiation hardness than SiPMs. This makes the MCP-PMT a better candidate for space based ACO LIDAR applications. A high-performance read-out integrated circuit (ROIC) is critical to realizing the full performance potential of an MCP-PMT based LIDAR system.

A conventional photon counting circuit uses a transimpedance amplifier (TIA) as the first stage, which amplifies the input current from the photodetector to a voltage. Conversely, in the current-mode approach using a current-conveyer, the input current is directly amplified into a larger current before being fed into additional processing stages. This avoids the gain-bandwidth limitations and stability issues inherent in traditional TIA designs [4]. The proposed photon-counting ROIC uses a current-conveyer as the input stage. The output of the current conveyer will convey the change caused by the input current to the following stages. The comparators can also be accordingly designed, so that it can track the change in current and make accurate decisions.

Recently, current-mode photon counting circuits have gained more popularity than its voltage mode counterpart. The main reason for this is that the current-mode approach provides a higher bandwidth and therefore can be used for applications with short detector pulses. Another advantage of the current conveyer is that it can provide a larger dynamic range. Typically, the maximum input current that can be injected or stolen from the input node is only limited by the bias current flowing in the current conveyer. Therefore, by increasing the bias current, one can easily achieve a large dynamic range. However, this comes at the cost of higher power consumption.

Many designs have been introduced in the literature that make use of the current mode approach [1-3]. Two current buffers introduced in [1] are one of the initial designs. This, however, was developed to read the output of a SiPM. Another design that uses a current-mode approach is illustrated in [2]. This is also a SiPM based readout circuit which is mainly developed for an MRI-compatible single photon emission computed tomography (SPECT). However, incorporation of many modules tends to make this system more complex and also eventually leads to more power consumption. It has to be noted that most of these are developed to readout solid state detectors. Therefore, its compatibility with other photodetectors has to be verified. Moreover, in most of these applications the dynamic range of the photon flux is not high and the ROIC design can be tailored for a narrow dynamic range. For a long-range LiDAR application, it is necessary to implement a circuit that has the high bandwidth to detect very

short pulses (300 ps FWHM) and a high counting dynamic range (1 GHz).

This work introduces the design of a multichannel, photon counting readout circuit that can interface with MCP-PMTs for high dynamic range, space-based LIDAR applications. The readout circuit is designed in a standard 180nm SiGe BiCMOS process. The paper is organized as follows. Section II provides brief description of the circuits that are used. Section III illustrates the simulated result and concluded in section IV.

II. CIRCUIT DESCRIPTION

One of the main limitations of the current voltage mode approach is the gain-bandwidth trade-off. The requirements of LIDAR systems demand the use of a current-mode approach for photon counting circuits. Figure 1 shows the block diagram of the current-mode based photon counting system. It consists of two current conveyor circuits (CC) [5], followed by a high-speed comparator. The photodetector is connected to one of the current conveyors and a reference current is connected to the other. The comparator makes a decision and gives a digital “high” if the amplitude of the photocurrent pulse is higher than the reference current.

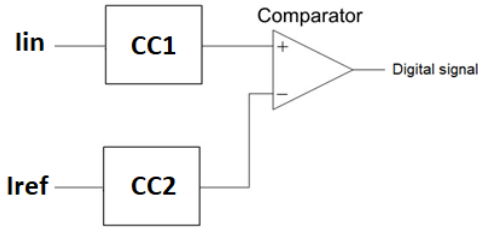


Figure 1: Block diagram of a current-mode photon counting system

A. Current Conveyor

Figure 2 illustrates the schematic of the BiCMOS current conveyor circuit. It can be seen that all the nodes of the current conveyor are at low impedance. This will help in pushing all the associated poles to a higher frequency and thus a high bandwidth can be attained. The advantage of using Heterojunction bipolar transistors (HBT) is that it can ensure low input impedance and high transconductance with reduced layout area compared to a CMOS device. Moreover, the HBT is inherently radiation hard due to a thin, heavily doped base junction [6]. The purpose of the voltage source V_{ref} is to set the V_{be} voltage of Q1 and Q2 so that the input to the detector is at a known fixed voltage. The benefit of doing this is that every node in the current conveyor is connected to a known voltage.

The operation of the current conveyor is straightforward. When a current, I_{in} , corresponding to the detector photocurrent is “stolen” from the input node (emitter of Q1), the voltage at that node will decrease. This will result in an increase in collector current of Q1 and increase the current in the PMOS current mirror (M1 and M2). As a result, the voltage at the output node, Out , will decrease. Due to the current mirroring between the transistors Q1 and Q2, the voltage at input node will be reset back to the voltage, V_{ref} when there is no detector current. In order to accommodate a large dynamic range, the

bias current of the current conveyor can be increased. This also provides an extra benefit of increased bandwidth. However, this will also result in the increase of the overall power consumption of the current conveyor.

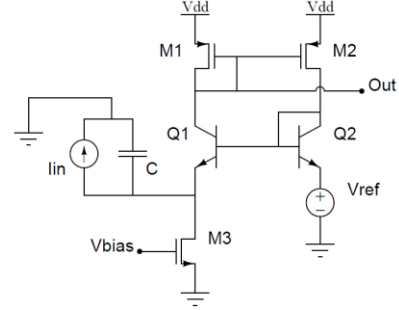


Figure 2: Schematic diagram of a current conveyor

Similarly, the input-output relationship of the current conveyor is illustrated in Figure 3. The output voltage of the current conveyor decreases linearly with the increase in current flowing out of the input node. When the current flow from the input node goes higher than 3.5mA (bias current level), Q1 will no longer be in the active region and therefore the output is no longer linear with the input.

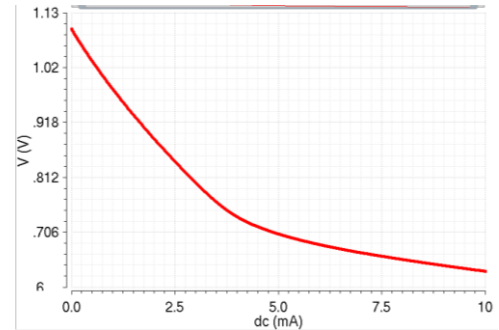


Figure 3: Input current range of the current conveyor

The input resistance of the current conveyor is also controlled by the bias current. Since the emitter of Q1 can be seen at the input of the current conveyor, the input resistance can be approximated as:

$$r_{in} \approx 1/g_m = V_T/I_C$$

Where g_m is the transconductance of the transistor Q1, V_T is the thermal voltage, and I_C is the collector current of Q1. A very low input resistance can be easily obtained by increasing the bias current of the current conveyor. This will also give an extra benefit of improved bandwidth but with higher power consumption. The transient results illustrated in Figure 4(a) shows the response of the current conveyor for a 300 ps FWHM current pulse with a 5uA amplitude at a repetition frequency of 500 MHz. It can be seen that the output voltage of the current conveyor swings by around 700μV. This voltage level is sufficient for the high-speed comparator to switch states. Similarly, Figure 4(b) shows the response of the current conveyor for a 300 ps FWHM pulse but with an amplitude of

1.25mA at a 500 MHz repetition rate; illustrating that the current conveyor has a large input photocurrent range.

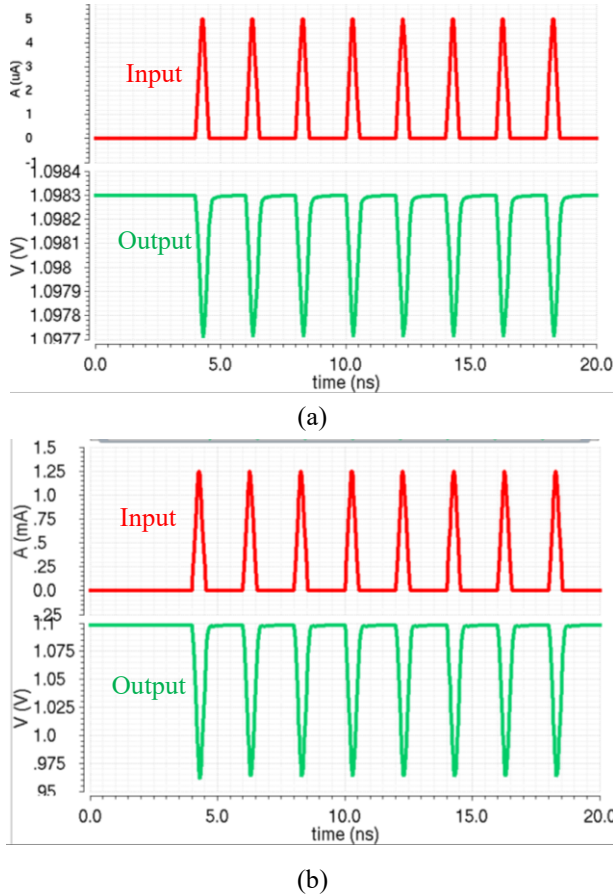


Figure 4: Transient response of current conveyor for a) 5µA current pulse b) 1.25mA current pulse

B. High-speed comparator

A high-speed comparator is needed to convert the small voltage output from the current conveyor to a logic level signal for further processing. The schematic of the comparator can be seen in the Figure 5. The first stage of the comparator is the decision stage, which will be used to discriminate the voltage levels from the current conveyor. The output of the decision stage is amplified using two output buffers followed by the inverter chains to obtain valid digital signals.

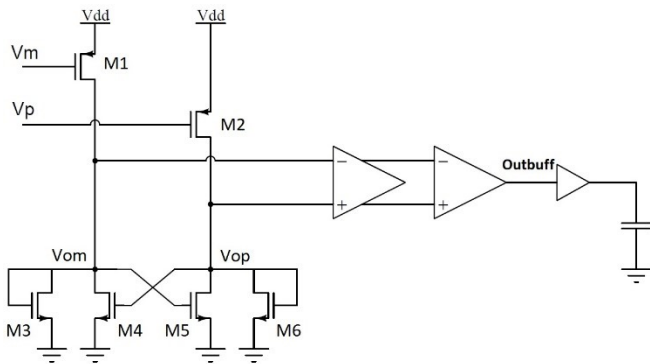


Figure 5: Comparator schematic

The bias current of the decision stage will be determined by the PMOS current mirror of the current conveyors (in this case, 3.5mA). The positive feedback made by transistors M4 and M5 will help in increasing the gain of the decision element. The diode connected transistors M3 and M6 are used to reduce the positive feedback gain and thereby helping the comparator to switch easily to different output states.

Figure 6 shows the response of the comparator, when the input is changed by 700µV. This corresponds to the change in the current conveyor output for a 5µA current pulse. Depending on the change in V_{in} , the decision stage in the comparator changes the state of V_{op} and V_{om} , which is illustrated in Figure 6. The decision stage output provides a signal swing of almost 10mV_{pp}. This voltage swing is then further amplified using the output buffers and thus a logic level swing is obtained at the input of the inverter chains. Another important thing that can be noted is that the inverter has to be properly sized so that the switching point is within the output range of the buffer.

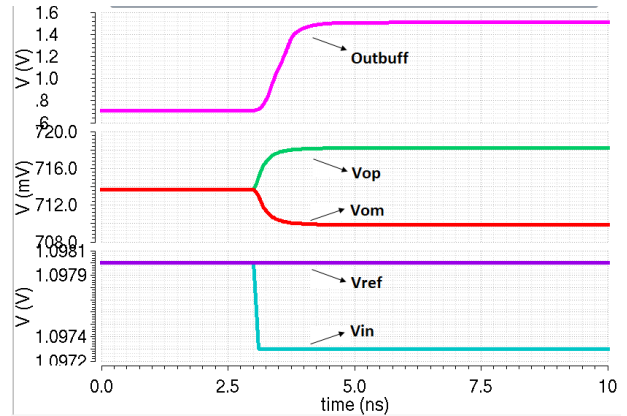


Figure 6: Comparator simulation results

A self-biased differential amplifier is used as the output buffers. This is illustrated in Figure 7. The advantage of such topology is that it can provide very high speed. A higher gain can be obtained for the differential amplifier by increasing the transconductance of the input devices (wide devices). However, this will also result in higher input capacitance and thereby reducing the overall speed.

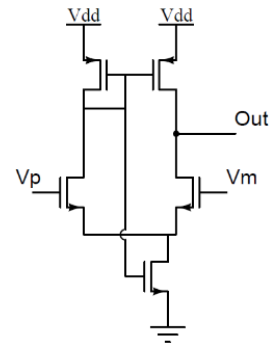


Figure 7: Self-biased differential amplifier

In order to ensure maximum gain, it is also essential for the output of the decision stage, V_{op} and V_{om} , to be within the

common-mode range of the differential amplifier. The AC response of the self-biased differential amplifier is simulated and a gain of 20dB is obtained.

III. SIMULATION RESULTS

A 4-channel readout circuit is designed and simulated in a standard 180nm SiGe BiCMOS process. The physical layout of the current mode photon counting circuit is illustrated in Figure 8. The complete layout occupies an area of 520um x 245um.

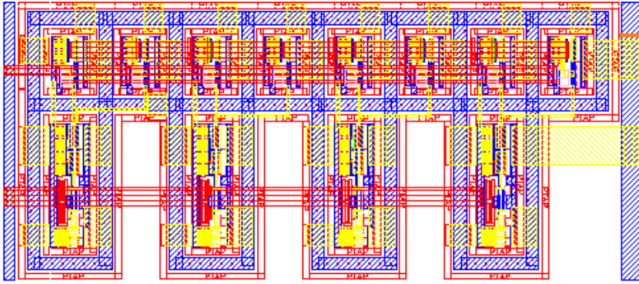


Figure 8: Physical layout of a 4-channel readout circuit

The complete system is simulated for different test cases in order to validate the performance in terms of bandwidth and dynamic range. An ideal current pulse source is used as the photodetector model for this circuit. The Full width at half maximum (FWHM) of the current source is set to be 300ps at a frequency of 500MHz. The amplitude of the pulses is alternated between 5 μ A and 125 μ A because one of the main performance concerns is whether the photon counting circuit can discriminate a low level pulse immediately after a high level pulse.

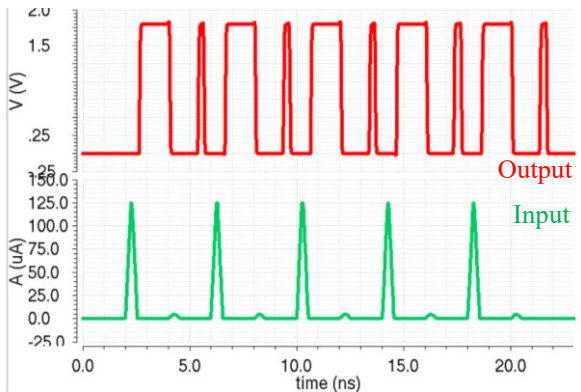


Figure 9: Transient response of the current conveyor for current pulses of 125 μ A and 5 μ A

The transient response of the readout circuit is seen in Figure 9. The magnitudes of the alternating input pulse train are set to 125 μ A and 5 μ A. It is observed that the output of the readout circuit provides valid digital signals. The output of the readout circuit also exhibits a delay of about 300 ps. This is mainly caused by the inverter buffer chains used in the comparator. In order to further validate the circuit's dynamic range, the magnitudes of the alternating input pulse train are changed to 1.25mA and 50 μ A. The transient response of the readout circuit is illustrated again in Figure 10 showing a 500 MHz count rate.

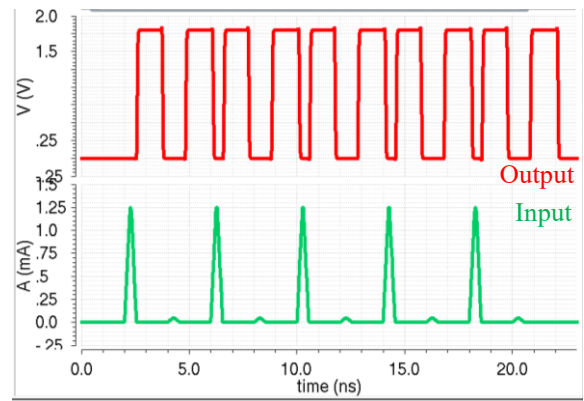


Figure 10: Transient response of the current conveyor for current pulses of 1.25mA and 50 μ A

IV. CONCLUSION

A current-mode photon counting circuit with large counting dynamic range and bandwidth is presented in this paper. This photon counting circuit is realized using SiGe HBT based current conveyors to overcome limitations in traditional TIA based approaches. The circuit was implemented in a standard 180nm SiGe BiCMOS process. The simulations conducted on the circuit confirms that it performs as intended and the results are summarized in Table I. Future efforts include testing the fabricated circuits to confirm they meet the simulated specifications.

TABLE I. SUMMARY OF RESULTS

| Parameter | Value |
|---------------------|--------------------------------|
| Process | 180nm SiGe BiCMOS |
| Supply Voltage | 1.8 V |
| Input current range | 5 μ A-1.25mA |
| Count Rate | 500 MHz for 300 ps FWHM pulses |
| Number of channels | 4 |
| Power consumption | 14.07mW/ch |

V. ACKNOWLEDGEMENTS

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