Variable Fast Transient Digitizer

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***Abstract*—A low cost, low power substitute for expensive, high power high-speed analog-to-digital converters (ADCs) in some situations is presented. This circuit is called a variable fast transient digitizer (VFTD). This paper provides an overview of the design and measured test results. The VFTD is designed to sample a high-speed analog input signal and later reconstruct the captured signal at a much slower rate, for example, around three orders of magnitude. This approach eliminates quantization error in the captured signal. Further, this approach enables the use of slow, low cost, analog-to-digital converters such as those found in microcontrollers. The VFTD discussed in this paper uses 256 sequential sample and hold cells with a process dependent variable delay element controlled by an off-chip voltage source. Using a power supply voltage of 5V the input range extends from 0 V to 3 V corresponding to an output voltage range from 2 V to 5 V, a capture window range from 81 ns to 1.78 µs, and a sampling rate range from 143.82 MS/s to 3.16 GS/s. The VFTD is fabricated on a 2 mm x 2 mm die using ON Semiconductor's 0.5 µm C5 process and requires a 0.5 mm x 1.5 mm area.**

I. Introduction

As circuits and components in modern electronics continue to decrease in size and subsequently increase in speed, the need to develop inexpensive, fast and efficient methods to capture and process information increases. Specifically, the ability to capture transient and high-speed analog signals is a common goal shared in a multitude of fields. These analog signals are used for a variety of applications including, but not limited to, telecommunications, electro-optics, photonics, biomedical, and many application-specific integrated circuit (ASIC) designs. Typically, modern implementations that deal with such signals use high-speed analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and various filters. These components tend to be bulky, expensive, consume excessive power, or have very specific operating frequencies. Some applications require detection and analysis of signals that have very narrow pulses. These applications traditionally detect the pulses using a threshold method [1]. However, using the FTD to capture a fast, and narrow pulse, allows for detecting pulses of continuous amplitude. Also, modern detection systems use thresholds to trigger an event, wherein the proposed Variable Fast Transient Digitizer (VFTD) allows complete analysis of the captured signal, rather than generating a pulse once a threshold has been reached [2].

The Fast Transient Digitizer (FTD) introduced by Buck and Baker was developed to address the need for a way to efficiently capture transients or high-speed analog signals and later reproduce a slowed or stretched out version of the captured signal for analysis with minimal loss of the original signal [3]. This eliminated the need for ADCs, DACs, and additional filters, such as reconstruction and anti-aliasing filters. The FTD's capture sequence behaves like 128 sequential track and hold capture stage cells with an effective sampling rate of 4.3 GS/s [3, 4]. However, one of the drawbacks of the FTD topology is it has a fixed capture rate that limits the number of useful applications of the design.

The VFTD aims to address the need for a variable sampling rate by redesigning the FTD's capture stage cells to include current starved inverters controlled by a DC bias voltage generated via an on-chip bias generator. The VFTD design allows for an equivalent, variable time delay throughout the 256 sequential capture stages that can be adjusted for application specific needs. The VFTD allows for sampling rates ranging from hundreds of MS/s to 3.16 GS/s, as compared to the FTD operating at the single sampling rate of 4.08 GS/s.

II. Theory of Operation

The VFTD consists of two major components, the bias generator and the sampling circuit. The bias generator is a simple voltage-controlled beta-multiplier as seen in Figure 1. The bias generator design includes an NMOS device controlled by an off-chip control voltage (Vc) and an off-chip bias resistor (Bias_R) [5]. This provides two external methods for adjusting current flow and results in a voltage-controlled current that is process, voltage, and temperature invariant [6].

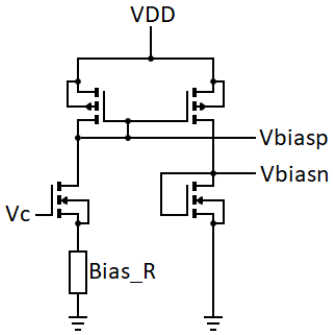

Figure 1: Bias generator

The second component is the sampling circuit consisting of 256 capture stage cells. This is effectively a tapped-delay-line that controls the sampling of the signal. Figure 2 shows a single capture stage cell. The delay element consists of a single CMOS current-starved inverter (M1-M4) and a basic CMOS inverter (M5-M6). The bias generator bias voltages, Vbiasp and Vbiasn, are used to set the bias in M4 and M1, respectively. Varying Vc and/or Bias_R adjusts the current flow through the current-starved inverter and consequently allows the delay through each capture stage to be varied. In this manner, the VFTD implements a variable sampling rate.

The capture stage operation begins when an externally generated trigger signal, Trig_in, transitions from high to low and propagates through the delay element to the gate of the NMOS M7. The analog input signal of interest, Analog_in, is connected to the drain of M7 and feeding through to the hold capacitor, C_Hold, node connected to both the source of M7 and the gate of PMOS M8. The capacitor value is selected based upon the thermal noise and settling time [5]. When Trig_in propagates through the delay element, after a roughly 300 ps delay, M7 switches off and a sample of the input analog signal is captured on the hold capacitor. Simultaneously, the trigger output signal, Trig_out, then propagates to the input of the delay element in the next sequential capture stage and the process repeats itself. In this manner, the 256 capture stages iteratively sample the input signal. The overall capture window is therefore defined as the time between the initial input trigger entering the first capture stage and the final output trigger exiting the last stage. The number of capture stages can be scaled according to application specific requirements.

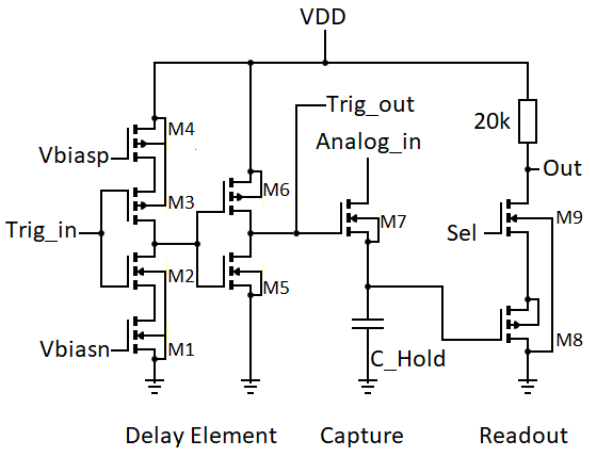

Figure 2 Schematic of a single capture stage unit cell with delay element

The readout portion of the cell includes a PMOS, M8, in a source follower configuration with an NMOS, M9, connected to its source. The current flowing in M8 is set by the voltage captured on the hold capacitor and ultimately determines the voltage on the output node. An NMOS was selected as the hold capacitor switch due to its ability to pass logic 0's well compared to PMOS devices which are able to pass logic 1's well. This allows the minimum analog input voltage range to go down to ground and bias M8 such that it remains in saturation and is therefore able to create a scaled representation of Analog_in. The maximum input signal range is set by the point wherein M8 enters triode and was determined to be 3 V.

M9 is a switch activated by control logic from an on-chip 8:256 decoder, connected to the gate of M9, Sel, during readout of the sampled signal. Recreating a slowed, or stretched out, version of the sample of Analog_in requires the stages to be readout sequentially with only one stage active at any given time. The decoder is controlled via binary values from 0 to 255 from an off-chip counter and ensures only one capture stage is active at any time.

Connecting a 20 kΩ pull-up resistor from the outputs of all the capture stages, labeled Out, to VDD results in a current controlled voltage drop proportional to the sampled signal. The resulting output signal is a stretched and level-shifted reconstruction of the original input signal.

III. VFTD Test System

The test system includes a PCB for the VFTD integrated circuit (IC), Figure 3, an Arduino Uno microcontroller, an 8-bit counter IC, and a debounced push button switch used to trigger the Arduino and initiate the capture and readout sequences. Additionally, the PCB has male headers for external signal interfacing and SMA connectors used for the analog input signal, reconstructed output signal, the function generator serving as the clock for the counter, and the output trigger signal. The output trigger was included to enable a means of measuring the capture window through 256 stages. The test equipment included two power supplies, a function generator, and and an oscilloscope.

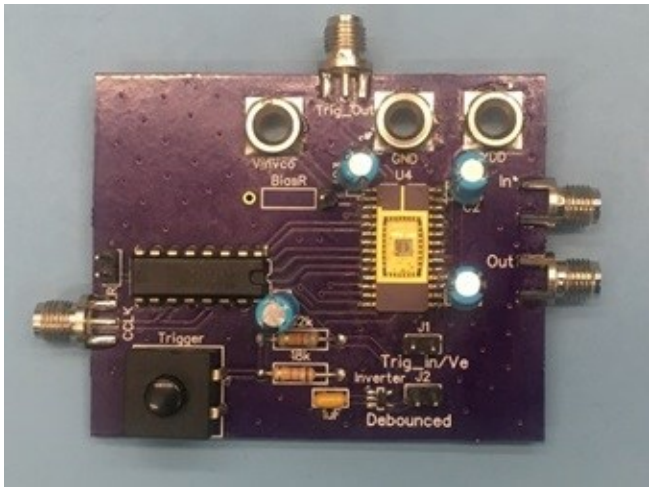

Figure 3: VFTD test PCB design

IV. VFTD Experimental Results

The VFTD IC was fabricated on a 2 mm x 2mm die using On Semiconductor's C5 process and requires an area of 0.5 mm x 1.5 mm and 19 pads. Figure 4 shows a photomicrograph of the wirebonded IC. All wirebonding, packaging, and testing of the VFTD IC was performed at the University of Nevada, Las Vegas.

The device characterization focus is on demonstrating the variable sampling rate since basic circuit functionality has already been established [3]. This is accomplished by adjusting Vc, Bias_R, or both giving two degrees of control. First, Vc is set to 5 V with a 2 kΩ bias resistor, as seen in Figure 5. In Figure 5 in the top frame, the 81 ns capture window is framed by the signals Trig_in and Trig_out with the sample of Analog_in, a 20 MHz, 3 V peak-to-peak sinusoid, taken between these signals. This ensures the input signal stays within the input range required for linear reconstruction of the signal. Note the time scale division in the top frame is 10 ns

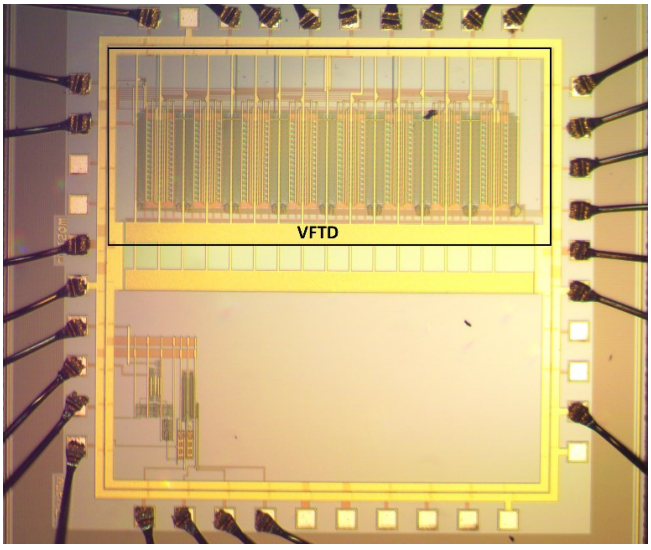

Figure 4: VFTD IC photomicrograph

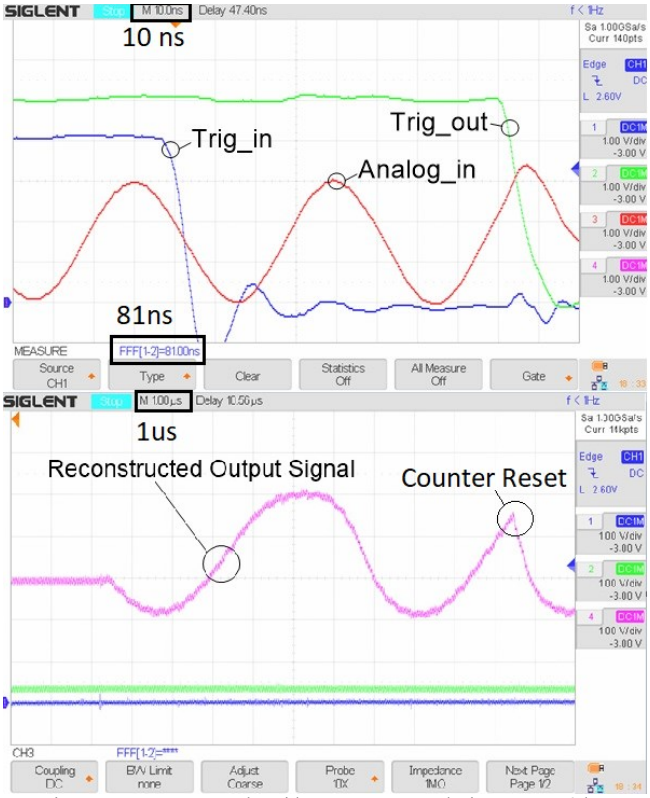

Figure 5: VFTD test results with Vc set to 5 V and Bias_R set to 2 kΩ

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Next, in Figure 5 the bottom frame time scale division is set to 1 µs and shows the reconstructed output signal stretched over 10 µs. The apparent discontinuity in the reconstruction is the result of the off-chip counter used to decode the capture stages resetting to zero and decoding the signal again. The VFTD effectively captured one and one half cycles of a 20 MHz sinusoid and reconstructed it as a 150 kHz signal.

Knowing there are 256 capture stages and using the values from Figure 5, the time delay through a single capture stage can then be determined by

$$t_{d,stage} = \frac{t_{d,capture\ window}}{256\ stages} = \frac{81\ ns}{256} = 316.0\ ps \qquad (1)$$

Test results using Vc set to 5V and Bias_R set to 2 kΩ results in an effective maximum sampling frequency given by

$$f_{sample} = \frac{1}{t_{delay,stage}} = \frac{1}{316\ ps} = 3.16\ GS/s \qquad (2)$$

Further testing is done by varying Vc and/or Bias_R, as summarized in Table 1 with simulation results also included for comparison. Table 1 results verify that changing Vc or Bias_R results in variations in the duration of the capture window, and consequently, the sampling frequency. Testing was performed with a maximum bias resistor value of 57 kΩ to demonstrate circuit functionality, however it should be noted that the sampling rate can be extended to a longer time duration by further increasing the size of the bias resistor. It is noted that the maximum sampling frequency achievable occurs with Vc set to 5 V and Bias_R set to 2 kΩ or less. Bias resistors with values less than 2 kΩ result in no appreciable performance improvements. The difference between the simulation and experimental values can be related to additional parasitics present during testing that are not modeled during simulations.

Additional tests demonstrate the VFTD can capture and reconstruct samples of various transients. Figure 6 displays the results using the maximum sampling frequency, 3.16 GS/s, or an 81 ns capture window, for a slow ramp up to 2 V, a step, and a fast ramp down. to 0 V. The time scale division in the top frame is set to 5 ns with 14 total divisions for a total window of 70ns, thus verifying the signal fits within the 81 ns capture window. The reconstructed, stretched signal is seen in the bottom frame of Figure 6 with a 1 µs time scale division for a 14 µs reconstruction window.

TABLE I. COMPARISON OF SIMULATIONS AND EXPERIMENTAL TEST RESULTS

Vc	Bias_R	Capture Window Simulation	Capture Window Experimental	Sampling Frequency Simulation	Sampling Frequency Experimental
5 V	2 kΩ	75.48 ns	81.00 ns	3.39 GS/s	3.16 GS/s
1 V	2 kΩ	294.85 ns	384.00 ns	949.00 MS/s	666.67 MS/s
1 V	4 kΩ	380.58 ns	542.00 ns	672.00 MS/s	472.32 MS/s
1.5 V	57 kΩ	1.00 µs	1.78 µs	256.00 MS/s	143.82 MS/s

Table II displays a comparison of the VFTD with the original FTD cited earlier in this work [3]. One difference is the layout area required for the VFTD for 256 stages is slightly larger than the FTD layout for only 128 stages. An additional advantage of the VFTD is the ability to vary the sampling frequency. The FTD has an advantage in maximum sampling frequency at 4.08 GS/s, however it is limited to a fixed frequency versus the VFTD with a much wider range of sampling frequencies.

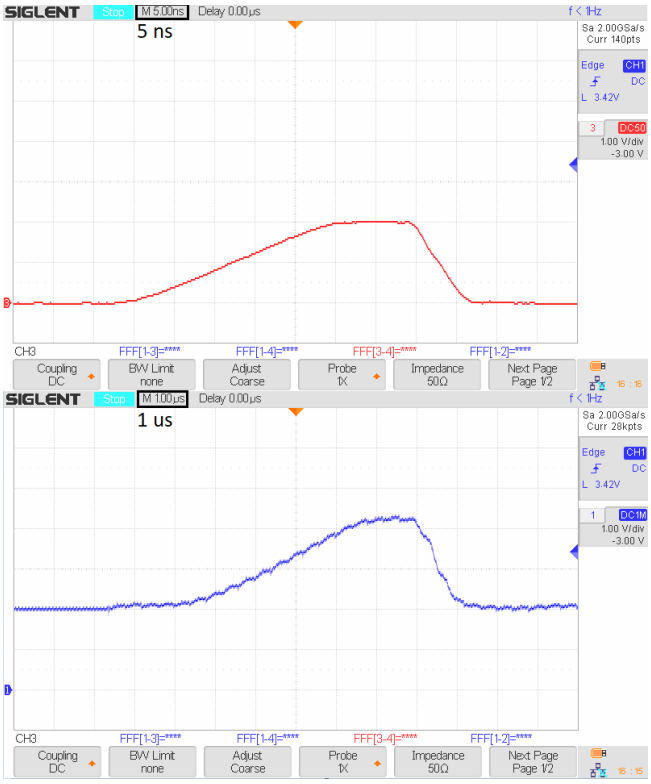

Figure 6: Test results for a slow ramp up, step, and fast ramp down

TABLE II. COMPARISON OF VFTD WITH PREVIOUS WORK [3]

Parameter	VFTD	FTD [3]
Technology	500 nm	500 nm
Number of Capture Stages	256	128
Layout Area	0.73 mm^2	.49 mm^2
Measured Capture Window	81.00 ns - 1.78 µs	31.40 ns
Sampling Frequency	3.39 GS/s - 143.82 MS/s	4.08 GS/s

V. CONCLUSION AND FUTURE WORK

A variable fast transient digitizer IC has been designed, fabricated, and characterized using a 500 nm CMOS process. The IC comprises an area of 0.5 mm x 1.5 mm. The circuit can capture and accurately reconstruct high speed analog or transient input signals at a measured variable sampling rate ranging from 143.82 MS/s to 3.39 GS/s with the ability to decrease the lower range by increasing the bias resistor value. The reconstructed signal can be readout at a slower, desired rate set by an off-chip counter or microcontroller with a minimum rate of 10 kHz due to leakage associated with the size of the hold capacitor. The capture window ranges from a minimum of 81 ns up to a measured value of 1.78 µs. The size of the capture window can further be increased or decreased by scaling the number of capture stage cells as required. Future efforts include investigating the addition of interleaving banks of capture stages to increase the sampling frequency by a factor proportional to the number of banks. Further, investigating the design of a wide-swing FTD using transmission gates to extend the input and output signal range at the cost of layout area could be investigated.

REFERENCES

[1] B. Gosselin and M. Sawan, "Adaptive detection of action potentials using ultra low-power CMOS circuits," *2008 IEEE Biomedical Circuits and Systems Conference*, Baltimore, MD, 2008, pp. 209-212.

[2] Y. C. Chen, Y. M. Chung, H. P. Chou and C. I. Hsu, "A CMOS signal processing unit for silicon photodiode detectors," *2001 IEEE Nuclear Science Symposium Conference Record (Cat. No.01CH37310)*, San Diego, CA, USA, 2001, pp. 765-767 vol.2.

[3] K. Buck and R. J. Baker, "Fast Transient Digitizer Chip for Capturing Single-Shot Events," in 12th IEEE Dallas Circuits and Systems Conference, Dallas, 2016.

[4] R. J. Baker, CMOS Mixed Signal Circuit Design, 2nd ed., Hoboken, NJ: *1*, 2009.

[5] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., *John Wiley and Sons, Inc.*, 2010

[6] A. Sedra and K. Smith, Microelectronic Circuits, 7th ed., *Oxford University Press*, 2014