Segmented Digital SiPM

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***Abstract*—A digital silicon photomultiplier (SiPM) using segmentation technique is designed, simulated and fabricated in the AMS 0.35 µm SiGe BiCMOS process. The digital SiPM is intended for photon counting applications. The digital SiPM consists of 16 avalanche photodiodes (APD) each with active area of 24 µm x 24 µm arranged in a 4x4 array with series 236 kΩ quench resistors. The SiPM has a peak responsivity at 490 nm wavelength and a fill factor of 12.6 %. The digital SiPM generates an output 5-bit digital word that indicates the number of APDs triggered in the SiPM array at the rising edge of clock. Simulation results show that the digital SiPM can work at a maximum speed of 100 MS/s and uses 64.6 mW of power. The digital SiPM occupies an area of 0.38 mm².**

Keywords — digital SiPM, silicon photomultiplier (SiPM), avalanche photodiode (APD), photon counting, LiDAR, segmentation

I. Introduction

Photon counting applications usually demand very stringent performance requirements such as high photon detection efficiency (PDE) and low dark count rate (DCR). Vacuum photomultiplier tubes (PMT) and discrete avalanche photodiodes (APD) are the most commonly used detectors for photon counting. These detectors have drawbacks in terms of system reliability, complexity, high cost and aren't well suited for mass production. As a result, PMTs are being replaced by solid state photon detectors (SSD). Recently, SSDs are being used in several photon counting applications such as high energy physics, medical imaging and light detection and ranging (LIDAR). A Geiger-mode avalanche photodiode (Gm-APD) is one example of an SSD that is typically used for these applications. In its most basic form a Gm-APD is realized as a reverse biased PN junction. When the reverse bias voltage applied across the Gm-APD is beyond breakdown, the field inside the device will be high enough to trigger impact ionization and avalanche multiplication. This results in a considerable amount of gain for Gm-APD and thus a current output upon photon detection. The gain for a Gm-APD is so high that it is best viewed as a triggered device rather than a linear amplifier such as a PMT or conventional APD. A Gm-APD can break down due to either thermally generated carriers (a dark count) or due to incident light (a light count). The procedure of quantifying the light level incident on a Gm-APD is by counting the number of pulses in a unit time interval.

An extension of a Gm-APD is the silicon-photomultiplier (SiPM), which comprises an array of Gm-APDs connected in parallel. Figure 1 shows the schematic of a traditional SiPM on the left side and its equivalent electrical model on the right. The output current from a SiPM, I_{SiPM} is an integer multiple of the current flowing in each Gm-APD, with a maximum current level determined by the number of Gm-APDs in the SiPM array. This output current is then converted to voltage by a transimpedance amplifier (TIA) and then digitized with an analog to digital converter (ADC) in order to be processed by a digital system. However, the output signal from a SiPM can get degraded by different parasitics such as diode capacitance of the Gm-APDs, bond wires, on-chip interconnects, and external load. Therefore, the intrinsic photon counting capability of Gm-APDs cannot be fully utilized with a SiPM signal chain consisting of only a TIA and an ADC. One way to mitigate this problem is by implementing a "digital SiPM" [1]. This is usually achieved by performing an A/D conversion on each individual Gm-APD within a SiPM.

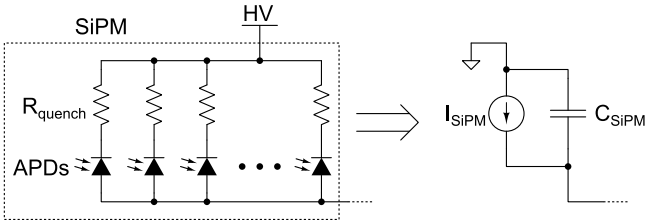

Figure 1: Simple electrical model of SiPM [2]

The Digital SiPM concept was initially introduced in [1] where individual APD signals are converted to digital signals. The output of each cell is then connected to an on-chip TDC for extracting the timing information. Although the digital SiPM can successfully mitigate parasitic effects, it comes with the drawback of reduced fill-factor associated with the conversion circuits present in every pixel. This additional circuitry takes up area in each cell of the SiPM that could have been otherwise used as a photodetector. Despite these drawbacks, the inclusion of digital circuitry on the same chip as the SiPM allows for the implementation of performance enhancement techniques not available in a conventional SiPM, and introduces new trade-offs in the design space [3,4]. The design in [3] mainly discusses compression techniques that can be implemented to reduce dark count rate. The design in [4] proposes the idea of a multi-channel digital SiPM which is used to improve fill factor by using a multi-channel SiPM resulting in less area occupied by electronic circuitry.

This paper proposes a digital SiPM using segmentation technique which is explained in section II. That is followed by the measurement results in section III and concluded in section IV. This work has similarities to the design in [4].

II. DIGITAL SIPM

In the traditional approach toward SiPM readout, the output of a SiPM, which is a current signal is fed into a transimpedance amplifier and the output of the transimpedance amplifier is then converted to a digital output using an ADC. A SiPM that contains a large number of cells has a wide dynamic range output. The dynamic range of the readout circuitry must match that of the SiPM if the full resolution of the SiPM is to be realized. For example, a SiPM with 4096 individual Gm-APDs would require a system with at least 12-bit accuracy. Silicon photomultipliers with pixel count in this range are commonly available on the market. The future trend is for SiPM pixel count to grow, which will result in increasing design difficulty for the high-speed analog front-end circuitry. The architecture described in this work mitigates the need for high performance analog circuits by doing an implicit data conversion for segments of Gm-APD cells in the SiPM and converting it directly to a digital number. Hence, the transimpedance amplifier is eliminated from the signal chain which results in the full dynamic range output from the digital SiPM.

Figure 2 shows the block diagram and physical structure of the designed digital SiPM. The SiPM is at the center. These are surrounded by the readout circuitry along the sides. The SiPM consisting of 16 APDs are segmented into 2 APDs per segment as indicated in Figure 2. The 8 segments are marked in the figure with each segment enclosing two APDs inside the SiPM array and the associated read-out circuitry. The readout circuitry detects the triggering of each APD and generates a corresponding digital signal on each rising edge of clock. Therefore, each segment generates two digital output signals. These signals from all segments are added together using multi-stage binary adders as seen in Figure 2 to generate the 5-bit digital result. Output data rate is equal to the clock frequency which can be a maximum of 100 MHz in this design. This result can be post-processed and used for photon counting applications. The count per unit time is directly proportional to the incident light intensity.

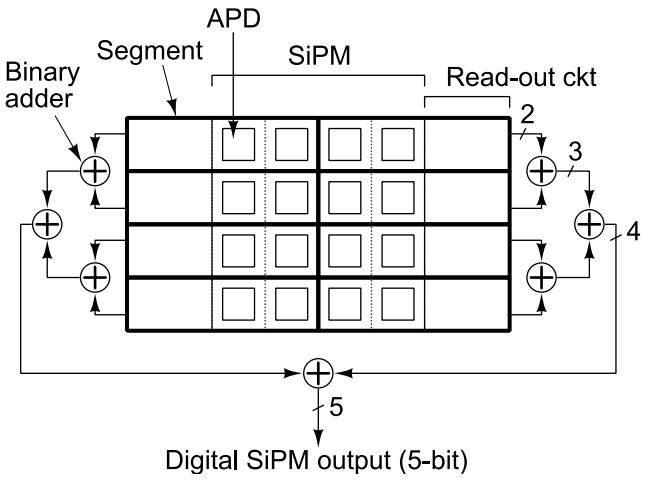

Figure 2: Block diagram of digital SiPM designed in this work

The readout circuitry present in each segment is shown in Figure 3. These consist of the two APDs with series quench resistors connected to a high voltage (HV). The APDs designed in this process technology need a bias voltage of about 11.5 V for Geiger mode operation. The output of the APDs is a current signal that is converted to a voltage using a transimpedance amplifier (TIA) [5]. Since the TIA input terminal has a bias voltage of about 3.8 V by design, the applied high voltage to the APDs needs to be offset by this value in order to maintain the breakdown voltage across the APDs. The APD current is given by Equation (1) [6] where $V_{HV} = 16\,V$, $V_{APD\_breakdown} = 11.5\,V$, $V_{TIA\_bias} = 3.8\,V$ and $R_{quench} = 236\,k\Omega$. This results in APD current of $I_{APD} = 3\,\mu A$. The TIA has constant gain of 50 kΩ for input currents from -25 µA to 40 µA which can accommodate two APD breakdown currents.

$$I_{APD} = \frac{V_{HV} - V_{APD\_breakdown} - V_{TIA\_bias}}{R_{quench}} \quad (1)$$

Since the APDs are operating in the Geiger mode, the output current is pseudo digital in that the value is either low or a high pulse. In order to resolve the two APDs triggering, the output of the TIA is compared against two reference voltages using two comparators. The reference voltages are common to all segments and are set such that they correspond to the output voltage of TIA when each APD trigger current is generated. The output of the comparators are latched using rising edge triggered flip-flops. This produces a synchronous output that is useful for readout. The clock for the flip-flops is common to all segments. An on-chip ring oscillator based voltage controlled oscillator (VCO) is used to generate the clock signals. This clock signal is also brought off-chip through a divide-by-2 clock divider. Clock and output data can be used to read the data synchronously into a digital system. A DSP or FPGA can be used to post-process the high-speed data.

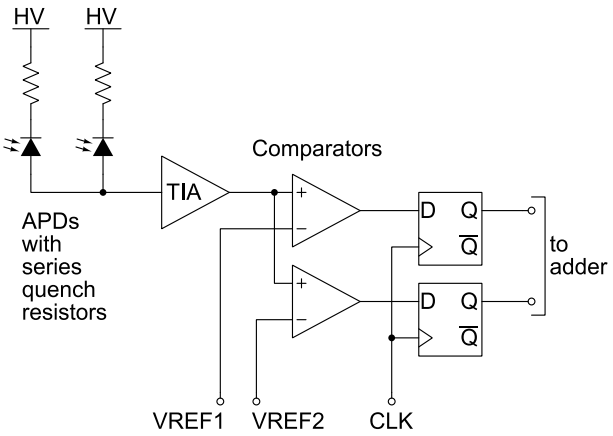

Figure 3: Single segment of digital SiPM showing APDs and associated read-out circuitry

Figure 4 shows the physical layout of the digital SiPM. The 4x4 SiPM is seen in the center. The 5-bit digital output is available on the center-bottom.

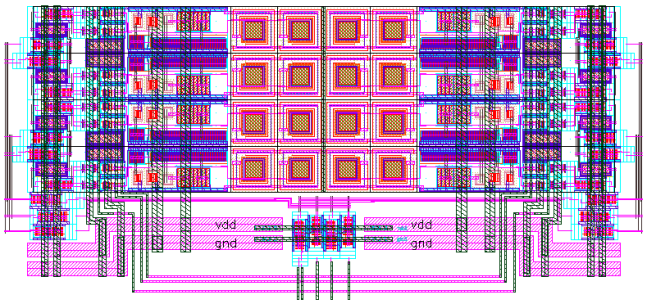

Figure 4: Physical layout of the segmented digital SiPM

The SiPM can be segmented in different configurations. In this design, each row is segmented in half as the left side and the right side as seen in Figure 5(a). Other examples of segmentation configurations are shown in Figure 5(b) and 5(c). These configurations have different tradeoffs of speed, area and power.

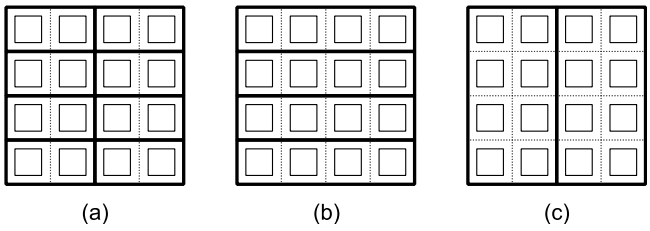

Figure 5: Examples of segmentation in digital SiPM. (a) Configuration used in this design using 2 APDs per segment, (b) Using 4 APDs per segment, (c) Using 8 APDs per segment

This work implements a digital SiPM with 4x4 APDs to demonstrate this segmentation architecture. This technique is scalable to larger SiPMs. However, there might be a tradeoff in the clock speed due to adder signal propagation.

The advantages of this segmented digital SiPM architecture are listed below:

- The entire dynamic range of the SiPM is available at the digital output
- Fill factor improvement due to not having processing circuitry inside each cell of the SiPM.
- Relaxed specifications of analog components. Simpler, lower power and smaller circuits can be used for TIA and comparator.
- The APD capacitance seen at the input of TIA is lower which results in faster response.

A. Transimpedance amplifier

Figure 6 shows the transimpedance amplifier used in each segment. It has a regulated common-gate architecture [5]. This is a PMOS equivalent of the TIA designed in [5]. This is to achieve higher linear gain range for positive input. This TIA is designed to have a gain of 50 kΩ. The TIA is only needed to have a gain range enough to resolve the APDs in one segment. As mentioned in the previous section, the TIA has constant gain for input currents ranging from -25 µA to 40 µA.

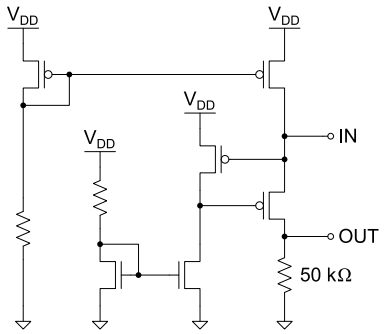

Figure 6: Schematic of regulated common-gate transimpedance amplifier

B. Comparator

The comparator shown in Figure 7 is built using combination of PMOS based and NMOS based self-biased differential amplifiers to achieve rail-to-rail input range [7]. The outputs of both differential amplifiers are tied together and buffered through inverters to resolve the signal levels.

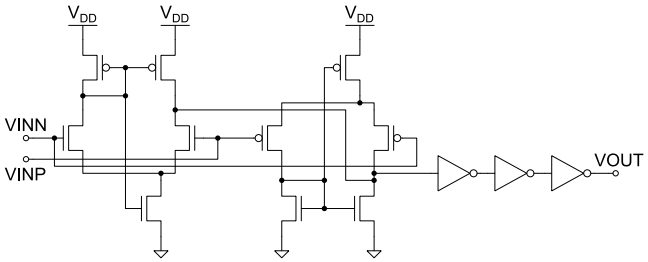

Figure 7: Schematic of comparator

C. Full adder

To implement the full adder, the mirror adder structure is used [8] as seen in Figure 8. This reduces the number of transistors and results in a compact layout.

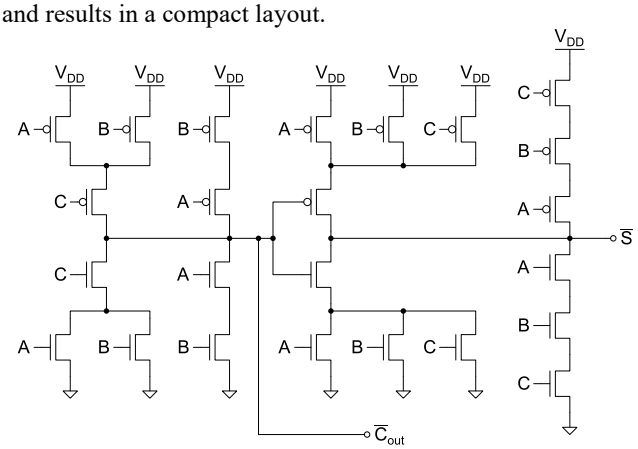

Figure 8: Schematic of full adder

III. Measurement Results

Figure 9 shows the microphotograph of the fabricated chip. The digital SiPM is on the lower left corner. The chip has dimensions of 2mm x 2mm. The digital SiPM has a size of 950um x 400um.

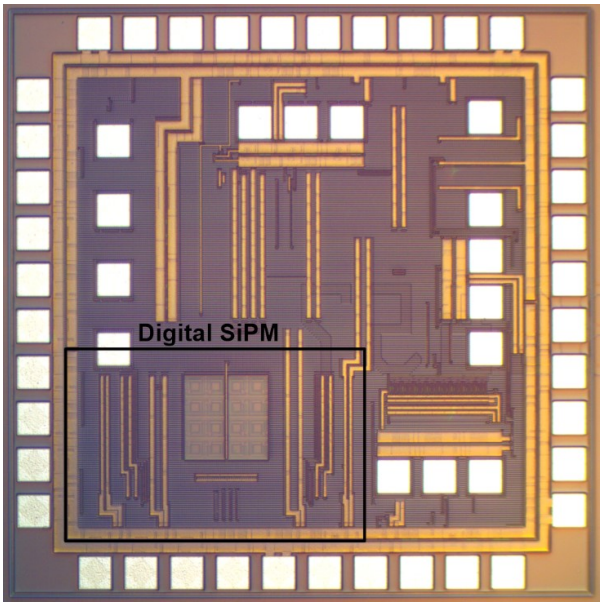

Figure 9: Microphotograph of the fabricated chip

Figure 10 shows the digital SiPM in operation. The setup is as follows. The digital SiPM chip is mounted with an LED inside an opaque enclosure. The LED is driven using a constant current driver set to 5 mA. The LED is turned on using a square wave signal. When the LED is on, the digital SiPM output shows higher count compared to when the LED is off. This can be seen in the oscilloscope screenshot. The digital SiPM clock is derived using the on-chip VCO whose frequency is set to about 60 MHz. This clock is taken off-chip through a divide-by-2 clock divider.

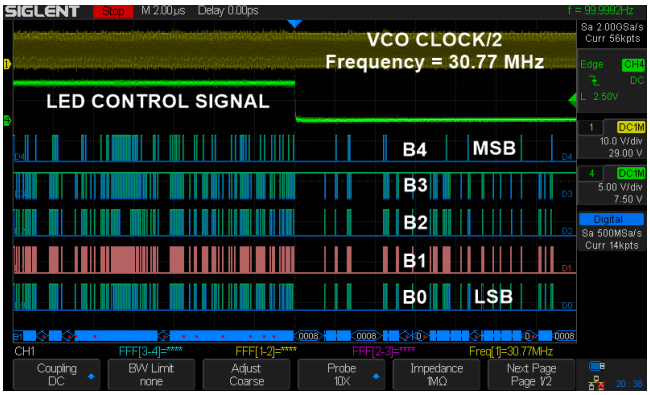

Figure 10. Measured response of the digital SiPM with pulsed LED light stimulus

IV. Conclusion

In this work, a segmented digital SiPM with 4x4 array is presented. The design parameters are summarized in Table 1.

The proposed segmented digital SiPM has advantages of maximum dynamic range output from the SiPM, better fill factor and reduced demand on analog performance. The output of digital SiPM is a 5-bit digital word which can be synchronously read out and processed using an external DSP or FPGA. The dark count of digital SiPM can be optimized in future work by implementing various spatial and temporal compression techniques [4].

Discrete SiPM devices that are tailored for particular wavelength responses can also utilize the segmented digital SiPM architecture if the APD cells are connected as segments and the connections bonded out by the manufacturer.

The current-mode ADC techniques proposed and demonstrated in [2] can be utilized to simplify and reduce the area of the read-out circuitry.

Table 1. Summary of Results

Parameter	Value
Process Technology	AMS 0.35um SiGe BiCMOS
Number of pixels	16
Fill factor	12.6 %
Sampling Frequency	100 MS/s *
Resolution	5-bit
Power	64.6 mW *
Supply voltage	5 V

* Simulated values

Acknowledgment

We are grateful for the support provided by Richard J. Hare and his team at NASA Langley Research Center. This work was supported by NASA under contract number 80NSSC18P2022.

References

[1] T. Frach,G. Prescher, C. Degenhardt, R. de Gruyter,A. Schmitz, and R. Ballizany, “The digital silicon photomultiplier—Principle of operation and intrinsic detector performance,” in IEEE Nucl. Sci. Symp. Conf. Rec., 2009, pp. 1959–1965.

[2] Vikas Vinayaka, Sachin P Namboodiri, Shadden Abdalla, Bryan Kerstetter, Francisco Mata-carlos, Daniel Senda, James Skelly, Angsuman Roy, and R. Jacob Baker, “Monolithic 8x8 SiPM with 4-bit Current-Mode Flash ADC with Tunable Dynamic Range,” to be presented in GLSVLSI ’19: 2019 Great Lakes Symposium on VLSI, May 9-11, 2019, Tysons Corner, VA, USA. ACM, New York, NY, USA

[3] L. H. C. Braga et al., "A Fully Digital 8x16 SiPM Array for PET Applications With Per-Pixel TDCs and Real-Time Energy Output," in IEEE Journal of Solid-State Circuits, vol. 49, no. 1, pp. 301-314, Jan. 2014

[4] S. Mandai and E. Charbon, "Multi-channel digital SiPMs: Concept, analysis and implementation," 2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC), Anaheim, CA, 2012, pp. 1840-1844

[5] M. d. M. Silva and L. B. Oliveira, "Regulated Common-Gate Transimpedance Amplifier Designed to Operate With a Silicon Photo-Multiplier at the Input," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 3, pp. 725-735, March 2014.

[6] Vikas Vinayaka, “Analysis and design of analog front-end circuitry for avalanche photodiodes (APD) and silicon photo-multipliers (SiPM) in time-of-flight applications,” M. S. thesis, Department of Electrical and Computer Engineering, University of Nevada Las Vegas, Las Vegas, NV, 2018. Available: http://cmosedu.com/jbaker/students/theses/Analysis%20and%20Design%20of%20Analog%20Front-End%20Circuitry%20for%20Avalanche%20Photodiodes.pdf

[7] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., John Wiley and Sons, Inc., 2010

[8] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., Addison-Wesley Publishing Company, USA, 2010