Monolithic 8x8 SiPM with 4-bit Current-Mode Flash ADC with Tunable Dynamic Range

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ABSTRACT

A monolithic photon-counting receiver consisting of an integrated silicon-photomultiplier and a current-mode analog-todigital converter (ADC) was designed, simulated and fabricated in the AMS 0.35 μ m SiGe BiCMOS process. The silicon photomultiplier (SiPM) consists of 64 avalanche photodiodes (APD) arranged in an 8x8 pattern with integrated 236 k Ω quenching resistors. This silicon-photomultiplier exhibits peak responsivity at 490 nm and is intended for atmospheric and oceanographic light detection and ranging (LIDAR) applications. The current-mode ADC is used to directly convert photocurrent from the silicon-photomultiplier into a 4-bit word. The maximum sampling rate achieved in simulation is 100 MS/s. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) for the ADC are 0.5 LSB and 0.17 LSB respectively. The dynamic range of the ADC is tunable based on the reference current and varies from 5 μ A – 80 μ A to 30 μ A –

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480 $\mu A.$ The whole system covers an area of 0.375 mm². The fill factor of the silicon photomultiplier is 12.6 %.

CCS CONCEPTS

Hardware~Data conversion • Hardware~On-chip sensors

KEYWORDS

Silicon Photomultiplier (SiPM); Flash ADC; current-mode; analog to digital converter; photosensor; SiGe; avalanche photodiode (APD); bubble correction; tunable dynamic range; LIDAR

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1 INTRODUCTION

Photon-counting has numerous applications such as medical imaging, time of flight (ToF), high energy physics, and LIDAR. The interest in LIDAR has been particularly high due to the advent of autonomous vehicle systems. With much of the focus in automotive applications, other uses for LIDAR have been neglected by the market. One such use of LIDAR is in atmospheric and oceanographic mapping [1]. The wavelengths

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of interest for this application are in the blue-green spectrum, between 460 nm and 532 nm, a band where there is a lack of low cost commercially available components and systems. The vast majority of LIDAR components are in the 1550 nm band for automotive LIDAR. One unique strength of LIDAR in the 460 nm to 532 nm band is that silicon photodetectors can be used which opens the possibility for a fully monolithic optical receiver solution instead of the current discrete component systems available on the market today. We propose a novel SiPM read-out circuitry consisting of a silicon-photomultiplier (SiPM) with a current-mode ADC implemented in a standard 0.35 μ m SiGe BiCMOS process to address the need for low-cost atmospheric and oceanographic LIDAR applications.

An avalanche photodiode APD is a photodetector that is typically used for low-light level detection. It is usually realized by a reversed bias p-n junction. When the reverse bias voltage applied across the APD is in the "knee" of the break down curve, photocurrent gain can be achieved (due to impact ionization and avalanche multiplication). This is the linear mode of operation used in most APD applications. An alternate mode of operation is operating the APD in Geiger-mode, where the device is biased beyond breakdown. In this mode, the output of the APD can either be the dark current level or a saturation current level set by the quenching resistor. A Geiger-mode APD (Gm-APD) can break down due to thermally generated carriers (a dark count) or due to incident light (a light count). The fundamental method of quantifying the light level incident on a Geiger-mode APD is by counting the number of pulses in a certain time interval.

An extension of a Geiger-mode APD is the siliconphotomultiplier, which is an array of Gm-APDs arranged in a grid and connected in parallel. The output from a SiPM is a current pulse whose amplitude is an integer multiple of the current level from a single Gm-APD, with a maximum current level determined by the number of Gm-APDs in the SiPM array. This current output is then typically amplified by a transimpedance amplifier (TIA) and then digitized with an ADC in order to be processed by a digital system. This work offers a current-mode ADC as a solution to directly interface to a SiPM without a TIA, leading to simplicity and robust design.

The design and development of optical receivers for photon counting have recently gained considerable interest [2]. Many designs have been reported in the literature aiming for the development of efficient SiPM read-out circuitry [3,4]. However, most of the designs are mainly focused for biomedical imaging applications such as PET, SPECT, etc. The commonly used SiPM read-out circuits follow the conventional approach of using transimpedance amplifiers to convert the current output from the SiPM to a voltage signal and then digitized by an ADC for further data processing [5]. This has many advantages as well as limitations in terms of dynamic range, bandwidth, power consumption and simplicity. Another technique that has been used is the implementation of "digital SiPM", where the output of each APD is digitized [6]. The main advantage of a digital SiPM is that it can improve the noise of the system. However, the design turns out to be complex and covers more layout area and power consumption.

The SiPM read-out can also be implemented by using the current-mode technique. By using this approach, a high bandwidth as well as a large dynamic range can be achieved compared to voltage-mode topologies. The design in [7] makes use of this approach by incorporating current buffer along with SiPM array. The main challenge with this approach is that the matching of the current source is very critical. The mismatch in the device size can lead to degradation in the overall performance of the whole read-out circuit.

In this paper, we present a novel fully integrated SiPM readout system using a 4-bit current-mode ADC implemented in AMS' SiGe $0.35 \,\mu$ m technology fabricated through the MOSIS service. The sensor (SiPM) is comprised of an 8x8 array of APDs. Since the output of the SiPM is a current signal, it will be directly fed into a current-mode ADC and thus bypassing a transimpedence amplifier and other circuitry that are conventionally used for an SiPM read-out. The ADC also offers the freedom of tuning the dynamic range and thereby can accommodate for different SiPM bias voltages. Section 2 of this paper discusses the overall system architecture. Section 3 reports the experimental setup and the measured results. Section 4 concludes the paper along with the scope for future work.

2 SYSTEM DESCRIPTION

Figure 1 shows the overall block diagram of the SiPM read-out circuit. It consists of the SiPM coupled with the current-mode 4bit ADC. The SiPM outputs a current signal whose amplitude depends on the number of APDs triggered. This output current is then fed to the 4-bit current-mode ADC which produces a digital output. The SiPM and current-mode Flash ADC blocks are described in the subsequent sections. The output of ADC is available off-chip for further data processing using a DSP or FPGA.



Figure 1: System architecture.

2.1 SiPM array

The SiPM is a photosensor whose output is a current whose value can be a set of discrete amplitude levels. The SiPM consists of an array of avalanche photodiodes (APDs) that are connected in parallel. Figure 2 shows the internal schematic of the SiPM and its equivalent electrical model. The anode of all the APDs are connected, ensuring the summation of each APD current output. The APDs are operating in Geiger-mode, which requires a

quenching resistor, R_{quench} placed in series as seen in the figure. All APDs are pre-charged above the breakdown voltage with a high voltage (HV) supply, typically 11V-15V. A single cell of the array showing a serpentine quench resistor wrapped around the APD is displayed in Figure 3. The layout of the 8x8 SiPM array in the AMS' 0.35 µm SiGe process is illustrated in Figure 4.



Figure 2: Circuit and simple electrical model of SiPM.

The main benefit of a SiPM as compared to a single APD is that it can detect multiple photons at the same time [8]. The significance of this is that the SiPM has a higher count rate and dynamic range than other photon-counting detectors.



Figure 3: Single APD cell of SiPM

The SiPM array needs a bias voltage higher than its breakdown voltage which is much higher than the supply voltage (VDD) of other circuits on the chip. In this fabrication process, the APDs have a breakdown voltage of about 12 V whereas VDD is 5 V. When the SiPM is connected to the ADC, the ADC input has a bias voltage which reduces the voltage across the SiPM. As a result, the SiPM bias voltage must be offset by the average value of the voltage on the ADC input. The voltage on the input of the ADC is discussed in the next section.



Figure 4: Layout of SiPM consisting of 8x8 array of APDs

2.2 Current-mode Flash ADC

The output of the SiPM is connected to the input of the currentmode Flash ADC. The ADC converts the incoming current to a 4-bit digital value. The output of the ADC is asynchronous and can be retimed using an off-chip clock if needed. Figure 5 shows the circuit of the 4-bit current-mode Flash ADC implemented in this work.



Figure 5: Schematic of 4-bit current-mode Flash ADC

The ADC mainly consists of current comparators, gain inverters and thermometer to binary encoder blocks.

In the Figure 5, the current comparator is seen on the top. It has the input current, I_{IN} input on the left side and the reference current, I_{REF} on the right side. The current comparator consists of PMOS current sources and NMOS current sinks in series. The current comparator operates as follows: The voltage at the junction point of the current source/sink (the drains of the PMOS/NMOS) is dependent on the current flow through the devices. If the current source value is higher than the current sink value, the voltage at the junction point is pulled up to VDD. Conversely, if the current sink value is higher than the current source value, the voltage at the junction point is pulled to ground. This is the mechanism of current comparison. The PMOS current sources are mirrored from the input current. The NMOS current sinks are scaled and mirrored from the reference current. The PMOS current is compared against each multiple of the reference current corresponding to all the ADC steps. The output of the current comparator array is a thermometer code.

The speed of the current comparator is limited by the current available to drive the gain inverters. The most significant current limitation occurs during conditions where the current source and current sink values are similar. This limitation can also be viewed as occurring near regions where the output code would transition to the next value.

The current comparator mainly relies on matching between the current mirror devices for proper operation. The device lengths are chosen to be four times the minimum length of CMOS devices in the fabrication process. This ensures good matching and increases the output resistance of the devices, which results in better gain and resolution of each ADC step. The length could be increased further to improve resolution, however there is a tradeoff of speed because of increased capacitance of all the devices. Also, increase in length for matching produces diminishing returns after a point where random mismatch and threshold voltage mismatch dominate [9].

Since the current comparators compare the input current against multiples of reference currents, changing the reference current changes the ADC steps and results in a tunable dynamic range. The allowable range of reference currents are limited by the device matching and the saturation current of the devices. In this design, the reference current can be varied from 5 μ A to 30 μ A which results in a minimum dynamic range of 5 μ A – 80 μ A up to a maximum 30 μ A – 480 μ A respectively.

The output of current comparators might not be resolved to logic levels if the difference between source and sink current values are too low. The gain inverters amplify the output of current comparators to standard logic levels.

The output of the gain inverters is a thermometer code of 16 levels. This is converted to 4-bit binary using a digital encoder. The schematic of the encoder is seen in Figure 6.

The thermometer to binary encoder consists of AND gates that convert the thermometer code to one-hot code. The one-hot code is converted to binary using the binary encoded ROM pattern. This generates the 4-bit binary output which is buffered and sent out off-chip.



Figure 6: Schematic of thermometer to binary encoder

The thermometer code from the comparator output is prone to errors (bubble) that must be addressed while designing the encoder. This is usually caused by metastability of the comparator. The 3-input AND gate eliminates bubble errors [10]. If a spurious 0 is present in a string of 1's or a spurious 1 in a string 0's, it will be corrected at the output of the AND gate. The scheme used here can only correct a single isolated spurious code. If there are two or more spurious 0's or 1's in a string of complementary bits, more advanced schemes would be needed to correct it.

The simulation results of the Flash ADC are seen in Figure 7. This shows a triangle wave input current and the corresponding analog representation of the digital output on the top part of the figure. The 4-bit digital output is seen on the lower part of the figure where the MSB, B_3 is on the bottom.



Figure 7: Simulated operation of the ADC

Complete layout of the Flash ADC is seen in Figure 8. The current inputs are on the left edge and the digital 4-bit outputs are on the bottom-right corner.



Figure 8: Physical layout of ADC

2.3 SiPM and Flash ADC

The input of the Flash ADC is a gate-drain connected NMOS as seen in Figure 5. As a result, an increase in input current also causes an increase in input voltage. This characteristic is seen in Figure 9 where the x-axis is the input current and the y-axis is the voltage on the input.



Figure 9: I-V characteristics of ADC input

Since the anode of the SiPM is connected to the ADC input, the voltage across the SiPM is the difference between the SiPM high-voltage bias applied to the SiPM cathode and the voltage on the input of the ADC. The SiPM bias voltage must be increased to compensate for the increase in ADC input voltage. This has a side effect that a higher bias voltage appears across the SiPM for lower currents and vice versa.

The variation in input voltage due to input current could be decreased by increasing the device widths used. However, this would put stricter requirements on the device matching due to reduced gate to source voltages. As a result, there is a trade-off between input offset voltage reduction and improved device matching.

3 MEASUREMENT RESULTS

The micrograph of the fabricated chip is seen in Figure 10. The chip has dimensions of 2 mm x 2 mm. As annotated in the figure, the SiPM array is at the center of the chip and the ADC is on the top-right corner of the chip. The output of SiPM is connected to the input of ADC using internal pad to pad bond wires. This was done to facilitate ease of testing; in future designs the SiPM and ADC can be directly connected with on-chip metal layers.

The test setup is implemented as follows: The chip is bonded on a TO-8 package and mounted on a PCB. The TO-8 package without a lid is inserted into one end of a copper tube. An LED driven by a constant current source is mounted on the other end of the copper tube. This results in a dark condition for the chip when the LED is off. The LED is activated using a square wave signal and the resulting digital output change is observed using a logic analyzer.



Figure 10: Chip photomicrograph

The measured output is seen in Figure 11. The LED control signal is seen on the top and the 4-bit digital output is seen on the bottom part of the oscilloscope capture image. The LED turns on when the LED control signal is high. The digital outputs

increase when the LED is on. Since the SiPM generates pulses with pseudo-analog levels which are proportional to the amount of light incident on it, this results in the pulses seen on the output of the ADC. In this plot, the ADC reference current is 10 μ A and SiPM bias voltage is 13 V.

The measured current-mode ADC transfer characteristics are seen in Figure 12. In this plot, the x-axis is the input current and the y-axis is the output digital code. This measurement is with the standalone ADC excluding the SiPM. The input current and reference current were directly applied to the ADC input using a sourcemeter to measure the characteristics. These characteristics are measured with a reference current of 10 μ A.



Figure 11: Measured response of the system



Figure 12: ADC static transfer characteristics



Figure 13: Measured DNL



Figure 14: Measured INL

The differential non-linearity (DNL) and integral non-linearity (INL) are derived from the transfer characteristics and seen in Figure 13 and Figure 14. Observing these characteristics, we see that the maximum DNL is 0.5 LSB and maximum INL is 0.17 LSB. The ADC also has a gain error of 13.18 μ A/bit and offset error of 26.1 μ A. The ADC I-V input characteristics are measured and seen in Figure 15. The voltage on the ADC input varies from about 0.8 V to 3.3 V for an input current change from 1 μ A to 500 μ A. The SiPM bias voltage needs to be increased correspondingly in order to apply the required breakdown voltage across the SiPM.



Figure 15: Measured characteristics of ADC input

	This work	[11]
Technology	AMS 0.35um SiGe	90nm CMOS
Supply voltage	5 V	1.2 V
Resolution	4-bit	3-bit
DNL/INL	0.5 LSB / 0.17 LSB	0.24 LSB / 0.24 LSB
Dynamic range	30 µA – 480 µA	Not reported
Sampling rate	100 MS/s *	2 GS/s
Power	14.3 mW *	3.1 mW

Table 1: Comparison of current-mode ADC

* Simulated value

4 CONCLUSION

In this work, an 8x8 SiPM is interfaced with a current-mode 4-bit Flash ADC. Both blocks reside on the same monolithic chip which results in an integrated system which is novel in this work. The whole system occupies an area of 0.375 mm² on the die. The current-mode ADC standalone results are summarized and compared with similar work [11] in Table 1. The ADC has DNL, INL, gain error and offset errors which are caused by device mismatch due to process variations. The read-out operation of the SiPM and ADC has been demonstrated. This work can be extended by developing a complete photodetection system which would need an on-chip digital signal processing depending on the appropriate application. The proposed monolithic photon counting system combining a SiPM with a current-mode ADC can significantly reduce the cost of LIDAR systems for atmospheric and oceanographic applications.

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