Variable Fast Transient Digitizer

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Abstract

A low cost, low power substitute for expensive, high power high-speed analog-to-digital converters (ADCs) in some situations is presented. This circuit is called a variable fast transient digitizer (VFTD). The VFTD is designed to sample a high-speed analog input signal and later reconstruct the captured signal at a much slower rate. This approach eliminates quantization error in the captured signal. Further, this approach enables the use of slow, low cost, analog-to-digital converters such as those found in microcontrollers. The VFTD uses 256 sequential sample and hold cells with a process dependent variable delay element controlled by an off-chip voltage source. Using a power supply voltage of 5V the input range extends from 0 V to 3 V corresponding to an output voltage range from 2 V to 5 V, a capture window range from 81 ns to 1.78 μs, and a sampling rate range from 143.82 MS/s to 3.16 GS/s. The VFTD is fabricated on a 2 mm x 2 mm die using ON Semiconductor's 0.5 µm C5 process and requires a 0.5 mm x 1.5 mm area.

Motivation

As circuits and components in modern electronics continue to decrease in size and subsequently increase in speed, the need to develop inexpensive, fast and efficient methods to capture and process information increases. Specifically, the ability to capture transient and high-speed analog signals is a common goal shared in a multitude of fields. Most of the implementations that deal with such signals use high-speed analog-to-digital converters (ADCs), and various other filters that tend to be bulky, expensive, power hungry, or have very specific operating frequencies. The VFTD is developed to efficiently capture high-speed analog signals and later reproduce a slowed or stretched version with minimal error.

System Architecture and Innovations

Conventional FTD

The Conventional FTD consists of 3 modules:
- Two basic inverters acting as a delay line
- A capture stage, implemented using an NMOS switch and a hold capacitor
- A readout stage, implemented using a PMOS source follower and an NMOS switch

FTD Operation

Sampling Process
- The “Trig_in” signal, transitioning from high to low, propagates through the delay line and samples the Analog_in value to the hold capacitor.
- Simultaneously, “Trig_out” then propagates to the input of the delay element in the next sequential capture stage and the process repeats itself for all 256 stages

Readout Process
- The value stored in the hold capacitor, is level shifted using a PMOS source follower.
- The level shifted output is then readout using an NMOS readout switch
- The readout switch is activated using an 8:256 decoder.

Design considerations
- The capacitor value is selected based upon the thermal noise and settling time constraints
- The NMOS sampling switch is sized accordingly to minimize the distortions

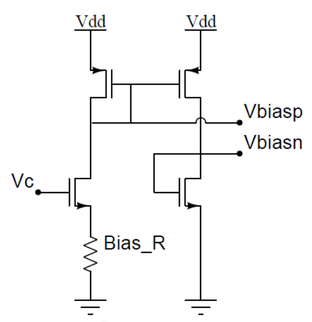
Drawback: The FTD has a fixed capture length that limits the number of applications that can use the FTD

Proposed Architecture

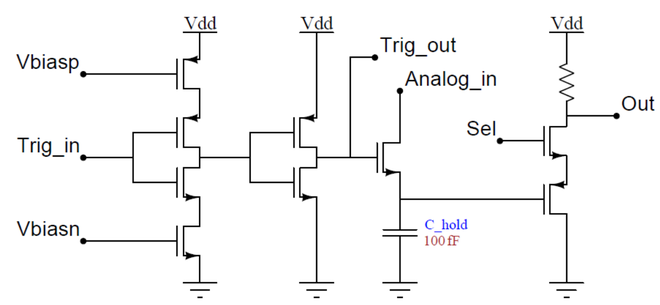
Circuit implementation

The VFTD aims to address the need for a variable sampling rate by redesigning the FTD capture stage

The variable sampling rate is achieved by the inclusion of a current starved inverter at the delay line
- The bias voltages for the current starved inverters are generated using an on-chip bias generator.
- The bias generator design includes an NMOS device controlled by an off-chip control voltage (Vc) and an off-chip bias resistor (Bias_R)
- This provides two degrees of control and results in a voltage controlled current that is process, voltage and temperature invariant.



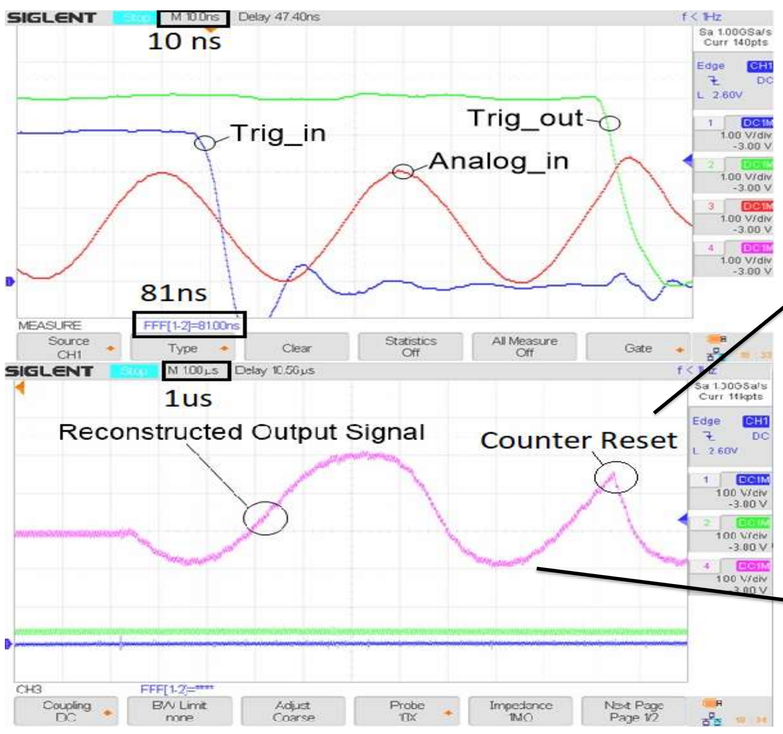
Biasing circuit



Proposed architecture

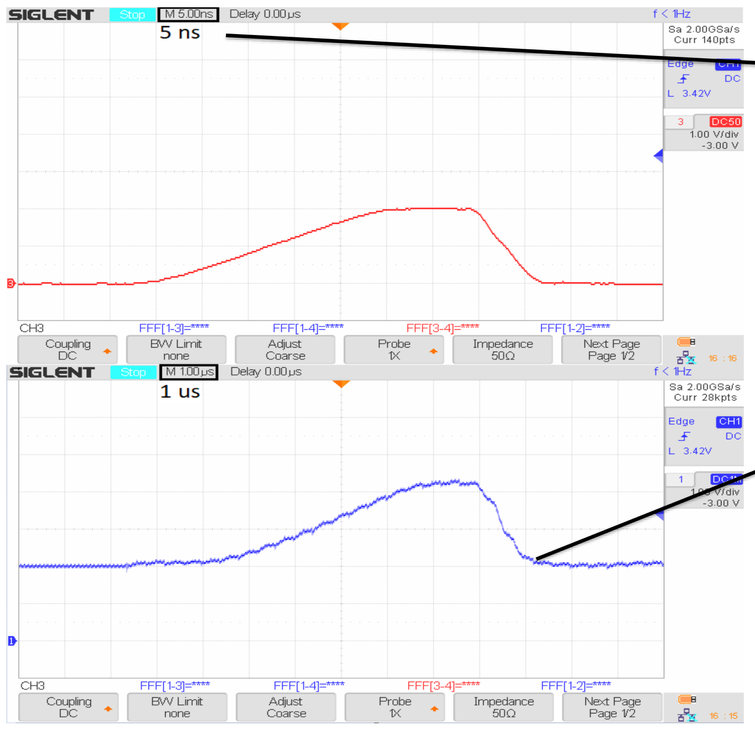
The VFTD design allows for an equivalent, variable time delay throughout the 256 sequential capture stages that can be adjusted for application specific needs.

Experimental Results



The discontinuity in the reconstruction is due to the reset of the off-chip counter

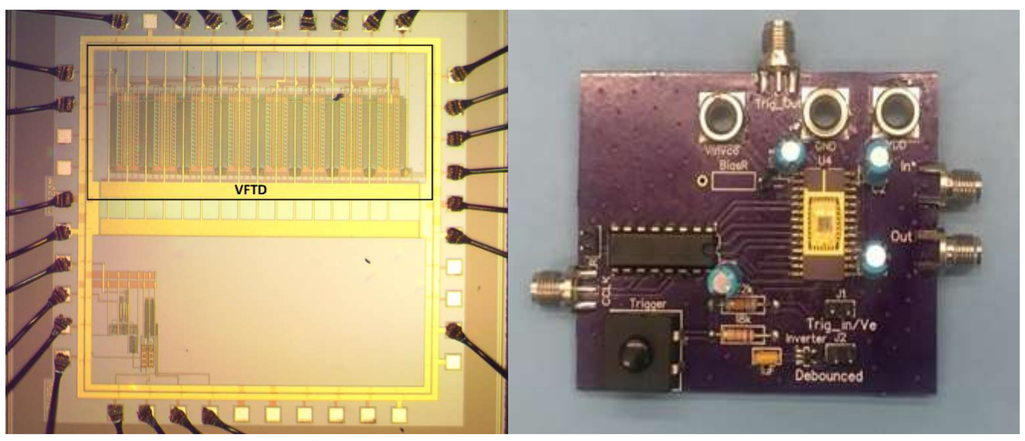
The VFTD effectively captured 1.5 cycles of a 20 MHz sinusoid and reconstructed it as a 150kHz



The time scale division is set to 5ns with a total capture window of 70ns

The reconstructed signal is seen with a 1us time scale division for a 14 us reconstruction window.

Test results for a slow ramp and a sinusoidal input.



Chip photomicrograph and test board

Chip performance summary

Vc	Bias_R	Capture Window Experimental	Sampling Frequency Experimental
5 V	2 kΩ	81.00 ns	3.16 GS/s
1 V	2 kΩ	384.00 ns	666.67 MS/s
1 V	4 kΩ	542.00 ns	472.32 MS/s
1.5 V	57 kΩ	1.78 µs	143.82 MS/s

Parameter	VFTD	FTD
Technology	500nm	500nm
Number of Capture stages	256	128
Layout area	.73mm^2	.49mm^2
Measured Capture window	81ns-1.78µs	31.4ns
Sampling frequency	143.82MS/s-3.16GS/s	4.08GS/s

Future work
- Incorporation of interleaving technique for higher sampling rates
- Developing a wide-swing FTD to extend input and output signal range

References

[1] B. Gosselin and M. Sawan, "Adaptive detection of action potentials using ultra low-power CMOS circuits," *2008 IEEE Biomedical Circuits and Systems Conference*, Baltimore, MD, 2008, pp. 209-212.

[2] K. Buck and R. J. Baker, "Fast Transient Digitizer Chip for Capturing Single-Shot Events," in 12th IEEE Dallas Circuits and Systems Conference, Dallas, 2016.