Analog Integr Circ Sig Process
DOI 10.1007/s10470-017-1062-8

Design and analysis of a feedback time difference amplifier with linear and programmable gain

Wenlan Wu[1,2] · R. Jacob Baker[1] · Phaneendra Bikkina[2] · Yu Long[2] · Andrew Levy[2] · Esko Mikkola[2]

Received: 5 May 2017 / Revised: 5 October 2017 / Accepted: 9 October 2017

Abstract This paper proposes a feedback time difference amplifier (FTDA) that achieves linear, controllable gain and changeable input range for different time difference gains. The proposed FTDA consists of two identical feedback output generators. The feedback output generator achieves a linear input–output transfer characteristic by employing two p-type keepers for time gain feedback control. Its validity was demonstrated using 0.13 µm SiGe BiCMOS process. The power consumption is 91.54 µW for the highest gain with input signals at 2 MHz. The gain can be controlled from 25.06 to 734.9 s/s within 40 ps input time interval.

Keywords Time amplification · Feedback technique · Time difference amplifier · Programmable gain · Linearity · Gain control · Time-to-digital converter

1 Introduction

As complementary metal-oxide-semiconductor (CMOS) technologies advance to below 10 nm dimensions, design of analog and mixed-signal circuits is becoming more challenging because of decreasing intrinsic gain, increasing leakage current, and reducing signal power. However, the desire for smaller area, higher density of integration, and faster switching speed keeps pushing process dimensions smaller and smaller. Time-mode processing technique is capable of solving many of these challenges [1].

The time-to-digital converter (TDC), as a front-end block, plays a significant role in time-mode signal processing. As transistor size scales down, leading to smaller gate delays, a TDC is an effective way to digitize a small-time difference between two rising edges. TDCs have been widely used in a variety of applications [2–4], such as Time-of-Flight (ToF) and lifetime measurements in high energy physics, jitter measurement in the testing of integrated circuits and high-speed data transfer, and all-digital phase-locked loop (ADPLL). There are two traditional methods achieving fully digital TDCs: counter-based and delay-line-based. A counter-based TDC is the simpler technique to quantize the input time interval by counting the cycles of a reference clock fitting into the time range. However, a faster clock is required to get a higher time resolution. This causes the power consumed by the clock generation and processing circuitry to increase.

The delay-line based TDC, also called the inverter-based TDC, is implemented by a chain of delay buffers such that its resolution is ultimately constrained by the propagation delay of each single inverter, as shown in Fig. 1. However, the resolution of one inverter is insufficient to reach 1 ps resolution. Furthermore, a longer delay line is required for a wide input range. Because of this, researchers are focusing on realizing the sub-gate delay resolution by introducing various methods including: Vernier delay line, pulse-shrinking, interpolation and a delay line with local passive interpolation. Nevertheless, 1 ps resolution with small area and simple processing has not been realized through any of these implementation methods.

✉ Wenlan Wu
wuw2@unlv.nevada.edu

Esko Mikkola
esko.mikkola@alphacoreinc.com

[1] Department of Electrical and Computer Engineering, University of Nevada, Las Vegas, Las Vegas, NV, USA

[2] Alphacore Inc., Tempe, AZ, USA

Published online: 16 October 2017

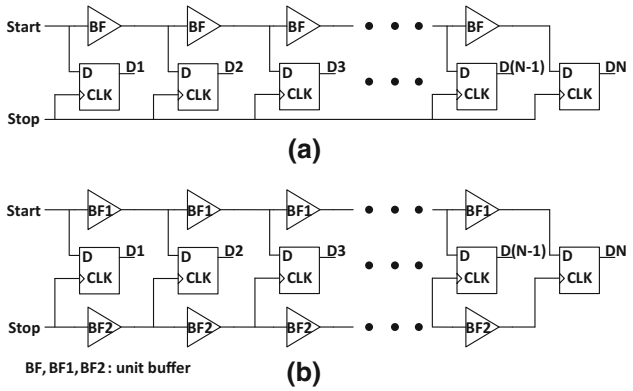


Fig. 1 **a** Delay-line-based TDC, **b** vernier delay line

Fortunately, TDCs are similar in concept to analog-to-digital converters (ADCs) and the wealth of ADC design experience provides insight into resolving the above issues. A two-step ADC improves resolution by amplifying the residue between the input and the closest coarse level, then quantizing the amplified residue again with the same coarse quantizer. This is the basic principle of time amplification. Time difference amplifiers (TDAs) thus become an integral method for improving the time resolution of TDCs as well as making a better coarse-fine TDC with a satisfactory trade-off between input dynamic range and time resolution.

The first time difference amplifier was introduced in [5], and consisted of two output generators (which is also called a mutual exclusive circuit, MUTEX) comprising one SR-latch followed by an XOR gate, shown in Fig. 2(a). Both MUTEXs have two shared inputs and one output. The time difference between rising edges of two inputs and outputs are defined as the TDA's input and output signals, respectively. The traditional TDA leverages the meta-stability of an SR-latch and positive feedback to achieve the principle of time amplification. The output delay in each output generator is a logarithmic function of the time difference between the two input clock edges. Each output is eventually forced to a logic level by the positive feedback from each latch. However, when the time interval between rising edges of the two inputs becomes smaller, the response time of the SR-latch become longer, causing a non-linearity issue related to the time difference gain.

State-of-the-art TDAs described over the past decade have implemented time amplification in different ways. Reference [6] presented an improved MUTEX by adding a time delay T_{td} to one of the two inputs in an SR-latch as shown in Fig. 2(b). The input–output characteristics of two mirrored MUTEXs are shifted by the same amount of offset delay in opposite directions, resulting in a T_{td} linear range. Unfortunately, the linearity of the input range is limited by the time delay.

A topology presented by [7, 8] uses a calibration technique to correct the non-linearity issue. The core of the TDA consists of two cross-coupled buffer chains whose delays are adjusted by a delay-lock loop (DLL)-based feedback loop, as shown in Fig. 3. The propagation delay of one buffer cell needs to be four times larger than the other buffer cell. Although this closed-loop TDA provides relatively stable gain against process, voltage, temperature (PVT) variation, the number of buffers in the TDA core needs to be increased linearly with the TD gain, causing higher power consumption and increased circuit complexity. For example, a TDA with gain of A requires a calibration loop with 6A inverters. Therefore, this topology is not a practical solution for high gain such as 100 or above.

In addition, other proposed open-loop structures use analog or digital methods. The analog method [9, 10] is to toggle between the outputs of two comparators that present the TDA output. The inputs to the comparators are voltages on different capacitors and their voltage difference comes from charging or discharging capacitors with a time delay. However, mismatches between delay elements, charging or discharging currents and comparators can influence the TDA linearity. A digital method in [11] is to multiply N times the unit pulse-width to achieve a wide pulse. The pulse-train TDA includes a buffer chain and one OR gate. However, the gain is limited by the number of buffers so achieving high gain increases the chip area and power consumption.

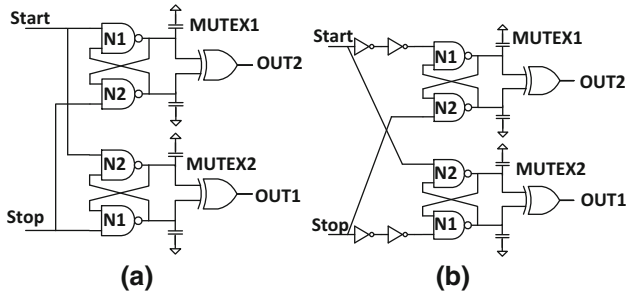


Fig. 2 **a** Traditional TDA [5], **b** inverter delay based TDA [6]

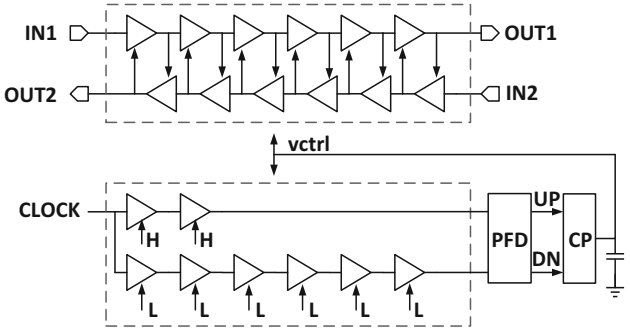


Fig. 3 Closed loop TDA with DLL-based calibration [7, 8]

In this paper, a feedback TDA with closed-loop structure is proposed to use simple circuitry for achieving highly linear time difference (TD) gain.

This paper organization is: Sect. 2 describes the traditional MUTEX; Sect. 3 presents the operation of a feedback keeper used in the digital portion of the circuit; the feedback output generator and feedback TDA are proposed in Sects. 4 and 5, respectively; the non-idealities analysis and simulation results are presented in Sect. 6; and conclusions are in Sect. 7.

2 Traditional output generator

The traditional output generator is a structure composed of one latch and one XOR gate, as shown in Fig. 4(a). The waveforms at each node are depicted in Fig. 4(b), whereby two clock signals with a time interval are applied to S and R of the latch, respectively. The positive feedback in the SR-latch forces S0 and R0 nodes to a digital level of one or zero. In general, the regeneration time of the output and input time difference has a relationship [6] which can be expressed as:

$$\Delta T_{out} = \tau * (\log(V_{TH}) - \log|\alpha * \Delta T_{SR}|) \quad (1)$$

where α is a proportional factor, $\tau = \frac{C}{g_m}$ is the regeneration time constant, C is the node capacitance including output capacitance of the NAND gate plus input capacitance of the XOR gate, g_m is the transconductance of the NAND gate when it is in metastable condition, and V_{TH} is the threshold voltage of the XOR gate. ΔT_{out} is a logarithmic function of ΔT_{SR} as shown in Fig. 5.

The traditional TDA can be optimized by using two MUTEXs with offset delays [5, 6]. The final output is defined as the subtraction between outputs of two MUTEXs, which can be derived using (2) in the range of $-T_{td} < T_{in} < T_{td}$. The final TD gain is shown in (3) that relates to the time delay, T_{td}.

$$T_{out} = \tau * (\log(T_{td} + T_{in}) - \log(T_{td} - T_{in})) \quad (2)$$

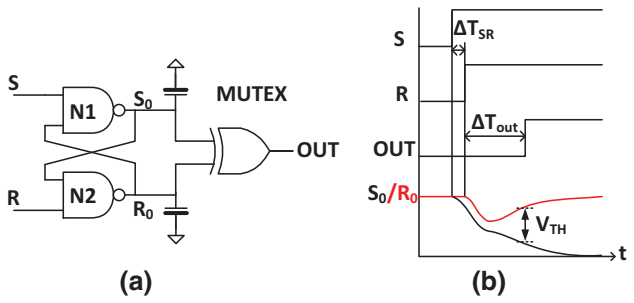


Fig. 4 Traditional MUTEX with waveforms at each node

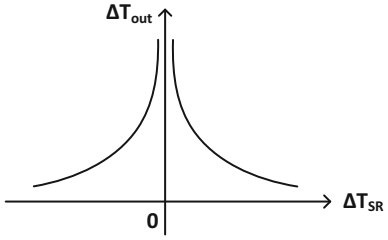


Fig. 5 Output regeneration time of MUTEX versus time difference between two inputs of the S-R latch

$$G = \frac{2C}{g_m T_{td}} \quad (3)$$

3 Feedback technique in digital circuit

The feedback technique used in the digital circuit was discussed in [12]. In the precharge-evaluation (PE) logic, also known as dynamic logic or clocked logic, a "keeper" PMOS device was used for feedback to eliminate the leakage issue existing in the inverter-output based PE gate.

As shown in Fig. 6, during the precharge phase, the PE output node A is pre-charged to V_{DD}. If the NMOS logic results in a logic high on node A during the evaluation phase then node A is at a high impedance with no direct path to V_{DD} or ground. The result is charge leakage from node A when the PE output is a logic high. A feedback "keeper" device can be added to help keep node A at V_{DD} when the NMOS logic is off.

4 Feedback output generator

Based on the above discussion, a novel feedback output generator (FOG) is proposed with functionality like the traditional one in [5]. In contrast, however, the feedback technique in FOG increases the output regeneration time, which is realized by adding one buffer and two feedback keepers between the SR-latch and the XOR gate.

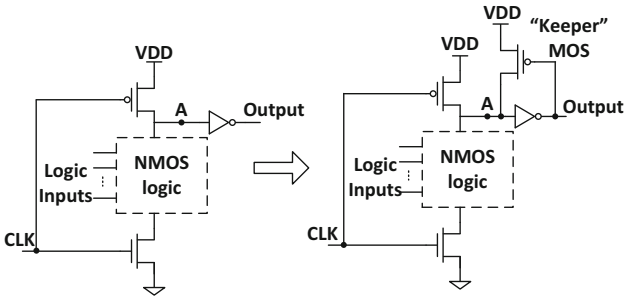


Fig. 6 Feedback keeper used in dynamic logic circuit

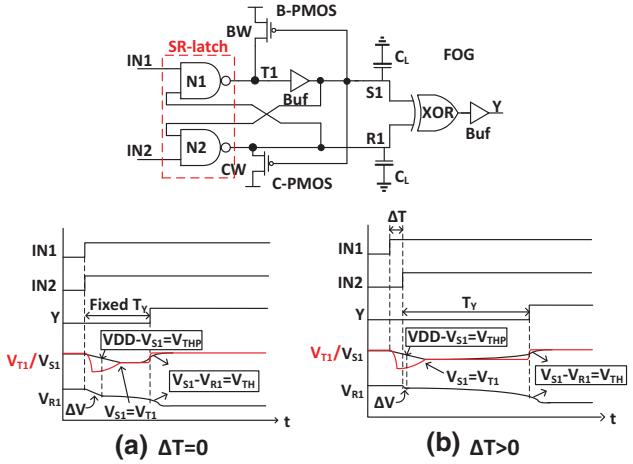


Fig. 7 Proposed FOG with two timing diagrams

The proposed FOG, shown in Fig. 7, includes one latch, two buffers, one XOR gate and two "keeper" devices (B-PMOS and C-PMOS). One buffer is used in the middle path between the latch and XOR gate. The other one is used to improve the drive capability of the output node. Gates of both B-PMOS and C-PMOS are connected to the same node S1. Two clock signals are given to IN1 and IN2, and the time difference T_{in} between their rising edges is regarded as the FTDA's input. If IN1 is assumed to rise to V_{DD} earlier than IN2, T_{in} is regarded as positive. Otherwise, T_{in} is regarded as negative.

Figure 7 depicts the operation of the proposed FOG with four steps when applying an input time interval. Initially, IN1 and IN2 stay at ground making the voltages at S1, T1 and R1 equal to V_{DD} so that feedback keepers are turned off. In the following discussion, for example, assume T_{in} is positive and IN1 rises to V_{DD} at $t0$.

First, V_{T1} is quickly pulled down to *Gnd* with a small NAND propagation delay when IN1 rises to V_{DD}. V_{S1} is also decreasing but slower than V_{T1} because of the delay effect caused by extra buffer and large parasitic capacitance at node S1. V_{R1} remains unchanged at V_{DD}.

Second, at the time $t1$ B-PMOS and C-PMOS are turned on. Before IN2 rises to V_{DD}, V_{S1} decreases until equal to $V_{DD} - |V_{THP}|$, which turned on two feedback "keepers". Meanwhile, V_{T1} is pulled up by turning-on B-PMOS.

The status of V_{R1} depends on the rising edge of IN2. If IN2 rises before $t1$, V_{R1} gets a ΔV reduction before C-PMOS is turned on. Otherwise, if IN2 rises after $t1$, V_{R1} stays at V_{DD}. Comparing the timing diagrams in Fig. 7(a), (b), the smaller T_{in} becomes, the larger the ΔV. The rising edge of IN2 causes the discharging of V_{R1}. For a larger ΔV the capacitor will be discharged more quickly, otherwise, the discharge time can be longer. Hence, output regeneration time is negatively proportional to $|\Delta V|$.

Third, the feedback process happens when the B-PMOS device becomes diode-connected, which means gate voltage V_{S1} is equal to drain voltage V_{T1}. At this step, both IN1 and IN2 stay at V_{DD}.

The two models in Fig. 8 describe the feedback operation. Since $V_{IN1} = V_{IN2} = V_{DD}$, the discharging currents flowing through NMOSs of NAND gates, I_{N1} and I_{N2}, are controlled by V_{R1} and V_{S1}, respectively. The current flowing through B-PMOS and C-PMOS and I_{P2} are determined by the gate voltage V_{S1}.

The B-PMOS device is sized to balance the currents ($I_{BP} = I_{N1}$) to keep V_{T1} equal to V_{S1}. The C-PMOS device is sized to make I_{CP} smaller than I_{P2} plus I_{N2} for slowly discharging the capacitor at the R1 node. A different width for C-PMOS would results in a different I_{CP} drain current, which means the size of C-PMOS can be used to control the reduction speed of V_{R1}. The decreasing V_{R1} is feedback to one input of N1-NAND gate. Before V_{R1} turns on the PMOS in N1-NAND gate, $V_{S1} = V_{T1}$ makes V_{R1} continue to decrease. When V_{R1} turns on the PMOS, the current balanced in N1-NAND is broken and V_{S1} begins to be pulled up to V_{DD}. The increasing V_{S1} is feedback to one input of N2-NAND gate; decreasing I_{CP} continues to reduce V_{R1}. Without feedback keepers like transition SR-latch, S1 and R1 can be quickly forced to V_{DD} or *Gnd*. Therefore, the feedback technique is used to expand the time of the 3rd step, and the reduction speed of V_{R1} is controlled by current difference, I_C.

$$I_C = I_{CP} + I_{P2} - I_{N2} \tag{4}$$

The control of output regeneration time is thus achi-eved. A wider C-PMOS device with a larger drain current decreases the discharge current I_C and increases the output regeneration time. A small C-PMOS device with a smaller drain current would have a larger output regeneration time.

The size of C-PMOS controls the reduction speed of V_{R1}. A properly-sized buffer inserted between the B-PMOS gate and drain is used to maintain the V_{R1} reduction condition. If the buffer has less delay, the faster-decreasing V_{S1} pulls V_{R1} up, so the third step will not happen. Otherwise,

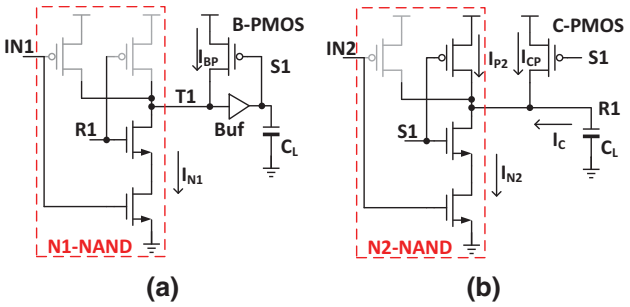


Fig. 8 **a** Current balance model, **b** capacitor discharging model

the slowly-decreasing V_{S1} speeds up V_{R1} reduction and shortens the output regeneration time.

In addition, for a larger T_{in}, the V_{R1} reduction curve becomes longer. The input time interval is positively proportional to the beginning value of V_{R1} when both keepers are turned on. The discharging time of a capacitor is calculated based on (5), (6). It is reasonable to achieve positive time amplification by making the $\frac{C}{I_C}$ greater than one.

$$V_{R1} \propto T_{in}, \quad I_C * \Delta t = C * (V_{R1} - 0) = C * V_{R1} \tag{5}$$

$$\Delta t = \frac{C}{I_C} * V_{R1} \propto \frac{C}{I_C} * T_{in} \tag{6}$$

The final step is logic-level generation. As V_{R1} continues to decrease, the difference between V_{S1} and V_{R1} is equal to the threshold voltage of the XOR gate causing the XOR gates output Y toggle to V_{DD}.

In this context, the output generation time T_Y, which is the difference between the rising edge of output and the later rising edge of the two input signals, is amplified and controlled by feedback P-type keepers.

A special case happens at $T_{in} = 0$ when the rising edges of IN1 and IN2 occur at the same time. The FOG still goes through four steps and the feedback technique slows down the V_{S1} and V_{R1} reduction speed to make the output regeneration time a constant value $T_Y(0)$ as shown in Fig. 7(a).

5 Proposed feedback time difference amplifier

The principle of the proposed FTDA is illustrated in Fig. 9(a), where IN1 and IN2 represent the inputs and Y1 and Y2 represent the outputs. The input time interval is the time difference between the rising edges of IN1 and IN2.

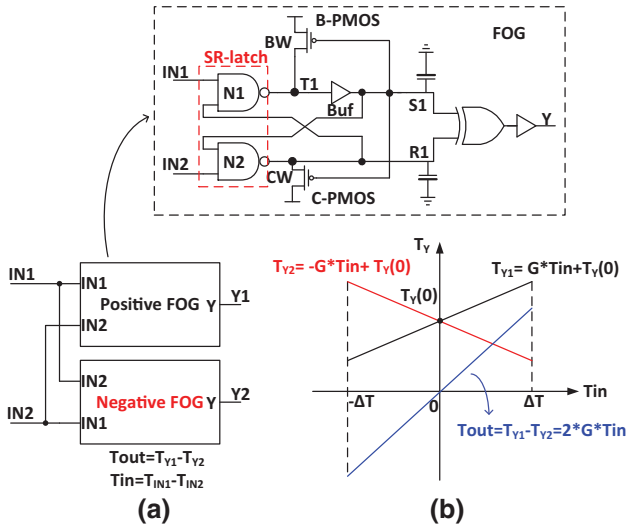


Fig. 9 Proposed FTDA with input–output transfer characteristic

The output time interval is time difference between the rising edges of Y1 and Y2.

5.1 Circuit implementation

At circuit level, the FTDA is composed of two identical FOGs. Each FOG has two inputs and one output. Cross-connected inputs realize opposite input time differences for the FOGs. For example, if IN1 rises earlier than IN2, the upside FOG has a positive input but the downside FOG has a negative one.

Based on the discussion in Sect. 4, either FOG can achieve a linear input–output transfer characteristic and cross the same Y-axis point ($T_Y(0)$), depicted in Fig. 9(b). However, their characteristic slopes are opposite because of reversed input signals.

The regeneration time of T_{Y1} and T_{Y2} can be written as

$$T_{Y1} = G * T_{in} + T_Y(0) \tag{7}$$

$$T_{Y2} = -G * T_{in} + T_Y(0) \tag{8}$$

The final output of proposed FTDA topology can be derived by subtracting T_{Y2} from T_{Y1}.

$$T_{out} = T_{Y1} - T_{Y2} = 2 * G * T_{in} \tag{9}$$

Fortunately, the constant value ($T_Y(0)$) is eliminated from the final output. The final TD gain becomes twice the absolute value of the characteristic slope gradient of either FOG.

5.2 Programmable gain

The time amplification of the proposed FTDA is achi-eved based on (9). The output time gain can be written as

$$G_{FTDA} = 2 * \frac{C}{I_C} \tag{10}$$

where C is the parasitic capacitance at node R and I_C is the discharging current flowing out of C. Hence, the output time gain can be increased by adding more capacitance at node R or reducing the discharging current through controlling the drain current of the C-PMOS device.

As shown in Fig. 10, the proposed FTDA can add a programmable gain feature through use of C-PMOSs of different sizes. Each C-PMOS has a switch in series and each switch can be turned on or off by control registers. The C-PMOS device controls the discharge current as well as affects the parasitic capacitance at node R so it can be used to control the FTDA time difference gain.

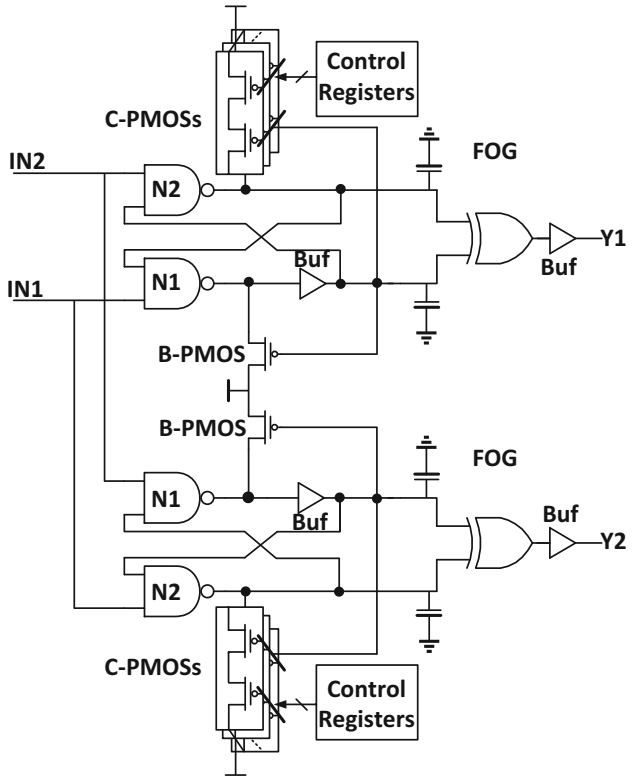


Fig. 10 FTDA with digital programmable gain feature

5.3 Changeable time input range

As discussed above, the proposed FTDA with zero input time interval, $T_{in} = 0$, can have a constant time delay $T_Y(0)$ for both FOGs, which can be called "DC operating point of time processing". It differs from the method in [6] by using the time delay to shift two logarithmic output curves left and right, respectively.

In actual applications, time processing circuits always move forward and cannot move back before the start time. Hence, output signals of FOGs can only exist on top of the horizontal line in Fig. 11, $T_Y \geq 0$. In other words, no matter the value of T_{IN} is negative or positive, the output regeneration time of FOGs is always larger than zero.

As a FOG has an intrinsic delay from IN2 node to output Y, including one NAND and one XOR gate delay, the smallest output regeneration time happens at the rising edge of IN2 ahead of that of IN1, resulting in a negative input time interval as shown in Fig. 7. Assuming T_{mim} is the smallest output regeneration time and the maximum output regeneration time can be increased by using a greater $|\Delta T|$. Considering two mirrored FOGs used in the FTDA, the positive slope FOG can be more positive and the negative slope one can be more negative. This splits the input–output transfer curve of the FTDA into three regions as shown in Fig. 11. The middle region, $|T_{in}| < \Delta T$, has twice TD gain compared to $|T_{in}| > \Delta T$.

Now assume T_{max} is the largest output regeneration time. In this case, the middle region, $-\Delta T < T_{in} < \Delta T$, is used as the input time range of the FTDA. The time difference between $T_Y(0)$ and T_{mim} is half the linear output time range and the corresponding input time interval is half the input dynamic range.

Based on the above discussion, the time input range can be adjusted by the TD gain as shown in Fig. 12. Now assume the time DC operating point ($T_Y(0)$), maximum and minimum output regeneration time are fixed. Figure 12 depicts the input–output transfer curves of the two FOGs used in the FTDA. The blue curve has higher gain but lower input range compared to the black curve. The red curve has lower gain but higher input range compared to the black curve. Their relationship looks like a moving scissor. Hence, the proposed FTDA can sacrifice the input range to obtain higher linear TD gain.

In addition, moving the time DC operating point as depicted in Fig. 13 increases the input range and keep the TD gain unchanged. The FTDA with the blue input–output transfer curves has the same TD gain as the black one, but its input range doubles. Based on the analysis of the FOGs, time DC operating point adjustment can be achieved by increasing the parasitic capacitances at input nodes of XOR

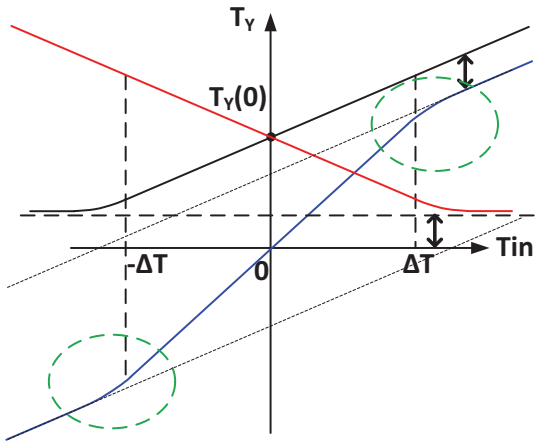


Fig. 11 FTDA input dynamic range is $-\Delta T < T_{in} < \Delta T$

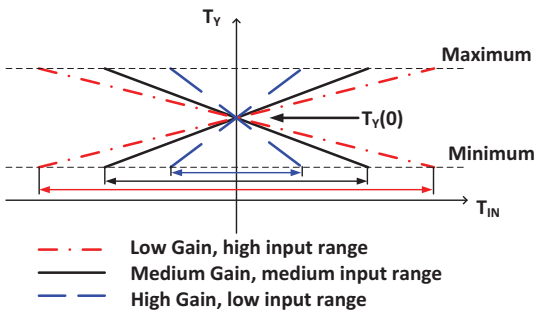


Fig. 12 FTDA changes the gain to obtain different time input range

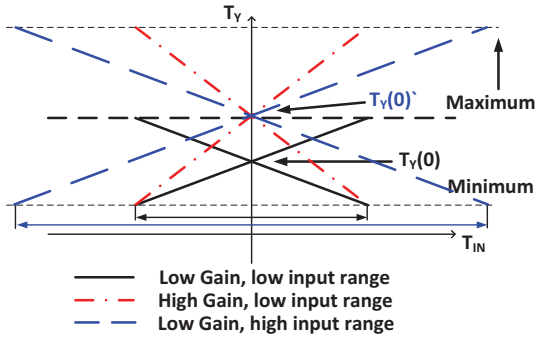


Fig. 13 FTDA changes the DC operating point to obtain different time input range and different TD gain

gate in Fig. 7. Furthermore, this method can also use to increase the TD gain with the same input time range, represented by the red curves in Fig. 13.

6 Non-idealities analysis with simulation results

6.1 Non-idealities

Compared to previous TDAs with a MUTEX structure, the proposed FTDA with two mirrored FOGs provides higher TD gain and better linear input range. Furthermore, a programmable gain feature can be added. However, the FTDA still suffers from some non-idealities with performance degradation.

First, the mismatch between two identical FOGs cause time offset and time gain error in the FTDA's input–output transfer curve. The FTDA concept is implemented by two identical FOGs and its time output is derived by subtracting their outputs. The mismatch effects include parasitic capacitance mismatch and MOSFET size mismatch, especially from the C-PMOS and B-PMOS devices. Due to B-PMOS size controls the output regeneration time of each FOG, the B-PMOS mismatch affects the absolute slope gradient and causes TD gain nonlinearity. The time DC operating point is determined by the size of C-PMOS and parasitic capacitance at the input node of the XOR gate. Hence, these mismatches result in both gain difference for FOGs and time offset in T_{out}.

Second, the TD gain is negatively proportional to the power supply as shown in Fig. 14. V_{DD} variation affects the drain current flowing through feedback keepers. For example, with $\Delta T > 0$, low V_{DD} makes the current I_{CP} flowing through C-PMOS smaller so that the source-gate voltage V_{SG} is pulled up slowly as shown in Fig. 15. The output regeneration time of the positive FOG in Fig. 9 becomes larger. Hence, the TD gain is increased by a smaller V_{DD}.

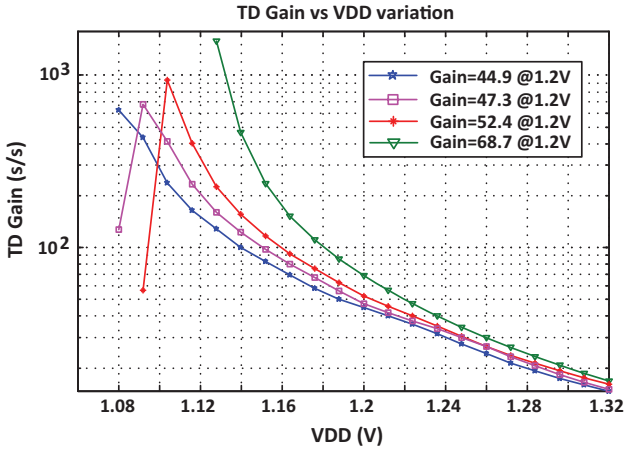


Fig. 14 V_{DD} variation affects the FTDA time difference gain

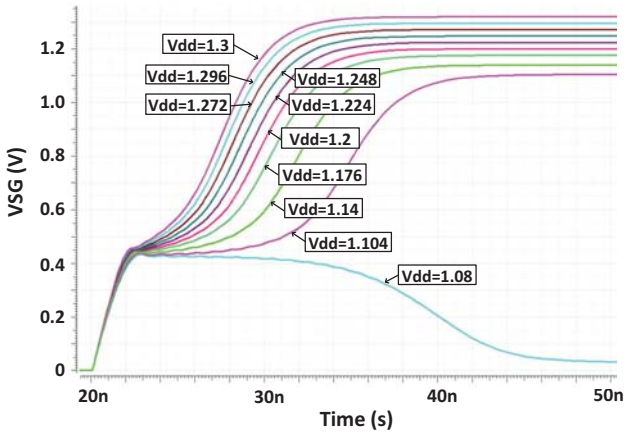


Fig. 15 V_{DD} variation changes V_{SG} of C-PMOS in positive FOG

However, too small V_{DD} can impair the FTDA operation. The drain current I_{CP} of the B-PMOS device is also influenced by V_{DD} changes. If V_{DD} is too low, the current balance operation functions poorly, causing V_{S1} to drop to ground instead of staying equal to V_{T1}. Node R1 in Fig. 15 is then pulled up to V_{DD}. As depicted in Fig. 14, the higher gain FTDA is more sensitive to V_{DD} variation and is much more easily damaged.

Third, temperature variation can influence TD gain. TD gain linearly increases with temperature decrease, as shown in Fig. 16. The principle of the proposed FTDA is based on drain current control of feedback keepers. Temperature variation affects the FTDA like changes in a power supply. Figure 16 shows that at low temperatures the TD gain can become too high resulting in damage to the FTDA.

Based on the above analysis, the proposed FTDA design needs a good bandgap reference to tolerate voltage and temperature variation. In addition, a common-centroid layout is also required to reduce the MOSFET and capacitor mismatch.

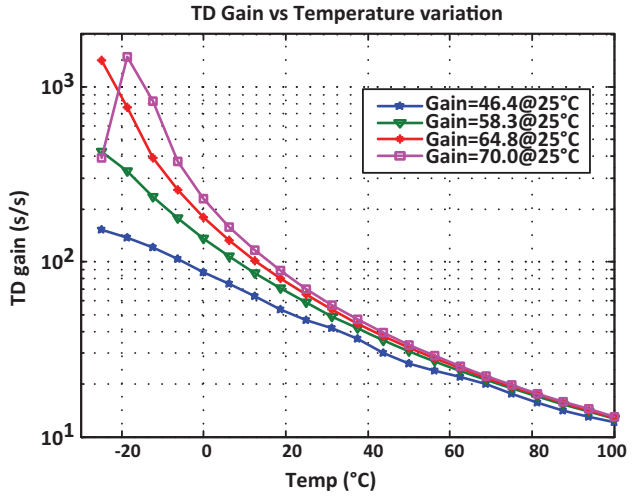


Fig. 16 Temperature variation changes TD gain

6.2 Corners simulation

Simulation results of different process corners are shown in Fig. 17. In the typical corner, TD gain of the FTDA example is 31 s/s. The fast NMOS/slow PMOS (FS) and slow NMOS/slow PMOS (SS) corners have higher TD gain. The fast NMOS/fast PMOS (FF) and slow NMOS/-fast PMOS (SF) corners have lower TD gain. These simulation differences occur because different corners influence the MOSFET speed. In other words, the drain current of MOSFETs have been affected. The above discussion also explains the TD gain variation caused by different corners.

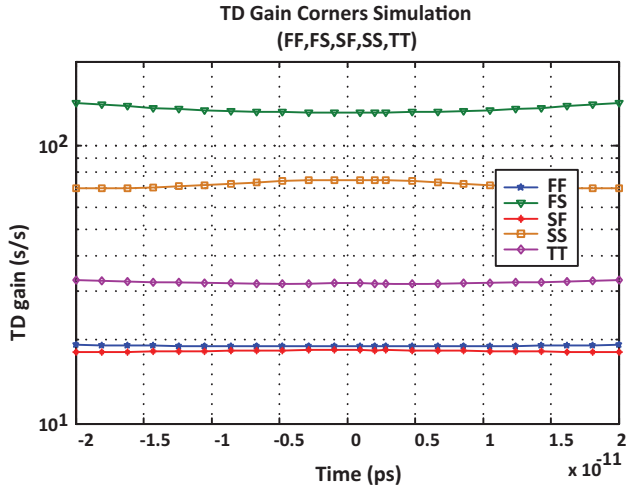


Fig. 17 FTDA process corners simulation

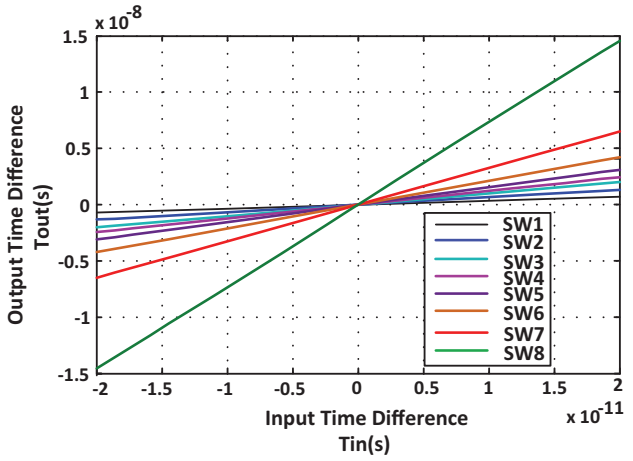


Fig. 18 Simulation result of transfer characteristic of different C-PMOS widths

6.3 Programmable gain simulation

The proposed FTDA with feedback keepers is demonstrated to provide a high gain time difference amplification by using 0.13 µm process with 1.2 V supply voltage. In the FOG, the size of C-PMOS varies from 280 to 500 nm. The capacitor in each input node of the XOR gates is 500 fF. The simulation results of the typical corner illustrated in Figs. 18, 19 demonstrates the time difference amplification and its TD gain is controllable by changing the size of the C-PMOS device.

The time difference amplification can be as high as 734 s/s in the input time difference ranging from − 20 to 20 ps. The FTDA with the highest gain needs to set the input frequency smaller than 2 MHz. When reducing the gain, input clock frequency requirements can be relaxed.

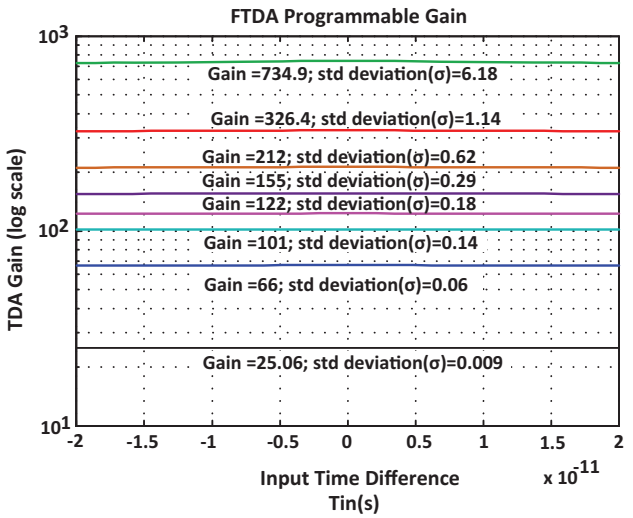


Fig. 19 Time difference gain with standard deviation for different C-PMOS widths

Table 1 Comparison of different TDAs

Methods	Gain	Input range (ps)	Process (nm)	Power (μW)	Result
Ref. [6], TDA with time-delay MUTEX	20	± 40	90	NA	Test
Ref. [8], closed-loop TDA with calibration	4	± 300	180	314	Test
Ref. [10], open-loop TDA	10–120	± 2000	130	23	Test
Ref. [11], pulse-train TDA	2–8	0–200	65	NA	Test
Ref. [13], programmable TDA with MUTEX	4–117	± 300	90	NA	Simulation
Ref. [14], TDA with controllable MUTEX	27–150	± 20	110	608	Test
This work, feedback TDA	25–734	± 20	130	91.54	Simulation

As shown in Sect. 5. Moreover, the TD gain provided by the FTDA is linear for the entire input time range. The maximum standard deviation (σ) is 6.18 for gain equal to 734.9 s/s in the typical process corner.

The test chip has been fabricated in 0.13 μm SiGe BiCMOS process with 297.8 μm × 88 μm area as shown in Fig. 20. The measurement process is underway.

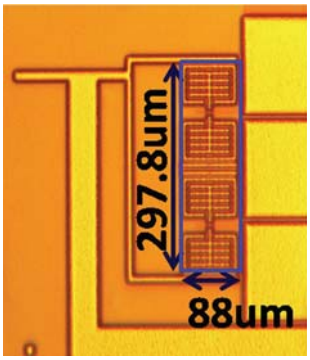


Fig. 20 Layout view of FTDA test chip

7 Conclusion

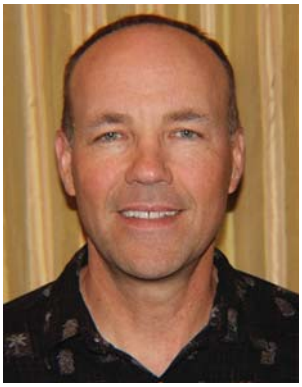
The paper proposes a feedback time difference amplifier by applying feedback keepers to achieve a significant improvement in the time difference gain and linearity. Two mirrored FOGs are used to form the FTDA providing a linear input–output transfer curve with a constant time offset. The most noteworthy components are two P-type keepers added to each FOG to provide feedback paths. The concept of time amplification through a feedback technique is achieved and explained. A programmable TD gain feature is discussed to be feasible. The capacitor discharging model is used to analyze the feedback gain control procedure. As a result, the proposed FTDA achieves the highest linear TD gain as depicted in Table 1. However, this design still suffers from PVT variation. Different non-ideal effects have been analyzed to help optimize it in the future.

References

1. Henzler, S. (2010). *Time-to-digital converters*. New York: Springer.
2. Hsu, C. M., Straayer, M., & Perrott, M. (2008). A low-noise, wide-BW 3.66 Hz digital fractional-n frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation. In *ISSCC 2008 digest of technical papers* (pp. 340–341).
3. Niitsu, K., Sakurai, M., Harigai, N., Yamaguchi, J., & Kobayashi, H. (2012). CMOS circuits to measure timing jitter using a self-referenced clock and a cascaded time difference amplifier with duty-cycle compensation. *IEEE Journal of Solid-State Circuits*, *47*(11), 2701–2710.
4. Villa, F., Lussana, R., Bronzi, D., Tisa, S., Tosi, A., Zappa, F., et al. (2014). Cmos imager with 1024 spads and tdcs for single-photon timing and 3-D time-of-flight. *IEEE Journal of selected topics in quantum electronics*, *20*(6), 364–373.
5. Abas, A. M., Bystrov, A., Kinniment, D. J., Maevsky, O. V., Russell, G., & Yakovlev, A. V. (2002). Time difference amplifier. *Electronics Letters*, *38*(23), 1437–1438.
6. Lee, M., & Abidi, A. A. (2008). A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue. *IEEE Journal of Solid-State Circuits*, *43*(4), 769–777.
7. Mandai, S., Iizuka, T., Nakura, T., Ikeda, M., & Asada, K. (2010). Time-to-digital converter based on time difference amplifier with non-linearity calibration. In *Proceedings of the ESSCIRC, 2010* (pp. 266–269). IEEE.
8. Nakura, T., Mandai S., Ikeda, M., & Asada, K. (2009). Time difference amplifier using closed-loop gain control. In *2009 symposium on VLSI circuits* (pp. 208–209). IEEE.
9. Dehlaghi, B., Magierowski, S., & Belostotski, L. (2011). Highly-linear time-difference amplifier with low sensitivity to process variations. *Electronics Letters*, *47*(13), 743–745.
10. Kwon, H.-J., Lee, J.-S., Sim, J.-Y., & Park, H.-J. (2011). A high-gain wide-input-range time amplifier with an open-loop architecture and a gain equal to current bias ratio. In *IEEE Asian solid state circuits conference (A-SSCC), 2011* (pp. 325–328). IEEE.
11. Kim, K. S., Kim, Y.-H., Yu, W., & Cho, S. H. (2013). A 7 bit, 3.75 ps resolution two-step time-to-digital converter in 65 nm cmos using pulse-train time amplifier. *IEEE Journal of Solid-State Circuits*, *48*(4), 1009–1017.

12. Baker, R. J. (2008). *CMOS: Circuit design, layout, and simulation* (Vol. 1). Hoboken: Wiley.
13. Alahmadi, A. N. M., Russell, G., & Yakovlev, A. (2012). Reconfigurable time interval measurement circuit incorporating a programmable gain time difference amplifier. In *IEEE 15th international symposium on design and diagnostics of electronic circuits & systems (DDECS), 2012* (pp. 366–371). IEEE.
14. Heo, M., Kwon, D., & Lee, M. (2014). Low-power programmable high-gain time difference amplifier with regeneration time control. *Electronics Letters*, *50*(16), 1129–1131.

Wenlan Wu has been pursuing the Ph.D. degree in electrical engineering at University of Nevada-Las Vegas since 2013. He received B.S. degree in Microelectronics from Xi'an University of Post and Telecommunications, Xi'an, China, in 2010, and the M.S. degree in electrical engineering from University of Macau, Macao, China, in 2013. He has worked as an intern at Alphacore, Inc since 2016. His research interests include high speed CMOS image sensor design, high resolution time-to-digital converters.



R. Jacob Baker received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas, in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno in 1993. From 1981 to 1987 he served in the United States Marine Corps Reserves (Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985 to 1993 he worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada test site. During this time, he designed, and oversaw the fabrication and manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. In 1991–1992 he was an adjunct faculty member in the department of electrical engineering at the University of Nevada, Las Vegas (UNLV). From 1993 to 2000 he served on the faculty in the department of electrical engineering at the University of Idaho (UI). In 2000 he joined a new electrical and computer engineering program at Boise State University (BSU) where he served as department chair from 2004 to 2007. At BSU he helped establish graduate programs in electrical and computer engineering including, in 2006, the university's second Ph.D. degree. In 2012 he re-joined the faculty at UNLV where he is currently a Professor of Electrical and Computer Engineering. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than 75 graduate students. In addition to this industry and academic experience, he has done technical and expert witness consulting for over 75 companies and laboratories. Over the last 32 years his research and development interests have been, or currently are, focused on analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits, circuit design for the use and storage of renewable energy, power electronics, and the delivery of online engineering education. Professor Baker is the named inventor on 144 US patents. He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation (over 50,000 copies in print), CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society, the 2007 Frederick Emmons Terman Award, and the 2011 IEEE Circuits and Systems Education Award. He currently serves, or has served, on the IEEE Press Editorial Board (1999–2004), as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011–2016), as a Distinguished Lecturer for the SSCS (2012–2015), and as the Technology Editor (2012–2014) and Editor-in-Chief (2015-present) for the IEEE Solid-State Circuits Magazine.

Phaneendra Bikkina received his M.S. degree in electrical engineering from Arizona State University in 2013. He is currently working on high speed mixed signal circuits and signal processing algorithms at Alphacore, Inc. His current research interests include high-speed and high-resolution data converters, high speed imagers and detectors, radio frequency interference detection and mitigation.

Yu Long received his M.S. and Ph.D. degrees in electrical engineering from Virginia Tech and the University of Tennessee in 2004 and 2016 respectively. Before that he also worked as a wirelesscommunication engineer in China. He is currently working at Alphacore Inc. on the design and applications of rad-hard circuits and system for power conversions with wide-band gap devices.

Andrew Levy Alphacore's senior program manager, has mathematics and computer science degrees and 30+ years of business management experience, having led engineering, marketing, business development and sales teams at IC, electronic design automation (EDA), and test and measurement (T&M) companies, including Intel, Cadence Design, and Credence Systems (now part of LTXCredence, an Xcerra company). A true entrepreneur, he has been a founder or early team member of five start-ups and has championed the development of innovative products everywhere he has worked.

Esko Mikkola received the B.Sc, M.S. and Ph.D. degrees in electrical and computer engineering from the University of Arizona, in 2000, 2002 and 2008, respectively. He is currently the chief executive officer of Alphacore, Inc., an Arizona based company specializing in analog and radio frequency electronics. His current research interests include high-speed data converters, electronics for high-speed imagers, GaN electronics, radiation hard electronics and hardware cybersecurity.