Two Techniques to Reduce Gain and Offset Errors in CMOS Image Sensors using Delta-Sigma Modulation

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***Abstract*—A per-column, delta-sigma, analog-to-digital converter for use in CMOS image sensors is reported. Two techniques, subtraction and preconditioning, are proposed to compensate for the column-to-column mismatches and the resulting fixed-pattern noise introduced into the image. Equations governing the operation of the proposed topology are developed. Experimental results verify that even in the presence of very large offsets, such as a 200 mV mismatch in the MOSFETs' threshold voltages, the proposed topology operates as desired.**

Keywords-Delta-Sigma Modulator; DSM; CMOS Image Sensor ADC; Gain Error

I. INTRODUCTION

This paper presents a per-column analog-to-digital converter (ADC) design using delta-sigma modulation (DSM) for use in a CMOS imager. Currently, mass-produced CMOS imagers use ADCs that are either pipeline or column parallel architectures requiring precision components [1]. The benefit of using a DSM ADC is that it's more tolerant to noise and power supply variations than traditional analog-to-digital conversion techniques. Also DSM-based ADCs don't require precise components, so they can be manufactured with good yield. However, as with any per-column ADC, there are practical matching concerns [1], [2], [3]. For example, fixed pattern noise will occur in the decoded image if the transfer functions of each column-parallel ADC are not identical. Variations in device characteristics can cause gain and offset errors in the ADCs' transfer functions. Path switching techniques have been introduced to reduce the effects of these errors [3], [6]. Unfortunately, a threshold voltage mismatch in the reference source-follower transistor in these topologies will cause a gain error in the DSM ADC transfer function. This gain error can be reduced through two different techniques, subtraction and preconditioning. Both techniques are discussed in this paper.

II. GAIN ERROR CORRECTION BY MEANS OF SUBTRACTION

Threshold voltage mismatches result in gain errors that can be reduced by generating two different reference currents through the same reference source-follower transistor, M14 in Fig. 1 [5], [6]. One reference current, say I_{REF1} in Fig. 1, is directed to one side of the DSM ADC, while the other reference current, I_{REF2}, is directed to the other side. The current mirror, M7/M8, subtracts out the reference source-follower transistor threshold voltage component resulting in a reference current that is free from the influence of M14's threshold voltage. This method is known as gain error correction by means of subtraction, and it's shown schematically in Fig. 1.

This DSM ADC measures the difference between the two analog input signals, V_{RESET} and V_{IMAGE}, with respect to two reference input signals, V_{REF1} and V_{REF2}, and converts this difference to a train of digital pulses. The conversion period takes N clock cycles. This DSM ADC requires a 4-phase, non-overlapping clock signal. The PHI1, PHI2, PHI3, and PHI4 signals are the four non-overlapping clock phases and their complement signals are PHI1B, PHI2B, PHI3B, and PHI4B, respectively. These signal's frequency is 1/4 the rate of the master clock denoted as f_{PHI}.

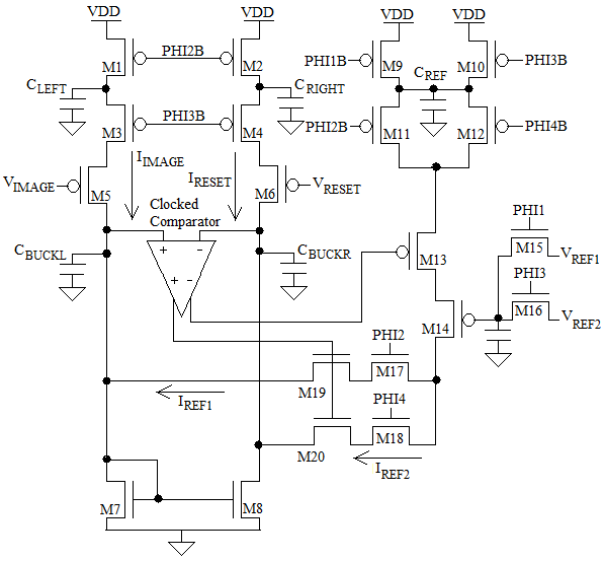

Figure 1. DSM ADC with gain error correction by means of subtraction [5], [6].

M5 and M6 are respectively known as the image and reset source-follower transistors. A dummy capacitor is added to the gate of M14 as a means to reduce the effects of charge injection and clock feed-through when PHI1 and PHI3 signals transition from high to low. The reference signal voltage needs to be on the gate of M14 a phase earlier and stays unchanged for the whole duration of the subsequent phase. This is to prevent any error in the magnitude of the two reference currents, I_{REF1} and I_{REF2}.

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On the first clock phase, M9 turns on and C_{REF} is charged to *VDD*. At the same time, M15 turns on and allows the first reference voltage, V_{REF1} to propagate to the gate of M14. At the end of the first clock phase, the clocked comparator measures the voltages on capacitor C_{BUCKL} and C_{BUCKR} and turns on M13, M19 and M20 for the remaining three clock phases if the voltage on C_{BUCKR} is lower than the voltage on C_{BUCKL}. M13, M19 and M20 are turned on for *M* times over the entire conversion period. During the second clock phase, M11 turns on and the first reference current, I_{REF1}, flows from C_{REF} to C_{BUCKL} if M13, M19 and M20 are turned on. The average I_{REF1} that flows into C_{BUCKL} is

$$I_{REF1} = \frac{M}{N} C_{REF} \frac{f_{PHI}}{4} \left(VDD - V_{REF1} - V_{th,M14}\right). \quad (1)$$

On the same clock phase, the voltages on C_{LEFT} and C_{RIGHT} are set to *VDD*. Then the third clock phase, C_{REF}, is reset back to *VDD* and the second reference voltage signal, V_{REF2}, is propagated to the gate of M14. During this phase, the image current, I_{IMAGE}, and reset current, I_{RESET}, will flow to C_{BUCKL} and C_{BUCKR} respectively.

$$\mathrm{I_{IMAGE}} = \mathrm{C_{LEFT}} \frac{\mathrm{f_{PHI}}}{4} \left(\mathrm{VDD} - \mathrm{V_{IMAGE}} - \mathrm{V_{th,M5}}\right) \quad (2)$$

$$I_{RESET} = C_{RIGHT} \frac{f_{PHI}}{4} \left(VDD - V_{RESET} - V_{th,M6}\right) \quad (3)$$

During the last clock phase, the second reference current, I_{REF2}, will flow from C_{REF} to C_{BUCKR} if M13, M19, and M20 remained on. The average I_{REF2} that flows into C_{BUCKR} is

$$I_{REF2} = \frac{M}{N} C_{REF} \frac{f_{PHI}}{4} \left(VDD - V_{REF2} - V_{th,M14}\right). \quad (4)$$

I_{REF1} has the same M14 voltage threshold component in its current equation as I_{REF2}. Assuming that there is no threshold voltage offset between the current mirror transistors, M7 and M8, this current mirror will subtract out M14's threshold voltage component from the true reference current, and then its average magnitude is

$$I_{REF} = I_{REF2} - I_{REF1} \quad (5)$$

$$I_{REF} = \frac{M}{N} C_{REF} \frac{f_{PHI}}{4} \left(V_{REF1} - V_{REF2}\right) \quad (6)$$

noting that mismatches in M7 and M8 are corrected for in the same way as mismatches in M5 and M6.

The digital code representation of the analog input signals, with respect to the two reference signals, can be found by summing the current into the C_{BUCKR} capacitor.

$$M = N \left(\frac{C_{LEFT}(VDD - V_{IMAGE} - V_{th,M5}) - C_{RIGHT}(VDD - V_{RESET} - V_{th,M6})}{C_{REF}(V_{REF1} - V_{REF2})}\right) \quad (7)$$

The ADC is tolerant to gain errors caused by threshold voltage mismatches because the denominator of the transfer function is free from the influence of the threshold voltage. Note that the gain of the DSM ADC can be changed by controlling the difference between the two reference voltage signals, V_{REF1} and V_{REF2}.

This DSM ADC is still susceptible, however, to a path offset error. The ADC can be modified to accommodate a path switching technique to reduce the effects of offset errors in its transfer function. Fig. 2 illustrates the DSM ADC with gain error correction by means of subtraction and offset error correction.

The conversion period of the DSM is now divided into 2 equal halves, where each half is *N*/2 clock cycles long. On the first half of the sensing period, control signals *SLT* and *SLB* are set to *VDD* and ground, respectively. During this sensing period, the digital code representation of the analog input signals, with respect to the two reference input signals, $M_{t=1}$, is

$$M_{t=1} = \frac{N}{2} \left(\frac{C_{LEFT}(VDD - V_{IMAGE} - V_{th,M5}) - C_{RIGHT}(VDD - V_{RESET} - V_{th,M6})}{C_{REF}(V_{REF1} - V_{REF2})}\right). \quad (8)$$

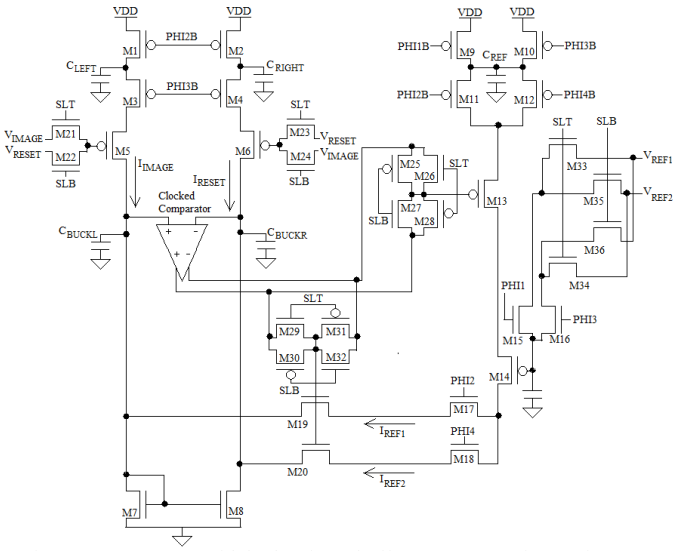

Figure 2. DSM ADC with both gain and offset error correction. Gain error correction by means of subtraction.

During the next half of the conversion period, SLT and SLB are driven to ground and *VDD,* respectively. The digital code representation of the analog input signals, with respect to the two reference input signals, for the second half of the sensing period, $M_{t=2}$ is

$$M_{t=2} = \frac{N}{2} \left(\frac{C_{RIGHT}(VDD - V_{IMAGE} - V_{th,M6}) - C_{LEFT}(VDD - V_{RESET} - V_{th,M5})}{C_{REF}(V_{REF1} - V_{REF2})}\right). \quad (9)$$

At the end of the sensing period, the digital output code for the two halves of the sensing period are added together and the final digital output code for the DSM with both gain and offset correction, is

$$M_{t=1} + M_{t=2} = \frac{N}{2} \left(\frac{(C_{LEFT} + C_{RIGHT})(V_{RESET} - V_{IMAGE})}{C_{REF}(V_{REF1} - V_{REF2})}\right). \quad (10)$$

The input-output transfer function of this DSM does not contain the threshold voltage of any transistor in the DSM. This means that the DSM is robust to any offset or gain error caused by threshold voltage mismatches. However, a gain error will still occur if the capacitors C_{LEFT}, C_{RIGHT}, and C_{REF} are mismatched. Note that the least significant bit voltage, V_{LSB} for this DSM ADC, with both offset and gain error correction by means of subtraction, is

$$V_{LSB} = \frac{2}{N} \left(\frac{C_{REF}}{(C_{LEFT} + C_{RIGHT})}\right) (V_{REF1} - V_{REF2}). \quad (11)$$

The bit accuracy increases linearly with the number of clock cycles, *N*, during the sensing period.

III. Delta-Sigma Modulation ADC with Gain Error Correction by Means of Preconditioning

At the beginning of every clock period, the initial voltage on the reference capacitor is usually set to *VDD*. If the initial voltage on C_{REF} is preconditioned by the reference source-follower transistor to another reference voltage instead of *VDD*, the true reference current that flows into C_{BUCKR} will be free from the influence of the threshold voltage. This will then lead to a transfer function that is robust to gain error. Fig. 3 shows the DSM ADC with gain error correction by means of preconditioning.

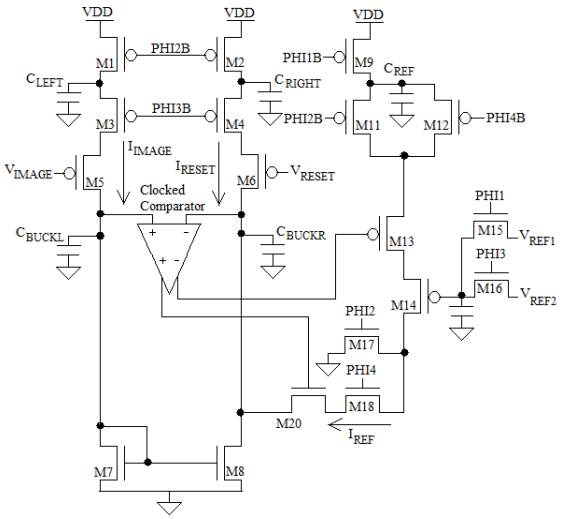

Figure 3. DSM ADC with gain error correction by means of preconditioning.

The operation of this DSM ADC is very similar to the DSM ADC with gain error correction by means of subtraction. It also requires 4-phase non-overlapping clock signals and its clock frequency is also 1/4 the rate of the master clock denoted as f_{PHI}. The generation of the image current, I_{IMAGE}, and reset current, I_{RESET}, in this DSM ADC is similar. However, the generation of the reference current is different. On the first phase of the clock signal, C_{REF} is set to *VDD* and the first reference voltage, V_{REF1}, propagates to the gate of M14. At the end of the first clock phase, the clocked comparator turns on M13 and M20 for the remaining clock phases, if the voltage on C_{BUCKR} is lower than the voltage on C_{BUCKL}. Like before, this happens *M* times over the entire conversion period. On the next clock phase, the voltage on C_{REF} is set to $V_{REF1} + V_{th,M14}$, if M13 is turned on by the clocked comparator. This is accomplished by allowing a current to flow from C_{REF} to ground through M11, M13, M14, and M17. The second reference current, V_{REF2}, will then propagate to the gate of M14 on the following clock phase. On the last clock phase, the reference current, I_{REF}, will flow from C_{REF} to C_{BUCKR}, if M13 and M20 are turned on by the clocked comparator. The magnitude of I_{REF} is

$$I_{REF} = \frac{M}{N} C_{REF} \frac{f_{PHI}}{4} \left(V_{REF1} + V_{th,M14} - V_{REF2} - V_{th,M14}\right) \quad (12)$$

which simplifies to

$$I_{REF} = \frac{M}{N} C_{REF} \frac{f_{PHI}}{4} \left(V_{REF1} - V_{REF2}\right). \quad (13)$$

The I_{REF} equation for this topology is similar to the I_{REF} equation of the topology with gain error correction by means of subtraction. Therefore, the same gain error correction property and input-output transfer function can be used. As before, a modification can be made to incorporate the path switching technique to reduce the effects of offset error in the transfer function. Its schematic for this design is shown in Fig. 4.

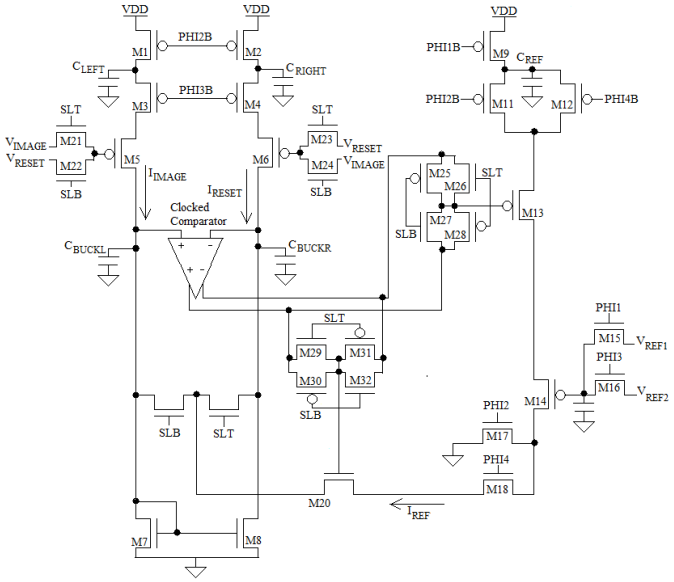

Figure 4. DSM ADC with both gain and offset error correction. Gain error correction by means of preconditioning.

IV. Test Chip Results

A test chip was fabricated in On's C5 process containing test structures to evaluate the performance of the proposed ADCs (see Fig. 5). The chip contains column slices with inputs to introduce mismatches to verify that the equations derived in this paper are valid.

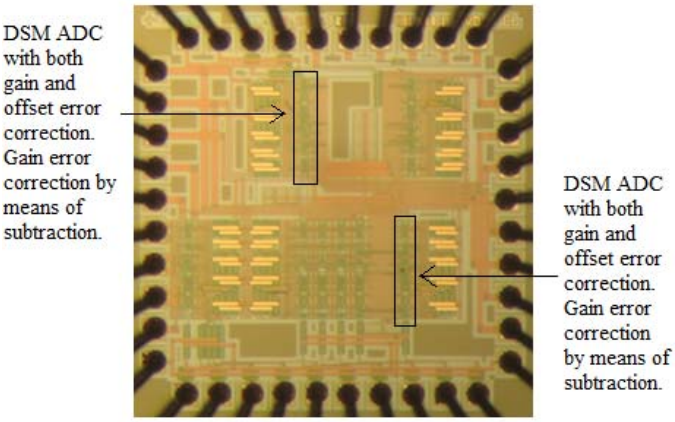

Figure 5. Test chip microphotograph.

Fig. 6 shows the measured results with offset and gain errors corrected by means of subtraction. Fig. 7 shows the test results for the DSM ADC with offset and gain errors corrected by means of preconditioning. Threshold voltage mismatch via M14 was evaluated (made worse) by offsetting V_{REF1} and V_{REF2} by equal amounts. Note that the offsets are unrealistically high in both figures, that is, 200 mV to verify robust operation.

The slope of the transfer function, using offset and gain error correction by means of preconditioning, Fig. 7, was constant with varying offsets on M14. However, using offset and gain error correction by means of subtraction, Fig. 6, had a steeper slope in its transfer function when the reference voltage is offset by –200 mV.

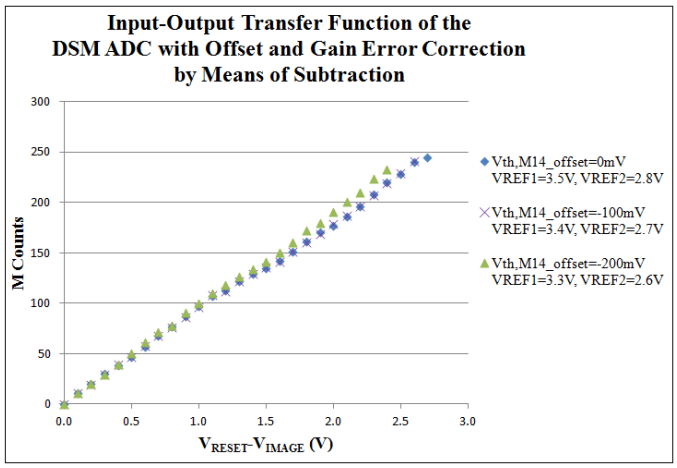

Figure 6. Using the subtraction technique to compensate for offsets in the reference voltages and threshold voltage of M14.

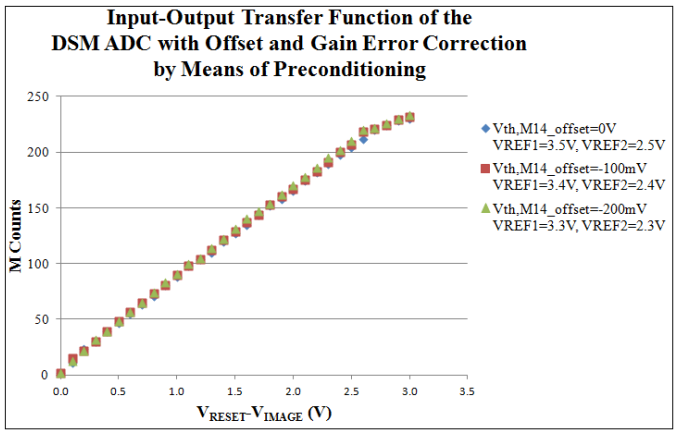

Figure 7. Using the preconditioning technique to compensate for offsets in the reference voltages and threshold voltage of M14.

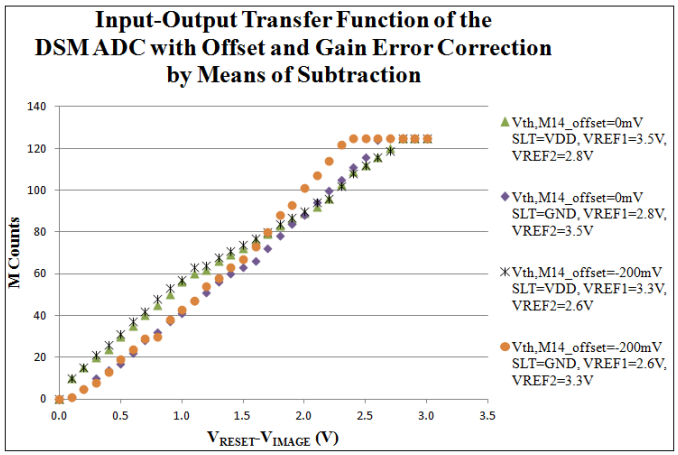

Figure 8. Showing transfer function with offset and gain errors by means of subtraction for each half of the conversion period.

Fig. 8 plots the input-output transfer function for each half of the conversion period. On the first half of the conversion period when SLT was set to *VDD*, the slope remained constant for both voltage offsets, 0mV and -200mV. However, a slope increase occurs during the second half of the conversion period, when SLT was set to GND and the reference voltage offset is –200 mV. This slope increase is most likely caused by the incomplete current mirroring of the larger second reference current from the left branch to the right branch of the DSM ADC. In other words, the drain of M7 must be greater than the NMOS threshold voltage, while the drain of M8 can swing near ground. This incomplete current mirroring will result in an equivalent V_{REF2} that is larger than intended, and thus resulting in a positive gain error. It should be noted, again, that a 200 mV offset is unrealistically large, so this issue, the increase in the transfer function's slope during the second half of the conversion, will likely never occur.

V. Summary and Conclusions

Gain error correction by the method of preconditioning is robust to a wide range of offsets. However, gain error correction by method of subtraction is only effective if the reference voltage levels are not too low. Path switching techniques can be applied in both methods to remove both offset and gain errors caused by mismatches in MOSFETs. Experimental results show that the matching between devices can be unrealistically large and the column parallel delta-sigma ADCs' behaviors track and match with good linearity. Finally, sensing resolution can be improved by sensing for longer periods of time. If, for example, a 100 MHz clock is used then the row readout time, using the data in Figs. 6-8 (250 counts maximum), is only 2.5 µs. For a 1,000 pixel row, this corresponds to a readout time of 2.5 ns/pixel which is faster than usually required.

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