Performance and Characteristics of Silicon Avalanche Photodetectors in the C5 Process

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***Abstract* — Avalanche photodetectors (APDs) have been fabricated in ON Semiconductor's C5 process without any special process or fabrication steps. The electrical and optical characteristics of APDs, with varying active area and guard ring configurations, are reported in this paper. Also reported are the details and considerations that went into laying out the APDs. It was found that substrate current was negligible and nearly independent of the geometrical shape of the substrate tie-downs around the perimeter of the APD structures. The measured APD breakdown is approximately 14 V. The devices show optical gains in excess of 1,000 at photocurrents of 10 μA.**

I. Introduction

Silicon avalanche photodetectors (APDs) find use in applications that require a high level of sensitivity to low light conditions at visible light wavelengths, that is at wavelengths less than 1 μm. Silicon APDs produced in specialized processes have been shown to have very good electrical characteristics. However, commercial APD applications require a low cost solution which limits the use of specialized processes. Specialized processes require extra steps and do not allow the integration of peripheral circuits on the same die adding additional cost. Reliable silicon APDs manufactured in a standard CMOS process are the ideal solution for low-cost production. Integrating the solution with CMOS is also desirable for readout. For non-commercial applications, including space and military, the desire is to reduce size, weight, power, and cost (SWaP-C). A monolithic active imager removes the cost associated with a hybrid focal plane array. It also reduces the weight and size. These features also provide benefit when considering the automotive market. Cost is a barrier in the consideration of active imaging systems for automatic braking and cruise control applications. A monolithic imager approach is the best chance of breaking into this market. Additionally, for single channel and multi-channel optical receiver products, for the OC-192 and OC-768 markets, an integrated APD provides a cost effective solution.

Avalanche photodetectors operate in a high gain region where the electric fields are large enough to produce impact ionization (aka avalanche multiplication). Electrons are created by the light penetrating, and being absorbed, in the depletion region of the photodetector. Impact ionization occurs when an electron gains enough energy, in between collisions, to create additional electrons. As a result the additional and subsequent collisions lead to a multiplication of the light-generated electrons. As is commonly known with increasing reverse bias, the electric field becomes larger along with the depletion width. Avalanche breakdown will occur when the multiplication factor, M, increases beyond unity [1], [2]. For reliable performance bending (non-uniform) electric fields, which result from curved edges, must be avoided. Ensuring that the depletion region is normal to the surface of the wafer is critical in the presented design. Guard rings are used to collect current injected into the substrate preventing undesired interaction with neighboring circuitry.

Section II of this paper discusses the considerations that go into APD layout. Section III reports the experimental results. Section IV provides a conclusion along with suggestions for future work. Section V details acknowledgements.

II. APD Test Chip

A test chip was laid out, Fig. 1, and tested using ON's C5 process. The C5 process is a standard CMOS process that includes three metal layers, two poly layers, n+/p+ active

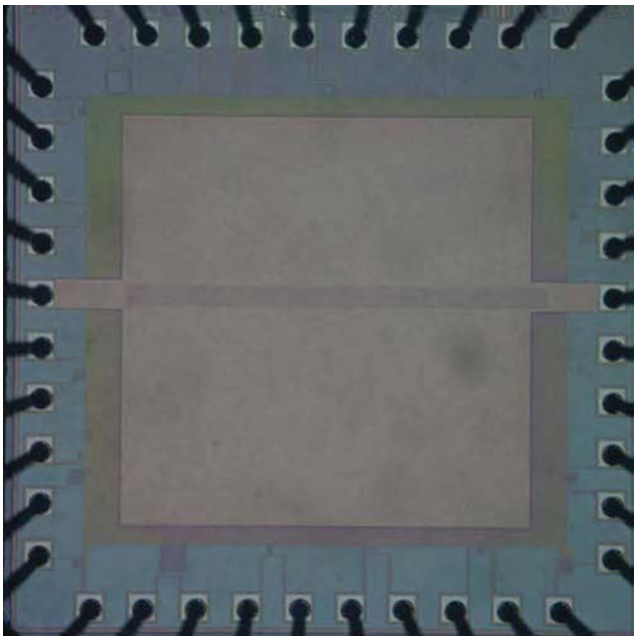

Figure 1 – Fabricated MOSIS chip with several APD structures. The center of the chip is covered with metal to keep light from generating carriers in the substrate and thus unwanted noise. The APD structures are adjacent to the bond pads around the perimeter of the chip.

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areas, and n-wells with a p-type substrate. Several different APD structures were laid out in the test chip to investigate the influence of active area size on performance as well as guard ring layout effects on substrate current. APDs were structured using different size active and guard ring areas. Guard rings protect against injection into the substrate from the formation of a parasitic pnp transistor but also decrease the fill factor. The guard rings collect the injected current before it finds its way to adjacent circuitry.

The chip shown in Fig. 1 was fabricated through the MOSIS service [4]. Figure 2 shows the partial layout of one of the APDs on the chip while Fig. 3 shows a microphotograph of the structure. The active, or light absorbing (avalanche area), of the APD is formed using the n-well with the p^+ layer as shown in the simplified layout and cross-sectional view seen in Fig. 4. This creates a larger depletion width mainly in the lighter-doped n-type region where photons can be absorbed to create electron-hole pairs. In order to increase the amount of active area exposed to light, a single contact is used to connect to the APD p^+ active area (note that metal running from the contact blocks light penetrating into the active area).

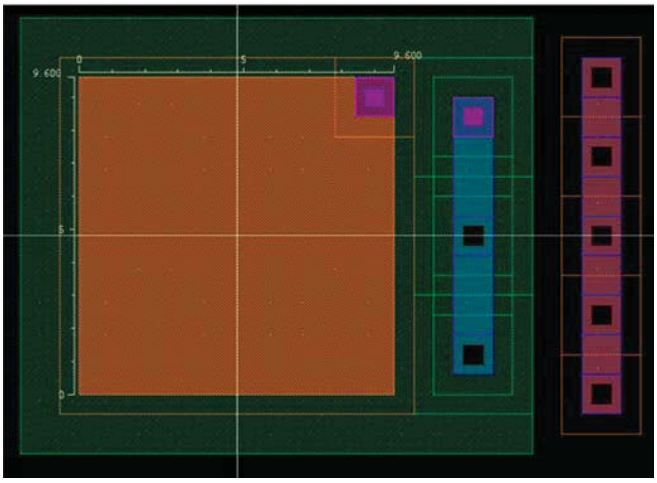

Figure 2 – An APD with a 9.6 μm square active area with reduced guard rings.

To guard against early breakdown due to higher electric fields from curved edges (junction curvature effect) [3], shallow trench isolation was utilized to ensure a planar p^+ to n-well transition. The entire depletion region, where impact ionization occurs, is normal to the surface of the wafer as shown in Fig. 4. The size of the active area will impact uniform avalanche multiplication. A smaller active area reduces the risk of this occurring at the cost of a lower light-absorbing area. The speed of the device is limited by diffusion of carriers, drift time in the depletion region, and the depletion region capacitance [2]. A larger depletion region decreases the capacitance but also affects transit times which can limit the frequency response. The series resistance of the n-well region should be minimized where possible to maximize speed characteristics. The APD structures reported

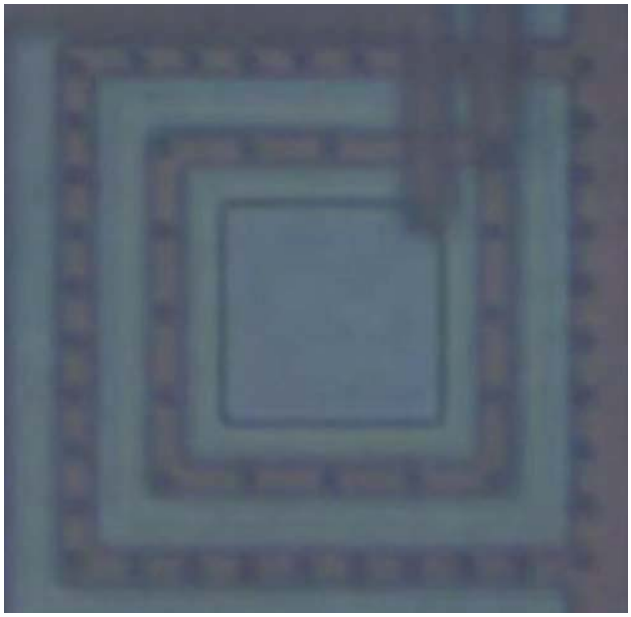

Figure 3 – Showing a microphotograph of an APD with a 9.6 μm square active area.

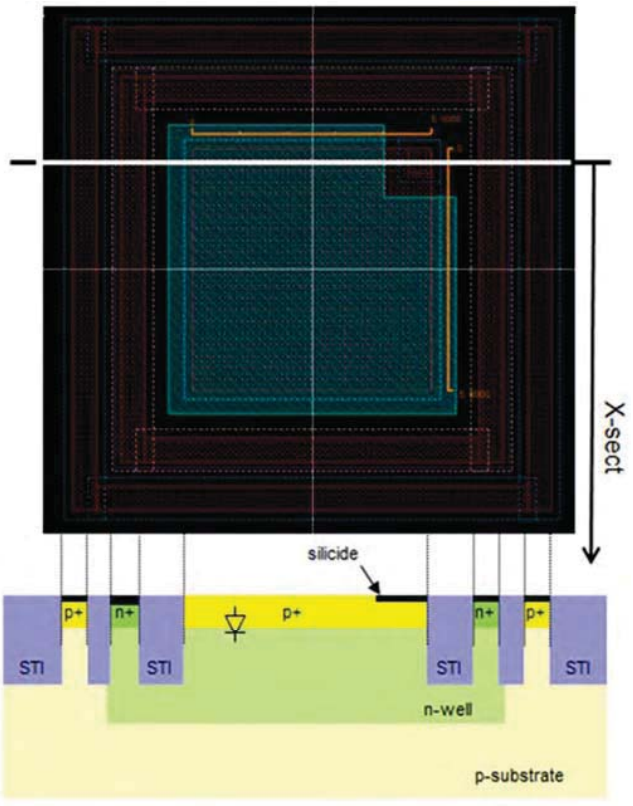

Figure 4 – Silicon APD cross-sectional view showing the lack of bending in the diode's depletion region (between the p+ and the n-well).

here include multiple contacts to the n-well region to decrease the series resistance. This is seen in Figs. 3 and 4 as the inside metal square ring surrounding the inside active area (Fig. 3, reddish color and red layout color in Fig. 4).

Finally it's important to note, when laying out the APDs, that the optical window above the APD structure (p+ to n-well) can be blocked if not careful. For example, processes that use silicided active (a refractory metal is added to the silicon active area to reduce the sheet resistance) will block light from the active area of the APD. A silicide block layer should surround the active area (but not the contacts from metal1 to active). Also, of course, metal can't be laid out over the APD structure [5].

III. Experimental Results

Electrical current measurements were performed to demonstrate functionality and to verify that the devices' currents scaled with the size of the active area. Fig. 5 shows the result from a photodetector consisting of a 19.2um square active area. Result is typical of all photodetector measurements. No measureable substrate current was detected when the diodes are reversed biased. This result indicates that substrate tie-downs around the n-well, as seen in Fig. 6, are not needed, that is, they are only required on one side of the APD structure. This is important since it indicates that the active area, relative to the rest of the diode, can be a larger portion of the overall APD layout.

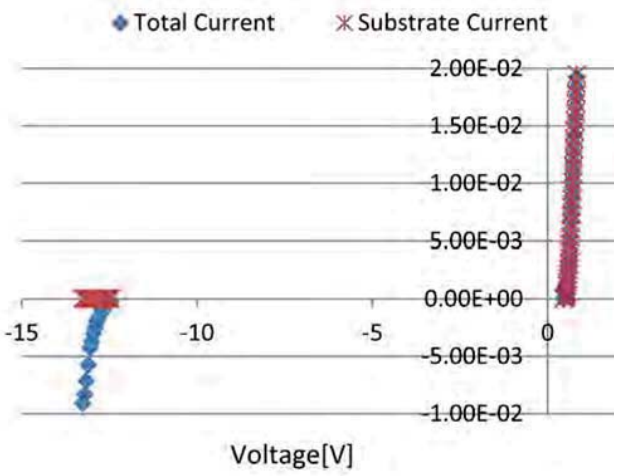

Figure 5 – Typical APD I-V curves showing substrate and APD currents.

As seen in Fig. 5, the APD was found to have a reverse breakdown voltage of approximately 14.0 V. Forward bias currents occur first in the p-substrate to n-well diode. This is expected due to the lower built-in potential of the p-substrate to n-well pn-junction when compared to the p+ to n-well pn-junction. Since the APD is never operated in a forward-biased mode the resulting substrate current isn't a concern.

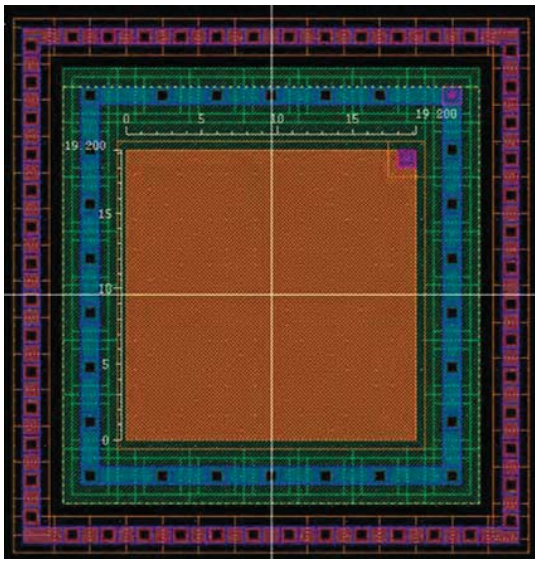

Figure 6 – Layout of a 19.2 μm square active area with maximized guard rings. A ring of p+ is placed around the n-well to ensure injected substrate current is collected and doesn't find its way into adjacent circuitry surrounding the APD.

Detailed current versus voltage measurements were taken in both dark and illuminated conditions. Dark conditions were produced using a light-proof enclosure. The illumination source was an uncalibrated, broadband microscope illuminator. The substrate and p^+ regions were tied to ground while performing a reverse bias voltage sweep and measuring current. Representative results from a photodetector with a 51 μm square active area are shown in Fig. 7. Only the bias range from 11.5 to 14.5 V is shown, in order to highlight the transition from ordinary diode conduction to avalanche multiplication.

The rapid increase in dark current at 13.5 V indicates the onset of avalanche multiplication initiated by thermally-generated carriers in the depletion region. Under "light" conditions a non-multiplied photocurrent of 1-2 nA is dominant until avalanche multiplication of photo-generated carriers begin at about 13.55 V.

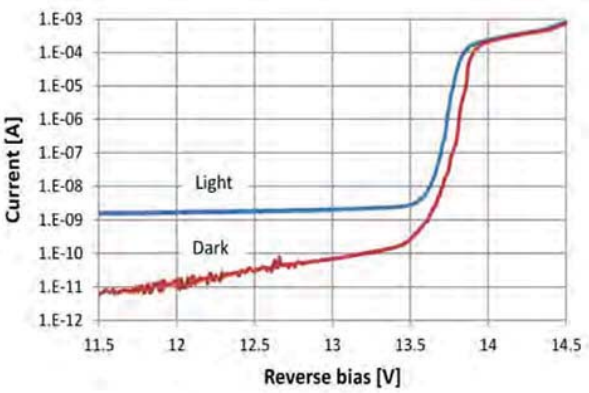

Figure 7 – Current measurements in dark and light conditions.

At high bias (V > 13.9 V) the rapid increase in current is moderated as the current-voltage characteristics become dominated by space-charge effects and heating [5]. This is not a desired operating regime for the APD and the data are not further analyzed.

Figure 8 shows the APD photocurrent as a function of reverse bias. Figure 9 shows the avalanche gain, M, of the APD, defined as the photocurrent at a given bias divided by the photocurrent at the bias where M=1. Here we have defined the M=1 bias as occurring just before the knee in the photocurrent curve, or 13.50 V.

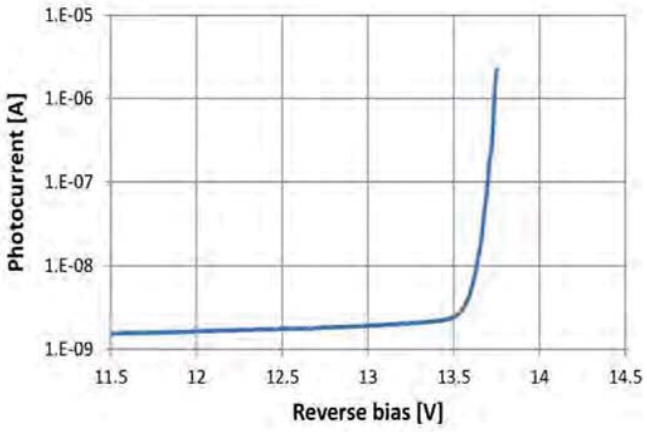

Figure 8 – Showing the APD photocurrent as a function of the diode's reverse bias voltage.

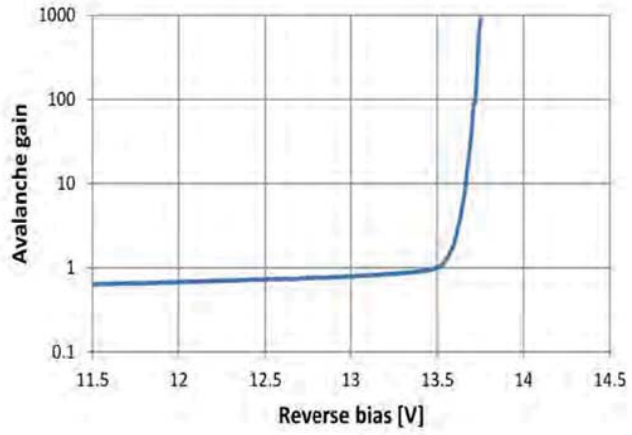

Figure 9 – Avalanche gain as a function of the diode's reverse bias voltage.

IV. Conclusion and Future Work

This paper reported the characteristics of APDs fabricated using ON's C5 fabrication process. Several different photodetectors were laid out and fabricated using various size active area and guard ring configurations. Characterization of the APD structures, fabricated in a standard CMOS process, demonstrated promising results.

Substrate currents were negligible and nearly independent of the geometrical shape of the tie-downs around the perimeter. This favors the design of structures with a smaller tie-down region which benefit from a larger fill factor. Gains in excess of 1,000 were found to be achievable. Measured gains are compatible with the applications detailed in this paper. Photodetector currents in the high gain region are favorable in relation to the design of read out integrated circuits (ROICs) regarding signal to noise concerns.

Future work may include characterizing the absolute responsivity, spectral response, pulse response, noise characteristics, and modulation bandwidth of the APDs. Additionally, the use of on-die readout circuitry, and characterization of an array of APDs with associated readout circuitry may be examined.

V. Acknowledgements

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VI. References

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