ON-CHIP 3D INDUCTORS USING THRU-WAFER VIAS

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***Abstract*—Three-dimensional (3D) inductors using high aspect ratio (10:1); thru-wafer via (TWV) technology in a complementary metal oxide semiconductor (CMOS) process have been designed, fabricated, and measured. The inductors were designed using 500 µm tall vias, with the number of turns ranging from 1 to 20 in both wide and narrow-trace width-to-space ratios. Radio frequency characterization was studied with emphasis upon de-embedding techniques and the resulting effects. The open, short, thru de-embedding (OSTD) technique was used to measure all devices. The highest quality factor (*Q*) measured was 11.25 at 798 MHz for a 1-turn device with a self-resonant frequency (f_{sr}) of 4.4 GHz. The largest inductance (*L*) measured was 45 nH on a 20-turn, wide-trace device with a maximum *Q* of 4.25 at 732 MHz. A 40% reduction in area is achieved by exploiting the TWV technology when compared to planar devices. This technology shows promising results with further development and optimization.**

Keywords- 3D; Integrated Inductors; Thru-Wafer Vias (TWVs), Thru-Silicon Vias (TSVs);

I. INTRODUCTION

The interest and proliferation of radio-frequency (RF) circuits in recent years has provided broad opportunity for the development of front-end RF modules, such as the voltage-controlled oscillators (VCOs), low-noise amplifiers (LNAs) and switching regulators needed to support new wireless applications [1, 2], including multi-mode wireless technology [3]. These RF modules have their foundation built upon discrete passive circuit components like the high frequency (HF) inductor. In the last decade, integration of monolithic inductors in silicon-based complementary metal oxide semiconductors (CMOS) has been realized and is preferable, due to the aggressive scaling in MOS devices, and its improved performance above 1 GHz [4, 5]. This movement has the added benefit that does not rely on off-chip components [3].

As devices scale, designers are challenged with producing smaller and more efficient RF building blocks, while maintaining or improving circuit performance, predictability, and robustness [2]. These three design requirements directly influence the selection of passive components used in the building blocks and thus have fueled the quest for an improved integrated inductor.

While the inductive coil has been around for over 100 years, its wide-spread use in modern CMOS circuits has been limited by its relatively large size (when compared to other circuit elements) and its inherent performance and integration limitations.

In order to achieve a reasonable inductance value (~10 nH), a planer inductor needs to be designed and manufactured with an extremely large footprint, on the order of 250 um^2. Unfortunately, increasing the inductor size both increases the manufacturing cost and produces undesired parasitic effects thus reducing its fundamental performance factors. This includes a poor quality factor (*Q*), a reduction in self-resonant frequency (f_{sr}), and a low inductance value (*L*). With this information in hand, circuit designers will be able to optimize and further experiment with new design solutions to achieve a better integrated inductor. This paper provides a starting point for an alternative inductor design, a 3D inductor using through-wafer vias (TWVs), also known as through-silicon vias (TSVs). An example layout/cross-section is seen in Fig. 1. This image of the 3D inductor was generated, and ultimately simulated, with Ansoft's HFSS software.

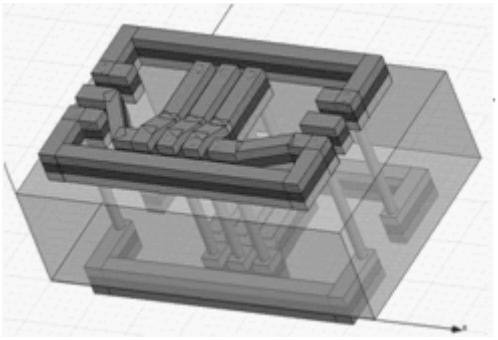

Figure 1. HFSS 3D Inductor Architecture

II. INDUCTOR PHYSICS

A. The Inductive Phenomena

An A/C current flowing in a straight wire, a simple coil of wound wire (solenoid), or a CMOS monolithic planar spiral inductor gives rise to the magnetic field intensity *H*, measured in units of A/m, and is related to the magnetic flux density *B*, measured in units of Tesla, as seen below in (1). The magnetic permeability μ is absolute magnetic permeability.

$$B = \mu H \tag{1}$$

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The total magnetic flux is equal to the integral of the magnetic flux density over an area of a surface S that intersects the field lines. In the special case of a planar surface, this can be simplified where A is the cross-sectional area of the intersecting surface and θ is the angle between the surface and the magnetic field lines that extend normal to the flow of current. In other words

$$\Phi_m = \int_S B \cdot dS \rightarrow \Phi_m = BA\cos\theta \quad (2)$$

Flux linkage (λ) represents the total magnetic flux passing through a surface *S* of a single loop of current-carrying wire. This is covered in (3), where N is the number of loops. For example, if two *N*-turn loops are tightly wound around *S,* the magnetic flux generated from each loop is shared through both loops. As such, the total magnetic flux linkage is increased by the square of the number of loops *N* times the magnetic flux of one loop of wire as shown below. The quantity of inductance can be determined by the ratio of the flux linkages to the current that creates the magnetic flux, as shown in (4). In other words, inductance is primarily a function of geometric shape.

$$\lambda = \Phi_T \cdot N \rightarrow \lambda = \Phi_1 \cdot N^2 \quad (3)$$

$$L = \frac{\lambda}{I} = \frac{\phi_T \cdot N}{I} = \frac{\mu \cdot N^2 \cdot \pi \cdot a^2}{h} \quad (4)$$

B. Mutual- and Self-Inductance

Using the method presented in the last section, two types of inductance make up the total inductance: mutual- and self-inductance. Mutual-inductance is a result of the proximity effect occurring between two closely spaced circuits, circuit elements, or wires [7] in series or parallel. Accordingly, this depends on the amount of flux linkages interacting between the two elements. Illustrated in Fig. 2 are two 3-loop coils of wire with interacting flux linkages. Coil A is being driven by current I_A, and as such is creating the flux density from coil A, while coil B is not being driven, but rather receiving.

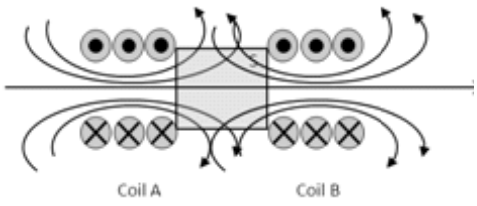

Figure 2. Mutual-Inductance of Two Coils

C. Electric/Magnetic Fields

The planar square spiral provides the best illustration of the electromagnetic fields exhibited and the utility of a physical model. As illustrated in Fig. 3, one magnetic and three electric fields are produced when an AC voltage is applied to port 1 [6]. The effects of the electric fields are modeled using capacitors while magnetic fields are modeled by inductors. Figure 4 shows the lumped circuit-equivalent planar inductor circuit model.

The first electric field E_1 is a result of the voltage difference between the terminal connections of the spiral and is simply due to ohmic losses in the traces [6]. This is directly dependent upon material resistivity (ρ) and is modeled as the series resistance R_S. The second electric field E_2 is a consequence of the voltage difference between any two turns in the spiral and any individual turn and the underpass [6]. This is a consequence of the second port being connected using a lower level of metal, which induces an inter-winding parasitic capacitance due to the presence of the interlayer dielectric. The modeling parameter for E_2 is C_P [6]. The third electric field E_3 is present due to the voltage difference between the silicon substrate and the metal of the spirals.

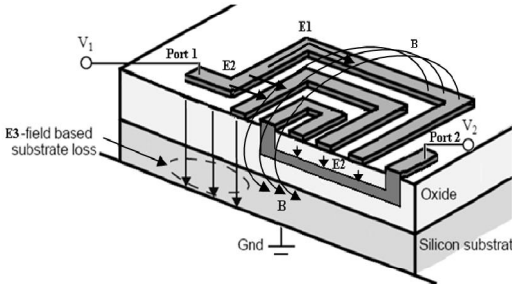

Figure 3. Electric and Magnetic Fields in a CMOS Planner Inductor

Field E_3 induces capacitive coupling to the substrate and is often times the most predominant parasitic since it extends into the substrate [6]. This is modeled as the parameter C_{OX}. The effect of this field is made worse because many CMOS circuits use low-resistivity substrates, an epitaxial layer, having a resistivity in the range of < 10 Ω/cm. This allows for current to flow in the substrate easily. Due to this current flow, it is necessary to include modeling parameters for the intrinsic substrate capacitance and resistance. These parameters are identified as C_{SUB} and R_{SUB}, respectively.

The final field is the magnetic field *B* produced by the AC current that flows through the traces of the spiral. While the magnetic field is what induces the desired inductive behavior, it also creates a complementary parasitic behavior in the metal traces due to eddy-currents [4, 6, 7, 8, 9].

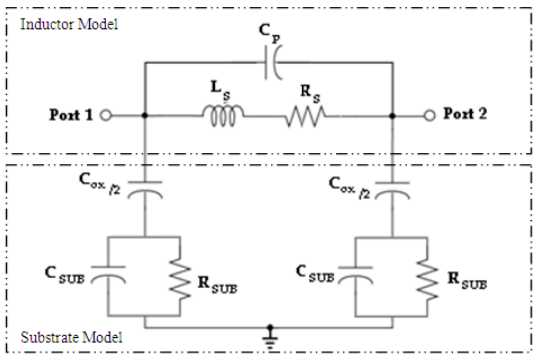

Figure 4. Equivalent Planar Inductor Circuit Model

III. 3D Inductor Fabrication

A. Fabrication

Fig. 5 illustrates the first generation of 3D masks for a 1-turn inductor where a) shows the via mask, b) shows the top metal mask with ground-signal-ground (GSG) probe pads and guard ring, and c) shows the bottom metal mask with guard ring. Fig. 5d depicts all masks overlaid to illustrate mask alignment. The Fig. 5e micrograph shows the topside view of a fabricated device. An optical resolution limitation was identified due to the dry-film photoresist which caused subsequent turns to become shorted. In Fig. 5f a SEM of the device clearly shows this. As such, a line-to-line spacing design rule of 30 µm minimum became necessary.

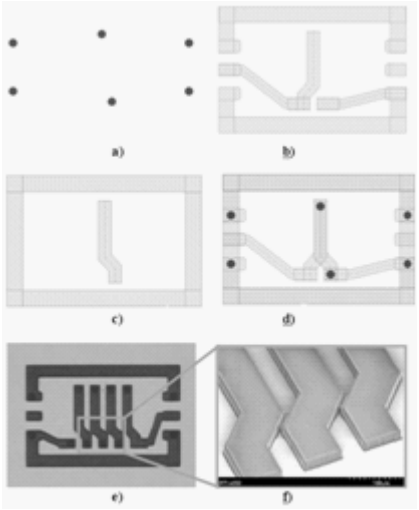

Figure 5. 1st Generation 3D Inductor Masks and Fabricated Device

Due to the new design rule, a second set of masks were needed that traded polygon lines for straight lines oriented off-angle. Mask redesign allowed for the addition of narrow-trace (NT) and wide-trace (WT) line-to-line spacing devices. Fig. 6 shows similar masking levels as Fig. 5 with the addition of these new devices.

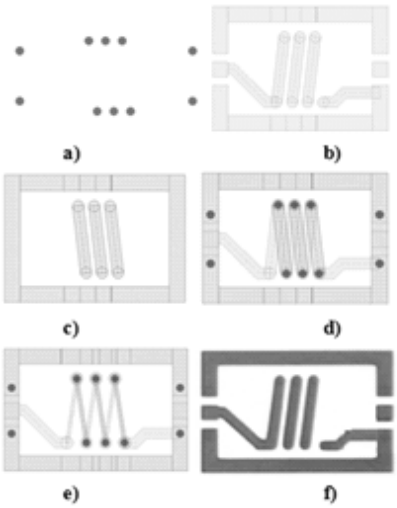

Figure 6. 2nd Generation 3D Inductor Masks and Fabricated Device

The TWV fabrication process flow is beyond the scope of this paper. The interested reader can review works reported at BSU covering solid and barrel-coated via methods.

IV. Measurement Technique

A. Equipment Setup/Calibration/De-Embedding

The 3D inductors were characterized with an HP8510C vector network analyzer (VNA) in conjunction with a manual Cascade™ Microtech Summit microwave probe station, 150 µm pitch ground-signal-ground Infinity Probes, a standalone PC, and a non-conductive auxiliary chuck built to isolate the bottom metal traces during measurement.

The short, open, load, and thru (SOLT) calibration method [10, 11] was used to remove parasitic factors between the VNA and the probe tips with a reasonably accurate (±10%) measurement below 20 GHz. Measurement repeatability is obtained by manually placing the probe tips exactly centered on the probe pads.

V. Measured 3D Inductor Performance

The highest quality factor observed below the self-resonant frequency (f_{sr}) on the measured devices, occurred on the 1-turn inductors and measured Q_{max} values of 11.25 (WT) and 7.84 (NT). Increasing the number of turns was dominated by parasitic components and decreased with increasing N-turns as shown in Fig. 7.

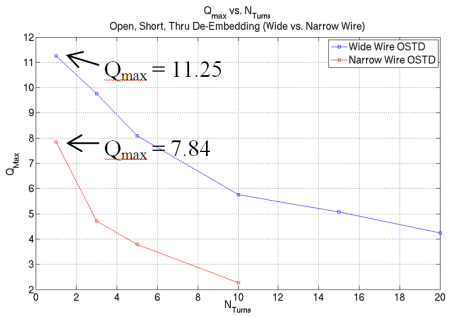

Figure 7. Q_{max} vs. N_{Turns}

The self-resonant frequency can be obtained from the quality factor plot or the impedance plot of $|Z|$. Fig. 8 shows this in the plot of f_{sr} versus N-turns. The NT devices resulted in a higher f_{sr} ~ 4.58 GHz for a 1-turn device, while the WT devices degraded at a slightly faster rate with increasing N.

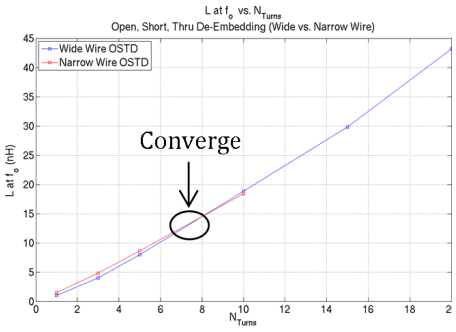

Figure 8. f_{sr} vs. N_{Turns}

The basic 1-turn 3D inductor measures inductance values of 1 nH (WT) and 1.5 nH (NT). As expected, inductance increases with the number of turns due to the increase in flux linkages. The measured inductance at the characteristic frequency f_0, versus the number of turns between the NT and WT devices, converges at N=8 as seen in Fig. 9.

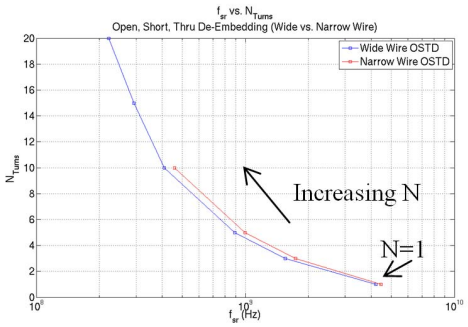

Figure 9. L vs. N_{Turns}

The WT 1-turn device measures a |Z| of 4.8 Ω, while the 20-turn device measures 20Ω at f_0. The resistance increases non-linearly with an overall average increase of 2 Ω per-turn. The WT devices overall measured lower in resistance than the NT devices. The 1-turn WT inductor measured 54% less resistance than the 1-turn NT inductor. Fig. 10 illustrates the impedance growth with increasing N values.

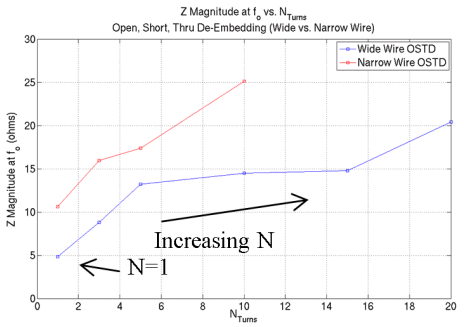

Figure 10. |Z| at f_o vs. N_{Turns}

The phase angle, also measured at f_o, measured higher on the WT devices, in the range of 84º to 76º for N = 1 and N = 20, respectively. The NT devices measured angles in the range of 82º to 66º for N = 1 and N = 10, respectively. Since phase angles at 90º cause resonance, a lower phase angle provides increased margin that ensures reliable performance.

VI. Conclusion and Future Work

The 3D TWV inductor architecture provides a 40% smaller device footprint when compared to an equivalent N-turn planer device. The 3D 1-turn wide inductor achieved a maximum WT device de-embedded Q of 11.25 and f_{sr} = 4.4 GHz. While the 1-turn WT device measured ~1 nH and increased non-linearly to ~45 nH up to 20-turns. Convergence between WT and NT devices occurs at N = 8 turns, with the NT device providing higher inductance below N = 8 and the WT device providing higher inductance above N = 8. The 1-turn WT device series resistance measured 4.8 Ω and increases to 20 Ω for N = 20. However, each additional turn added drops off to 1.02 Ω per turn above N = 15.

As with the planar inductor, the 3D TWV inductor suffers similarly from capacitive coupling to the substrate. As such, future work on this architecture should be focused on optimization of the via height (wafer thickness), the via pitch, the inductor radius, and the line-to-width space ratio. The architecture would also benefit from devising a scheme to either remove or replace the silicon substrate within the core of the inductor.

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