Systematic Design of Three-Stage Op-amps using Split-Length Compensation

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***Abstract*—Over the past decade CMOS technology has been continuously scaling which has resulted in sustained improvement in transistor speeds. However, the transistor threshold voltages do not decrease at the same rate as the supply voltage (V_{DD}). Besides, the open-loop gain available from the transistors is diminishing. This trend renders the traditional techniques, like cascoding and gain boosting, less useful for achieving high DC gain in nano-scale CMOS processes. Thus, horizontal cascading (multi-stage) must be used in order to realize high-gain op-amps in low-V_{DD} processes. This paper presents a design procedure for op-amp design using split-length compensation. A reversed-nested split-length compensated (RSLC) topology, employing double pole-zero cancellation, is illustrated for the design of three-stage op-amps. The RSLC topology is then extended to the design of three-stage fully-differential op-amps.**

***Index Terms*—CMOS Amplifiers, fully-differential, nano-CMOS, Op-amp compensation, split-length, three-stage op-amps.**

I. Introduction

OPERATIONAL Amplifiers are an essential component in the modern mixed-signal systems. They are utilized in wide variety of circuits including data-converters, filters, voltage references and power management circuits. However, continued scaling in CMOS processes has continuously challenged the established paradigms for operational amplifier (op-amp) design. As the feature size of CMOS devices scales, creating faster transistors, the supply voltage (V_{DD}) is reduced. The higher speed due to CMOS scaling comes at a price of the reduction in transistor's open-loop gain ($g_m.r_o$). Further with device scaling, the threshold voltage of transistors doesn't scale well with V_{DD}, resulting in lower headroom for analog design. In addition to these challenges, the process variations become more pronounced leading to significant offsets in op-amps due to the device mismatch [1], [2]. In order to meet the gain requirements of op-amp in nanoscale CMOS processes and low supply voltage, three or higher stage op-amp topologies have become important. In this paper, we present a systematic design methodology for split-length compensated low-voltage three-stage op-amps.

II. Split Length Compensation

It is well known that if the compensation current from the output node is fed back to the internal nodes, using a current buffer structure, significant improvement in opamp performance can be achieved. These compensation methods give rise to left-half plane (LHP) zero, instead of a right half plane (RHP) zero (which degrades the phase), and thus enhance the phase margin [3]. In nano-CMOS processes low-voltage, high-speed op-amps can be designed by employing a split-length composite transistor for compensation instead of using a common-gate transistor in the cascode stack [4]. Fig. 1 illustrates the splitting of an n-channel MOSFET (NMOS) or a p-channel MOSFET (PMOS) to create a low impedance internal node-A [4].

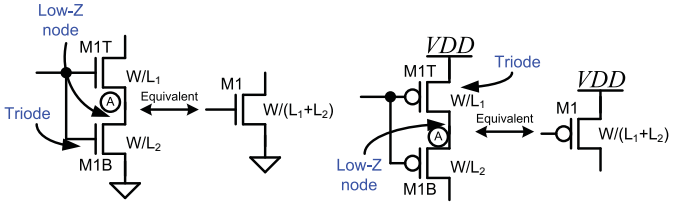

Figure 1. Illustration of the split-length NMOS and PMOS devices and the low-impedance nodes [4].

In two-stage op-amps employing split-length compensation, pole splitting is achieved with a lower value of the compensation capacitor (C_c) and with a lower value of second-stage transconductance (g_{m2}). This results in a much larger unity gain frequency (ω_{un}) attainable by the op-amp, with lower power consumption and a smaller layout, when compared to the Miller compensated op-amps [4].

III. Split length compensation of Three Stage Opamps

Continued interest in the three-stage op-amp design has seen numerous three-stage op-amp design techniques [5], [6], [7]. However, they exhibit either complex implementation or larger power consumption when compared to the commonly used two-stage op-amps. This section provides a tutorial on the design techniques, introduced by the author in [8], [9], which result in high-speed and low power three-stage op-amps.

A. Multi-Stage Op-amp Biasing

Biasing is an important concern when designing multi-stage op-amps. If all the gain stages of the multi-stage op-amp are not biased adequately with the intended overdrive voltages, the bias currents and hence the transconductances (g_m) and gains of the amplifying stages remain undefined. This may worsen the performance of the op-amp, consume larger current and can even render the op-amp unstable in closed loop. Consider

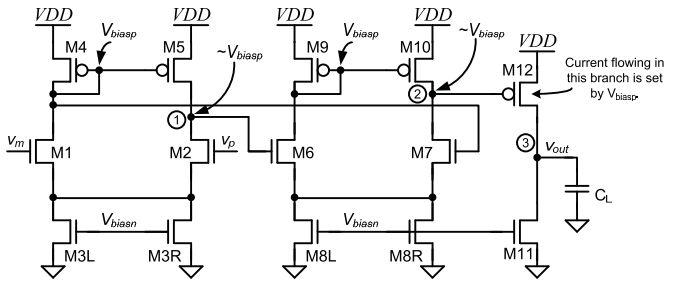

Figure 2. Biasing scheme for the three-stage op-amp, where all gain stages are biased properly with known bias currents flowing in all branches (compensation not shown here).

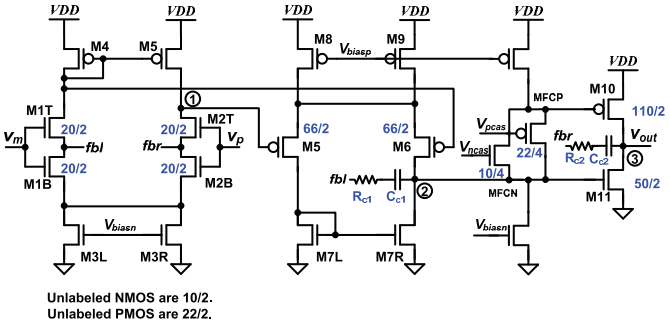

Figure 3. A low-power, pole-zero canceled, class-AB, three-stage op-amp.

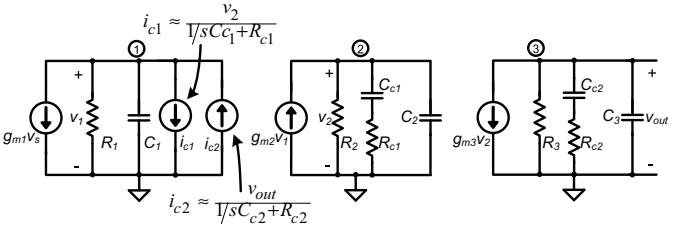

Figure 4. Small signal analytical model for the RSLC three-stage op-amp.

the three-stage op-amp topology illustrated in Fig. 2. Here diff-amps are used for the internal gain stages, both of which are biased with the same reference, V_{biasn}. In this topology, the voltage levels of the nodes 1 and 2 are set to be approximately equal to Vbiasp, due to symmetry in each of the diff-amps. Thus the bias currents in all the three gain stage branches are well defined, and their g_m's and the DC gains are precisely fixed. A diff-amp is not used in the last stage due to its limited output swing. Alternatively, if we had a common-source gain stage as the second stage in the op-amp, the drain voltage of transistors in second stage (node-2) will be set by the contention between the PMOS current source and the NMOS current sink. In this scenario, the voltage at node-2 will not bias correctly in the presence of large device mismatches.

B. Three-Stage Op-amp Compensation

The split-length compensation scheme is applied to three-stage op-amp design. A reversed nested compensation topology is used so that the output is not loaded by both of the compensation capacitors, which results in a larger unity gain frequency (ω_{un}). Fig. 3 shows a reverse-nested split-length compensated (RSLC), class-AB three-stage op-amp. A stack of maximum three transistors is used to realize the low-V_{DD} gain stages. In this topology an NMOS diff-amp is cascaded with a PMOS diff-amp which is followed by a class-AB output buffer. The PMOS diff-pair in second stage employs wider devices to increase the input common-mode range of the second stage. A split-length diff-pair (SLDP) is used for indirect compensation in order to achieve better supply noise isolation [8]. A diff-amp is employed in the second stage to ensure that the third stage is 'properly' biased by symmetry. The compensation capacitor C_{c_1} is used to feedback the compensation current i_{c_1} from the output of the second stage (node-2) to the output of the first stage (node-1) though a common gate current buffer. Similarly, capacitor C_{c_2} is used to feedback current i_{c_2} from node-3 to node-1. Here, the bias voltages $V_{pcas} = V_{DD} - 2V_{SG}$ and $V_{ncas} = 2V_{GS}$ are used to bias the floating current mirror. To ensure overall negative feedback in the circuit, the compensation capacitance must be connected across two nodes which move in opposite direction [8].

C. Small Signal Analysis and Pole-Zero Cancellation

The simplified small signal model for the RSLC three-stage op-amp is shown in Fig. 4. Here, g_{mc1} and g_{mc2} are the transconductances of transistor M2T and M1T respectively. R_{c_1} and R_{c_2} are the impedance attached to the nodes fbr and fbl respectively, which are both roughly equal to . Here, g_{mk} is the transconductance of the k^{th} gain stage while and C_k are the resistance and capacitance respectively, attached to the node-k in the op-amps (k =1, 2, 3). After applying nodal analysis to the small signal model shown in Fig. 4, the resulting transfer function can be written as [8].

$$H(s) \approx \frac{A_{OL}\left(1 + b_1 s + b_2 s^2\right)}{\left(1 + \frac{a_0}{a_1}s\right)\left(1 + \frac{a_2}{a_1}s + \frac{a_3}{a_1}s^2\right)\left(1 + \frac{a_4}{a_3}s + \frac{a_5}{a_3}s^2\right)} \tag{1}$$

The DC gain A_{OL} is equal to and the unity gain frequency is given as

$$\omega_{un} = \frac{g_{m1}}{C_{c_2}} \tag{2}$$

and the dominant pole is located at

$$\omega_{p_1} \approx \frac{1}{g_{m3}R_3 g_{m2}R_2 R_1 C_{c_2}} \tag{3}$$

The pole-zero cancellation leads to the following design criterion

$$R_{c_1} \approx \frac{C_L}{g_{m3}C_{c_2}}, R_{c_2} \approx \frac{C_{c_1}\left(C_L + C_{c_2}\right)}{g_{m3}C_{c_2}^2} \approx \frac{C_{c_1}}{C_{c2}}R_{c_1} \tag{4}$$

Note that the design equations are independent of the parasitic nodal resistance and capacitance values. The pole-zero cancellation leads to real pole-zero doublets located at [8] (see Fig. 5)

$$\omega_{p_2} = \omega_{z_1} \approx \frac{1}{R_{c_1}C_{c_1}} = \frac{g_{m3}C_{c_2}}{C_{c_1}C_L} \tag{5}$$

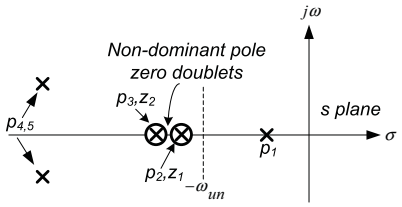

Figure 5. Pole-zero plot for a typical split-length compensated three-stage opamp.

$$\omega_{p_3} = \omega_{z_2} \approx \frac{1}{R_{c_2} C_{c_2}} = \frac{g_{m3} C_{c_2}}{C_{c_1}(C_L + C_{c_2})} = \frac{\omega_{p_2}}{1 + \frac{C_{c_2}}{C_L}} \quad (6)$$

From Eq. 5 and 6, we can see that the non-dominant pole-zero doublets appear close together in the frequency domain. The pole-zero doublets should be placed at a frequency higher than the ω_{un} of the op-amp, which results in the upper bound on ω_{un} [8]

$$\omega_{un} \leq \sqrt{\frac{g_{m1} g_{m3}}{C_{c_1} C_L}} \quad (7)$$

The location and quality factor of the parasitic conjugate poles due to the loading of nodes *fbl* and *fbr* are given by

$$\Re(\omega_{p_{4,5}}) \approx \frac{g_{m3} C_{c_2}}{C_L} \sqrt{\frac{g_{m2} R_2 C_{c_2}}{C_1 C_2 C_{c_1}}} \quad (8)$$

$$Q_{4,5} \approx \sqrt{\frac{g_{m2} R_2}{R_{c1} R_{c2}}} \left(\frac{1}{\frac{1}{R_1}\sqrt{\frac{C_1}{C_2}} + \frac{1}{R_2}\sqrt{\frac{C_2}{C_1}}} \right) \quad (9)$$

The mirror poles in the diff-amps are located at a higher frequency than the poles $\omega_{p_{1-5}}$. The phase margin for the opamp can be approximated as

$$\phi_M \approx 90^\circ - tan^{-1} \left(\frac{\frac{\omega_{un}}{Q_{4,5}}}{1 - \left(\frac{\omega_{un}}{\omega_{4,5}}\right)^2} \right) \quad (10)$$

It can be observed that the location of the parasitic poles and hence the phase margin is dependent upon the choice of open-loop gain in the second stage. The slew-rate for these opamps can be estimated as $min\left(\frac{I_{SS_1}}{C_{c_1}}, \frac{I_{SS_2}}{C_{c_2}}\right)$, where I_{ss_k} are the diff-amp tail currents. A detailed comparison of the RSLC opamps with the prior literature is provided in [8], [9].

IV. Design Procedure

The design of three-stage opamp using split-length compensation can be seen as a non-linear optimization of multiple variables. We present an iterative design procedure to meet desired set of specifications:

1) Start with initial specification of ω_{un}, A_{OL}, C_L and SR.
2) Distribute DC gain, A_{OL}, across the stages as A_1, A_2 and A_3 (where $A_k = g_{m_k} r_{o_k}$)
3) Select the overdrive which will set V_{GS}, f_T and $g_m r_o$.
4) Select a value for g_{m1}. Select g_{m2} for the desired phase margin (PM) (Eq. 8,9).
5) Select $C_{c_2} = \frac{g_{m1}}{\omega_{un}}$ (Eq. 2).
6) Select C_{c_1} and g_{m3} such that the pole-zero doublet locations are outside ω_{un} (Eq. 5,6).
7) Calculate R_{1c} and R_{2c} (Eq. 4).
8) If either of R_{1c} or R_{2c} is negative (not realizable), move the corresponding pole-zero doublet to a lower frequency by changing the corresponding C_{c_k} and R_{c_k}. Here, ω_{un} may need to be reduced. Go to step 4.
9) Simulate the design for frequency response and transient settling. If the phase margin (ϕ_M) needs to be increased, go to step 4.
10) Verify if the design meets desired specifications. If not, modify the design using the following steps and go back to step 2.
    a) Settling speed can be increased by increasing g_{m1} or decreasing C_{c_2}.
    b) Power can be reduced by decreasing g_{m3} or g_{m2} .
    c) Layout area can be reduced by decreasing C_{c_1} , C_{c_2} or g_{m3}.
    d) Slew-rate (SR) can be improved by increasing the bias current in the first stage or by using smaller C_c's.

In order to simplify the design procedure, a MATLAB based toolkit has been developed [10]. The scripts in the toolkit use small-signal parameters of the transistors and the parasitic capacitances as input data to assist in design and pole-zero compensation of the three-stage opamps. Fig. 6illustrates the frequency response of a RSLC three-stage opamp designed for 67°phase-margin.

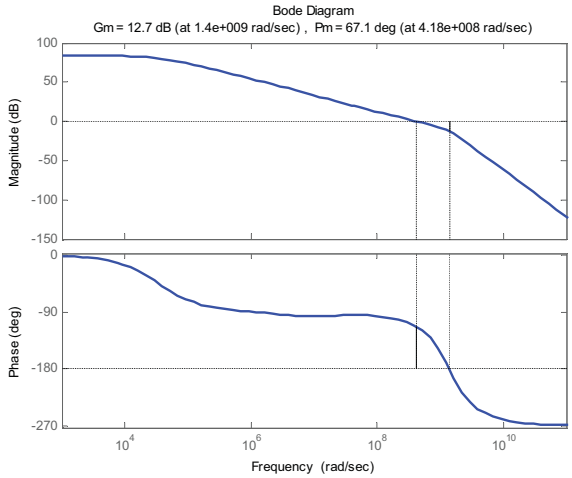

Figure 6. Bode plot for the RSLC three-stage opamp design.

The script also enables greater insight into the stability of multi-pole and zero system using Nyquist stability plot (see Fig. 7). Nyquist stability criterion captures the rich closed-loop dynamics of the three-stage opamps, especially when uncanceled LHP zeros are located, which lead to transient settling artifacts not captured by the Bode plot.

V. Fully-Differential Three-Stage Opamps

Fully-differential (FD), three-stage op-amps can be implemented by extending the design techniques presented in

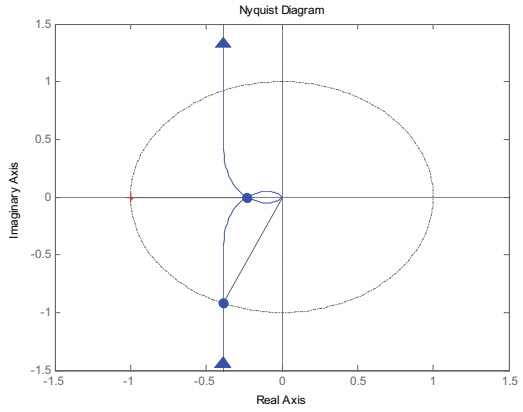

Figure 7. Nyquist stability plot for a RSLC three-stage opamp design. Here the phase margin (ϕ_M) can be observed to be 67°.

Section IV. A FD op-amp requires the output common mode level to be balanced by a common-mode feedback (CMFB) loop. The first topology in the logical sequence is the one with a single CMFB loop around all the three stages. Topologies based upon this block diagram have been proposed in [11], [12], [13]. However, it is observed that the CMFB loop disturbs the biasing of the second and third stages as the common mode levels at node-1 and node-2 vary widely. Additionally, such such topologies exhibit start-up problems. A robust three-stage opamp has individual CMFB loops for all the stages. However, it must be ensured that the common-mode sensing circuitry does not load the internal gain stages. Fig. 8 shows the schematic of a fully-differential implementation of the split-length compensated three-stage opamp. CMFB loops are employed in each of the gain stages. In the output stage, resistive common-mode sensing is used to ensure that the CMFB loop can operate for large output swings. The current in the PMOS device in the class-AB output buffer is lower than that in the NMOS in order to avoid the scenario, where the negative output impedance from the PMOS buffer circuitry, might lead to instability [14].

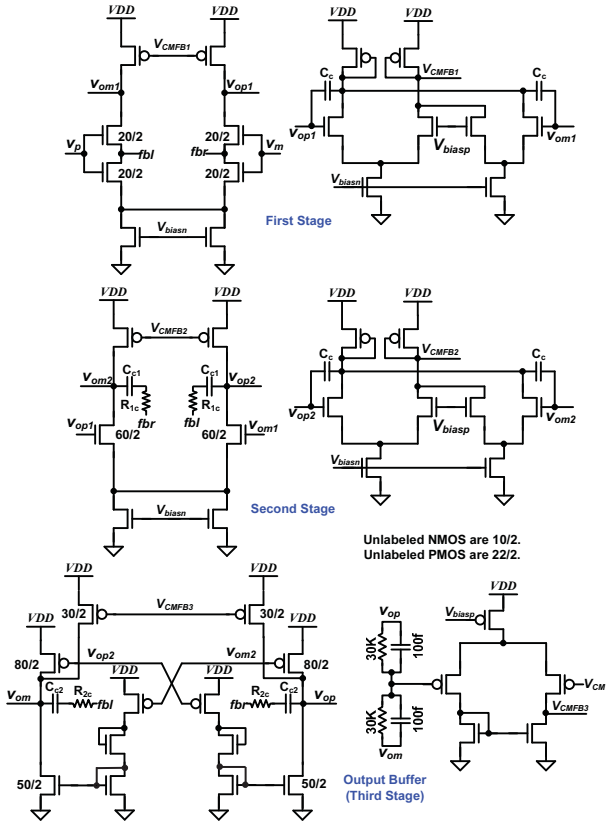

Figure 8. Fully-differential implementation of the split-length compensated three-stage op-amp along with the common-mode feedback circuits for each of the gain stages.

VI. Conclusion

A methodology has been presented to design split-length compensated (RSLC) three-stage op-amps suitable for low-voltage nano-CMOS technology. A toolkit has been created and made available to simplify the compensation procedure for three-stage opamps and for understanding the dynamics of multi-pole and zero opamp systems. The op-amps exhibit large DC gain, and settling as fast as a corresponding two-stage amplifier, with minimal excess power consumption and smaller layout area. The fully-differential, three-stage, RSLC op-amps presented in this work are low-voltage, offset tolerant and suitable for design in nano-CMOS technologies.

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