A Non-Volatile Memory Array Based on Nano-Ionic Conductive Bridge Memristors

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***Abstract*—Much excitement has been generated over the potential uses of chalcogenide glasses and other materials in circuits as "memristors" or as non-volatile memories. The memristor is a fourth passive two terminal electronic device, postulated by Leon Chua in 1971 and rediscovered in 2008. Our Conductive Bridge Memristor (CBM) changes its resistance in response to current passing through it by building up or dissolving a conductive molecular bridge in an otherwise insulating chalcogenide film.**

This paper outlines the design and simulation of a non-volatile memory using an array of CBM devices integrated with CMOS access transistors and read/write access circuitry.

We have designed and simulated a large memory array layout using CBM devices accessed by an NMOS transistor and CMOS row/column read and write drivers. The design uses a folded-cascode op-amp configured to integrate current on the column as a strategy for sensing the device resistance. Each CBM device is connected to the array through a single minimum size NMOS transistor. The design has been simulated using a SPICE model for the PMC (Programmable Metallization Cell) [7]. We demonstrate the feasibility of accessing the device for read without exceeding the write threshold, and discuss the tradeoff of speed vs. array size associated with this technique. Plans are being developed to fabricate the design on a MOSIS multi project wafer with BEOL processing for the CBM devices.

***Keywords* — Chalcogenide, Memristor, Non-Volatile Memory, Scaling.**

I. INTRODUCTION

THE Conductive Bridge Memristor (CBM) is a metal-dielectric-metal sandwich having a glassy material through which metal atoms may migrate under an electric field, eventually creating a conductive path. The effect is reversible and nonvolatile, meaning the effect does not dissipate after power is removed and the device may retain its state for long periods of time. Reversal of the conductive path is done by reversing the electric field. This non-volatility is the great advantage of which research on the device hopes to take benefit .

In 1971, Leon Chua described a new two-terminal circuit element called the memristor, characterized by a relationship between charge and flux-linkage [1]. He introduced the Memristor as a fourth basic circuit element, then showed that this element explains some peculiar behaviors seen to differ from those exhibited by resistors, inductors, or capacitors. He believed the properties of a Memristor would lead to a number of unique applications which could not be realized with networks of traditional passive components.

Chua's work was lost in obscurity until in 2008, researchers in HP Labs [2] popularized the work when they used the paper and the term Memristor to describe a new technology for future scalable memory using TiO_2 based devices at the 50 nanometer scale. They claimed that while memristive effects had been seen in various nanoscale research, they had never been well explained until HP found and applied Chua's formulation. It also appears to be a requirement that we work at the nanoscale to make an effective Memristor [2].

In work predating the HP revelation, two-terminal devices later dubbed Programmable Metallization Cells (PMC) were developed at Arizona State University (ASU) by Michael Kozicki, Maria Mitkova, and others [3] [4]. The PMC consisted of Chalcogenide glass sandwiched between metal layers. A related device using similar chalcogenide material but having a different physical mechanism is the Phase Change Memory (PCM) [5]. A good paper discussing a variety of future scalable memory technologies is presented by Roberto Bez [6].

II. A CBM MEMORY ARRAY

In this discussion we will use the term PMC as the term for the ASU developed SPICE model of the Memristor [7]. This model should be a good approximation of the Chalcogenide CBM we intend to build.

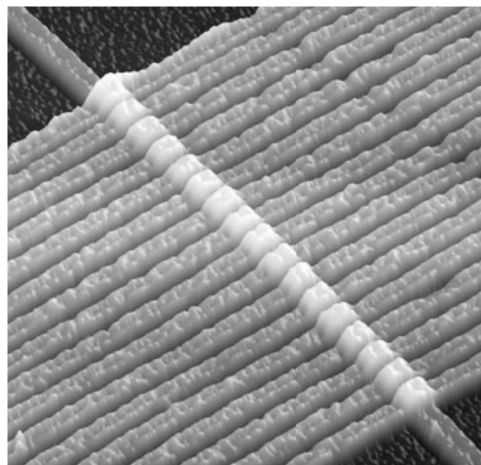

Figure 1 HP Labs TiO_2 Memristor Crossbar [2]

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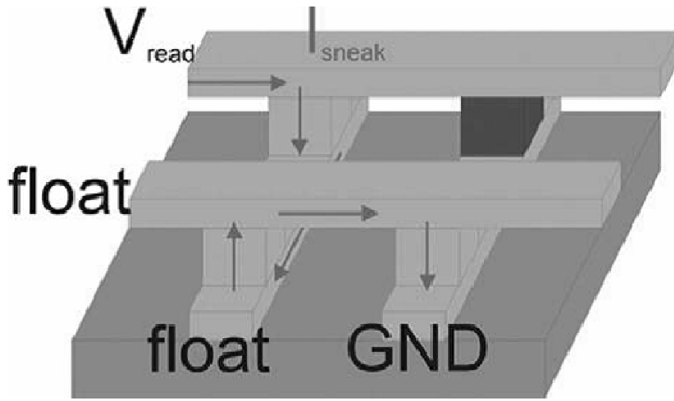

Figure 2 Sneak Path Problem in Resistive Memory [8]

The first problem to overcome with a memory array of resistive devices is the sneak path problem [8]. Sneak path refers to conduction paths other than the path through the resistor connecting the selected row and column. In Fig. 2 we see the intended signal path through the darker vertical connection bypassed by one of the many possible sneak paths marked by arrows. If the intended read path is in a high resistance state, but three devices in any sneak path are low resistance, the output voltage could be falsely read.

In addition to the sneak paths, there is the problem that a resistive array will draw a widely varying overall power depending on the number of resistors in the low resistance state [9]. This can become costly for both the power regulator and the cooling system.

We have chosen to solve both problems with a row access transistor for every bit. This choice gives us freedom from worry about the large range of resistances offered by various forms of memristive devices. Typical reports show 5 or more orders of magnitude between on and off state resistances.

A. *CBM Threshold*

One of the problems with using a CBM as a memory is that the devices studied so far have a very low voltage threshold of operation, on the order of 200mV to turn the device "ON" meaning having low resistance; and an even lower reverse threshold of about -50mV at which the PMC regains its high resistance as the metal atoms which form the conductive path migrate back toward the metal plate. We use a differential amplifier circuit with good discrimination for small changes in voltage to use as the sense amplifier for our memory column.

A CMOS differential amplifier is not effective near the voltage rails (VDD and GND), so we operate with a bias above the ground rail, called Vbias. In these simulations, VDD is 5V, Vbias is 1V, and GND is 0V. For programming, another reference of twice Vbias or 2V is also required.

Our layout and device parameters are from the ON Semiconductor C5 process (0.5micron transistor L, 0.3micron λ). Our simulator is LTspice IV.

B. *Bit Cell*

The memory bit as shown in Figs. 3, and 4 connects the column line to our PMC cathode through a row access transistor. The anode of the PMC contacts a common top plate which is held to a reference voltage. We can program any bit in the array by driving the bit's column to GND or VDD with the common top plate held at Vbias. When the bit's row is activated, the access transistor is opened, creating a positive or negative 1V potential across the PMC, sufficient to write the device to an on or off state respectively.

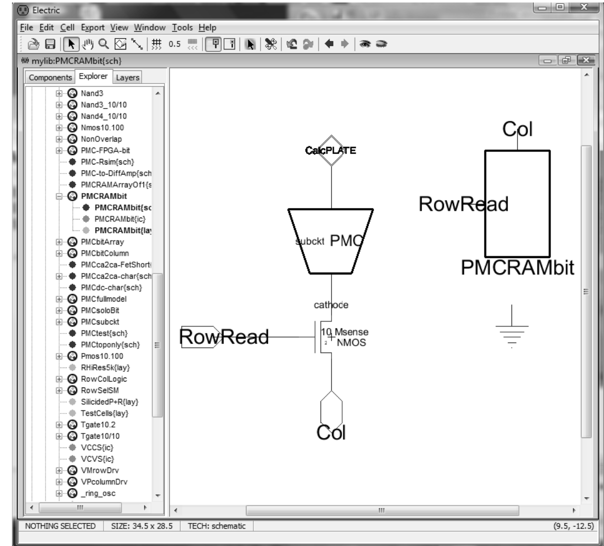

Figure 3 PMC Model and Row Access Transistor

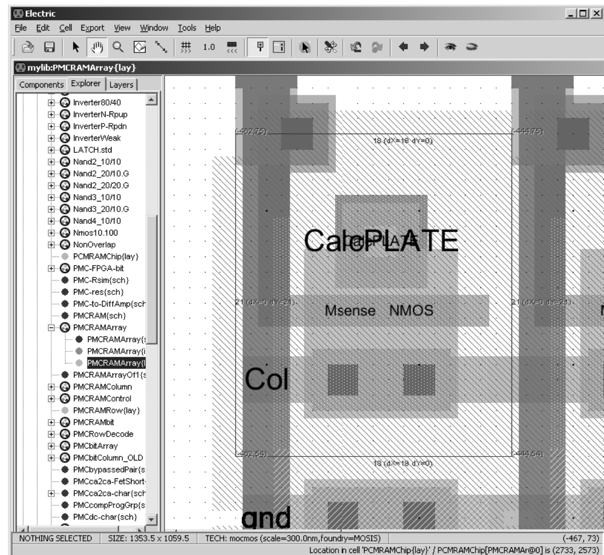

Figure 4 Memory Bit Layout

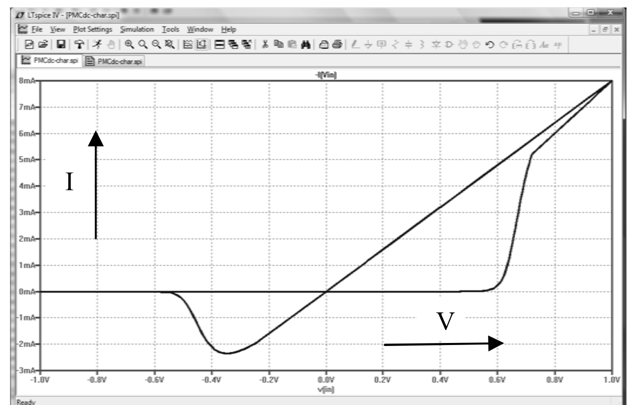

Figure 5 PMC SPICE Model I-V Curve

C. Write Block

At the head of each column is a write block having three transistors to control writing data into the PMC by switching one of three voltages onto the column. The signals described here are shown in Fig. 7. When the Prog signal is high, the column is driven to ground, which presents positive 1V across the PMC. This is above the threshold needed to turn the bit on after about 250ns. When Erase is high, the column is driven to 2V or twice the common bias voltage of 1V. This creates negative 1V across the PMC, which quickly turns the device off. The signal Keep is used to hold a Vbias level on the column for read operation.

D. Column Sense Amp

The column sense amp circuit shown in Fig. 6 is an integrator design containing an operational amplifier and feedback capacitor is configured to integrate the input voltage. This configuration converts a sense pulse at the feedback transistor gate into a voltage ramp with slope equal to I/C where I is current supplied by the selected PMC device and C is the feedback capacitance. With the appropriate timing on the row access transistor we can determine whether the PMC is on or off without exceeding the devices thresholds. The output of the integrator ramps upward steeply if the bit is on, and a high is trapped in a latch. If the bit is off, a low is recorded.

E. Simulation

The simulation in Fig. 8 shows the column sensing two preprogrammed PMC devices, one in high resistance state, and the other in low resistance. The traces labeled Col 0 and Col 1 show column sense amp output, while the traces labeled Out 0 and Out 1 show the latched output for each column. Clearly we are able to sense and latch a binary value for the small (8x8) array layout simulated here. We have also shown the ability to read and write the memory in the presence of the equivalent parasitic row and column line resistance and capacitance of much larger arrays, and at a significantly faster speed than has been reported for other memristive memories.

F. Memory Array Limits

This design is not limited by the change in resistance, as long as it is sufficiently large for discrimination. Rather, the limits will be parasitic delays which increase access time, and the Area-Yield constraint. These are the same limits as for conventional memories; however, we believe these devices to be capable of scaling down much smaller than conventional solid state memory. The CBM is actually expected to improve with continued downward scaling as nanoscale effects are understood and exploited. By connecting a contact-size CBM with a transistor the same size of a 1T DRAM (one-transistor per bit dynamic memory) transistor, we imagine a scaling benefit over the capacitor based 1T DRAM bit cell.

III. CBM APPLICATIONS

A. Scalable Memory

A significant reason there has been so much recent research into these devices is the desire to continue scaling solid state memory past the limits of the current 1-transistor, capacitive cell DRAM. Heroic efforts have been made to continue scaling both the capacitor and access transistor, but it appears the limit may be reached at or near the 25 nanometer node.

There is grave concern that very soon after that technology node, lithography capability will exceed the physical ability of the memory to function. Costs may increase as increasing effort is required to continue scaling conventional memory due to the physical limitations.

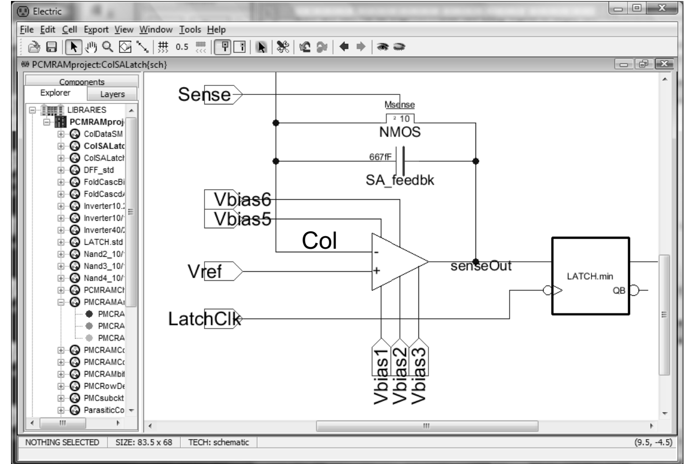

Figure 6 Column Sense Amp Circuit

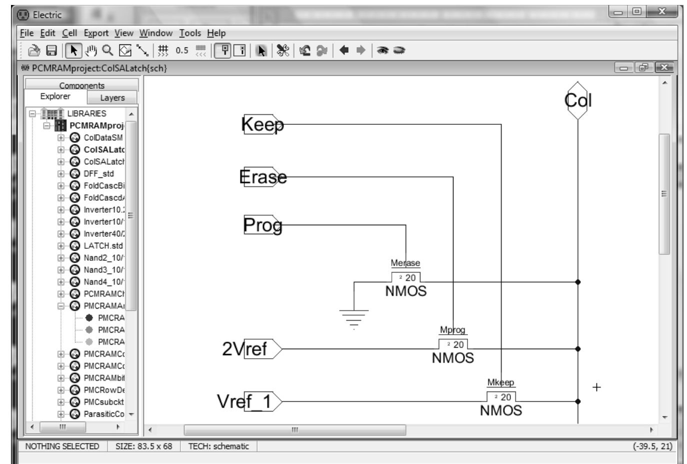

Figure 7 Column Write Block

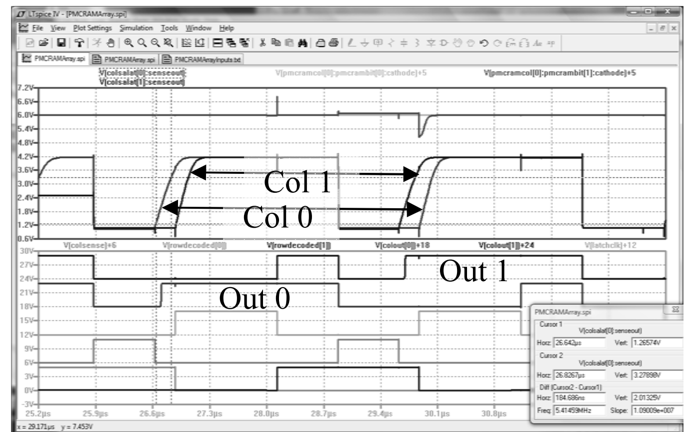

Figure 8 Column Simulation

B. 3D, Back End of Line Memory

The CBM and similar technologies present the possibility of integrating memory cells into the metallization structure of device connections. We note that a memory bit could be substituted in place of a standard metal via in about the same area [8]. Arrays of such bits would be limited only by the metal pitch of the lines to access them, and there is no reason to limit the devices to a single via layer. Transistors on the base silicon layer would not be affected and could be independent of the memory.

The memory could extend upward in the 3rd dimension as far as the technology allows. This appears quite achievable, because the Memristor devices are created with low temperature processes. However, accessing 3D stacked memory bits in a general random logic design, such as for an SoC (system on chip), remains an ambitious exercise.

C. Dense FPGA

FPGAs (Field Programmable Gate Arrays) are becoming very popular both as a prototyping tool and as a short production run solution. The economy of designing and tooling new mask sets for an ASIC are making the volume requirements for a single design very large. FPGAs avoid much of the NRE cost for small volume products. Furthermore, if a product becomes unexpectedly popular, there are companies which specialize in “conversions” of the FPGA design to ASIC form. A dense integration of memory and logic is the greatest need for economical FPGA design.

D. Nonvolatile Memory

A memory which is nonvolatile in addition to these other benefits enables new applications, architectures, and design strategies stretching out into the future.

IV. Future Directions

A. Memory Progress

Memory has progressed from threaded magnetic cores to drums and disks to solid state, but we still rely on the magnetics for non-volatility. In fact we think we have progressed, but it might look like digression the way we over complicate our processors with multiple levels of cache attempting to speed the access to ever slower (compared to CPU clock speed) storage media. A proximate memory which scales sufficiently to match the associated processor seems a bit overdue.

B. Hardware Design Tool Progress

Having graduated from using pencil and slide rule to calculator to CAD to CAE, we are now using genetic algorithms and evolutionary programming to search design spaces. Reconfigurable hardware enables machines which adapt to their environment and circumstances. The processing requirements are huge, and the memory demands as well. The future will routinely expect multiprocessor machines with large numbers of processors each with sufficient memory in close proximity. Such machines should not require modification by human hands, but will learn and adapt according to the momentary need.

C. Future Architectures

As our experience with memristor designs grows and matures, we might expect entirely novel architectures to emerge. One direction is particularly exciting. From the beginning, researchers have compared the memristor function to that of the neural synapse. One recent paper gives results from a heterogeneous design involving memristors as synapses and CMOS circuits for neural summing and output [11]. Another discusses difficulty with a single memristor and proposes a more complex design for a multi-memristor synapse [12]. We believe such research is the beginning of a new and exciting computational architecture which will be able to learn from its environment rather than require detailed human programming.

Acknowledgement: This work was supported under SMI grant contract number 41846, AF Prime Contract Number: FA9550-10-C-0075

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