

# A 2 GHz Effective Sampling Frequency K-Delta-1-Sigma Analog-to-Digital Converter

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**Abstract**— As CMOS technology scales to nanometer dimensions, analog-to-digital converter (ADC) design has become increasingly more challenging. This is mainly due to the increased transistor leakage currents, process variations, and poor matching. The K-Delta-1-Sigma (KD1S) modulator was proposed as a practical solution for designing high-speed ADCs in nanometer CMOS processes. This paper presents an 8-path KD1S modulator with an effective sampling frequency of 2 GHz derived from a 250 MHz input clock. The simulation results confirm the true first-order noise shaping of the modulator. The simulated SNR is 44.95 dB and the simulated SNDR is 44.41 dB corresponding to  $N_{eff} = 7.17$  bits with a conversion bandwidth of 15.625 MHz.

**Keywords**— analog-to-digital converter; wideband ADC; K-delta-1-sigma ADC; delta-sigma modulation; time-interleaved data converters; noise shaping.

## I. INTRODUCTION

An increased number of wideband wireless communication standards and well-advanced optical communications have put stringent requirements on the speed, resolution, and power consumption of analog-to-digital converters [1]-[2]. Nyquist-rate ADCs like the Pipeline and Flash architectures have been used in high-speed applications where resolution is less important than conversion rate. Compared to the Flash ADCs that operate with data conversion rates of 100's of MHz with relatively low resolution (up to 8 bits), Pipeline ADCs provide higher resolution (10-14 bits) over a range of 100 - 500 MHz [3]. However, along with the technology scaling pipelined ADCs suffer from the notable performance degradation which is mainly due to process variations and poor component matching. Therefore, designing high-resolution pipelined ADCs using nanometer processes calls for an extensive amount of digital calibration at the cost of increased area, latency, and power consumption [4]. Thus, pipelined ADCs and calibration techniques have become less useful with CMOS technology scaling.

Investigating other ADC topologies which are inherently tolerant to device mismatches and nonlinearity is becoming more and more interesting. Two of these popular topologies, conventional and time-interleaved delta-sigma converters, are discussed in Sec. II. Section III contains a brief review of discrete-time KD1S topology [5]. In section IV a new CT-

KD1S topology is proposed and discussed in detail followed by the simulation results in Sec. V. Finally, Sec. VI provides concluding remarks.

## II. CONVENTIONAL AND TIME-INTERLEAVED DELTA-SIGMA MODULATORS

### A. Conventional Delta-Sigma Modulators

Delta-sigma ADCs, also known as oversampling ADCs, are a very popular choice for analog-to-digital conversion [6]. Compared to Nyquist-rate ADCs, delta-sigma ADCs are able to achieve much higher resolution, commonly given in terms of signal-to-noise ratio (SNR), for relatively less conversion bandwidth. A block diagram of a conventional first-order delta-sigma modulator is shown in Fig. 1.

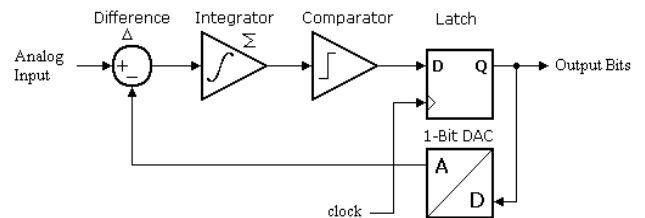


Fig. 1. Block diagram of the first-order delta-sigma ADC.

A delta-sigma ADC constitutes of a noise-shaping modulator (NSM) followed by digital filters and decimation stages [7]. The modulator makes use of oversampling, i.e. the sampling frequency is a multiple of the Nyquist rate. Oversampling ratio (OSR) is therefore defined to be:

$$OSR = f_s / (2 \cdot BW) \quad (1)$$

The NSM moves the quantization noise,  $Q_e$ , to frequencies outside the baseband. Therefore the amount of in-band quantization noise is decreased. Afterward the modulated out-band noise is digitally filtered to achieve an increase in the signal-to-noise ratio (SNR). Using NSM much of the analog signal processing is transferred to the digital domain which is favorable for the continued CMOS technology scaling. Also, the use of a 1-bit comparator and digital-to-analog converter (DAC) results in good linearity.

Because of the high loop gain in the forward path (at low frequencies), NSMs are almost insensitive to device mismatches and nonlinearities which is again a very interesting and useful feature when using nanometer CMOS processes. Due to the feedback desensitization of the loop the requirements for the comparator is also much more relaxed. The op-amp's dc gain requirements is also less challenging and can be set to be as low as the *OSR* value. The drawback of using NSMs is that the signal bandwidth is limited due to the oversampling and therefore conventional delta-sigma ADCs are narrowband.

### B. Time-Interleaved Delta-Sigma Modulators

Another way of increasing the resolution and effective sampling rate is to simply put  $K$  ADCs in parallel where each of the ADCs operates at a rate of  $f_s$  and therefore the effective sampling rate is  $K \cdot f_s$ . This technique, which uses non-overlapping clocks for parallel paths, is called time-interleaving. The ADCs used in slow parallel paths can be either Nyquist-rate or delta-sigma ADCs. Using Nyquist rate ADCs, we will face the same issues discussed in Sec. I. Therefore much effort has been applied towards time-interleaving to delta-sigma modulators (DSMs) [8]-[12]. The time-interleaved topology using parallel DSMs is shown in Fig. 2. This technique does not provide a notable increase in resolution (only 0.5 bits per doubling the number of paths). This topology is discussed in detail in [5]. This technique also does not result in true noise-shaping when using  $K$  parallel DSMs.

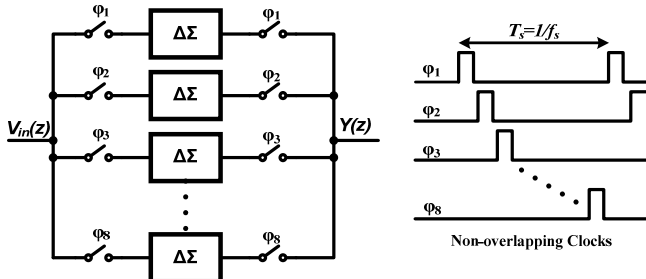


Fig. 2. A time-interleaved or parallel delta-sigma modulator [5].

### III. THE K-DELTA-1-SIGMA (KD1S) MODULATOR

In order to achieve true noise-shaping with interleaving of delta-sigma modulators the forward path of the topology can be shared while the feedback paths are interleaved [7]. Ideally, each of the paths has to settle within a  $T_s/K$  time interval. The block diagram of the previously proposed switched-capacitor KD1S ADC [5] as well as the corresponding clock signals are shown in Fig. 3. As it is seen in the figure the discrete-time KD1S ADC includes  $K$  comparators (8 in this case), switched-capacitor circuitry and a shared integrator. There are  $K$  different clock non-overlapping phases as shown in the Fig. 3 and the time interval between rising edges of any two adjacent clock phases sets the effective sampling of the KD1S ADC:

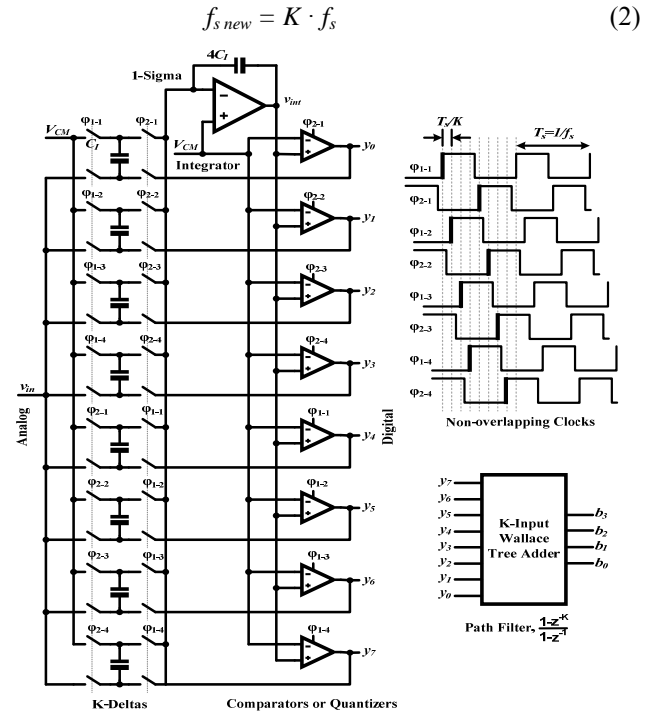


Fig. 1. The  $K$ -Delta-1-Sigma modulator topology [7].

Using an adder to sum up the parallel  $K$ -path outputs has the decimation filter response of:

$$F_{dec}(z) = (1 - z^{-K}) / (1 - z^{-1}) \quad (3)$$

The output of the shared integrator is connected to  $K/2$  paths at any time instant which means the output spreads the sampled signal across  $K/2$  paths at any time. The mismatches and non-idealities in the forward path are averaged out through the  $K$  paths. However, the non-ideality or mismatches in the feedback paths has to be more precise since they add directly with the input signal.

Ideally the comparators fully respond to the partial settling of the integrator's output in the time interval of  $K/2$ . In this case the true first-order noise shaping is feasible and the noise transfer function (NTF) of the KD1S modulator is given by:

$$NTF(f) = 2 \sin(2\pi f / Kf_s) \quad (4)$$

Noise-shaping for both time-interleaved and KD1S modulators is seen in Fig. 4. As shown in this figure, the noise shaping for a time-interleaved DSM does not gain (much) from having  $K$  parallel DSMs. However, the KD1S topology pushes the quantization noise out to higher frequencies. The result is that the KD1S topology acts like a single path clocked at  $f_s$ .

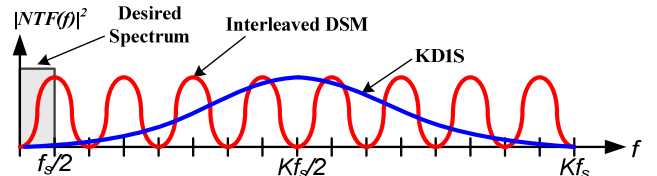


Fig. 4. True wideband noise-shaping using a  $K$ -Delta-1-Sigma Modulator.

#### IV. CONTINUOUS-TIME K-DELTA-1-SIGMA MODULATOR

The continuous-time (CT) version of the KD1S modulator is seen in figure 5. The switched-capacitor circuitry has been replaced by an active RC integrator with resistive feedback. CT-KD1S has the same noise-shaping properties discussed in the previous section while also presenting a couple of advantages compared to a switched-capacitor KD1S implementation. The main advantages of CT-KD1S compared to DT-KD1S are low power consumption, inherent anti-aliasing filter (AAF), relaxed bandwidth requirement for the integrator and resistive input impedance. The main drawback of the CT-KD1S occurs because each path is feeding information the entire time,  $T_s$ , rather than, ideally just during the  $T_s/K$  time slice.

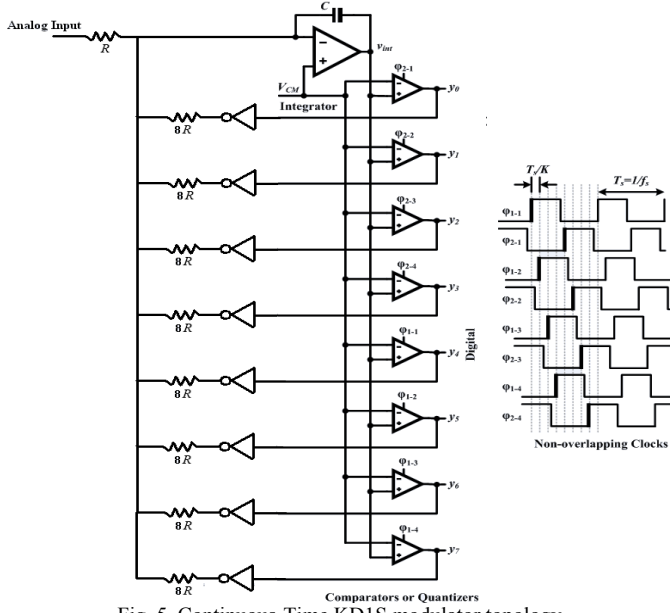


Fig. 5. Continuous-Time KD1S modulator topology

In this implementation the comparator is clocked on the rising edge of the clock, every  $T_s = 1/f_s$ . Each comparator output is then fed back to the integrator summing node and held there for the entire clock period. The size of the integrating capacitor is set relatively small so that the op-amp can drive it quickly. The input resistor value is set by the integrating time constant that would be chosen to be some multiple of  $T_{s\ new} = 1/f_{s\ new}$  [7]. The value of the feedback resistors is therefore  $R_{fb} = K_{path} \cdot R$  such that in parallel they are equal to the input resistor.

There are a couple of drawbacks to using CT-KD1S, such as greater sensitivity to RC time-constant variations, and more stringent requirements on comparators' jitter and settling time performance. Feeding back the comparators' outputs to the integrator summing node for the whole clock period increases distortion since the integrator output would be adjusted based on old information from each comparator relative to the input. Therefore by increasing the feedback duration the distortion increases which results in degradation of the signal to noise and distortion ratio (SNDR) and hence the modulator performance. It is shown in Fig. 6 how the third-order harmonic distortion

(HD3) term goes up with increasing the feedback duration and therefore the effective number of bits ( $N_{eff}$ ) decreases. The clock period of each path of the modulator used to generate Fig. 6 is  $T_s = 3\text{ns}$ . Therefore, one way to increase the performance of CT-KD1S modulator would be to decrease the feedback duration by adding switches to the feedback paths. However, this may not be a desirable solution due to tougher settling-time requirements and hence increase in the op-amp's power consumption.

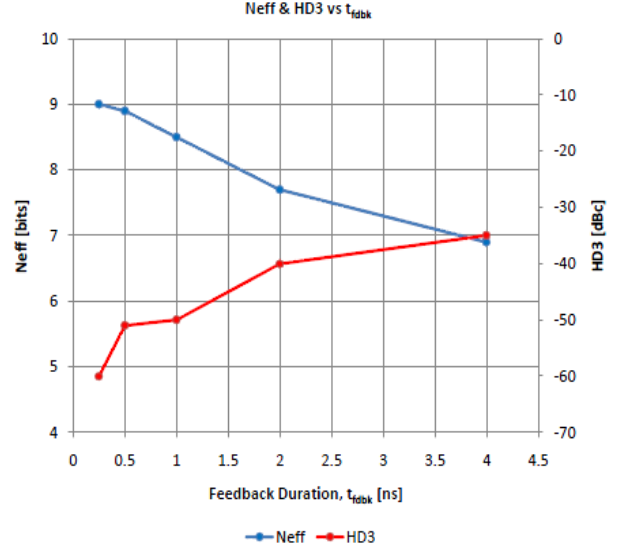


Fig. 6. CT-KD1S performance versus feedback duration.

One way to overcome the jitter problem is to retime the comparators' outputs. The problem with this approach is that any block added after the comparator will add more delay to the feedback path, hence degrading the modulator performance.

Therefore, to enhance the jitter performance we should think of a way to change the feedback signal from a timing-dependent signal to a timing-insensitive signal. The proposed method in this paper is to replace the feedback resistors with a switched-capacitor network shown in Fig. 7.

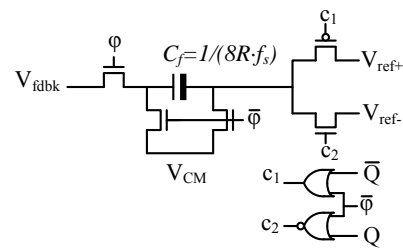


Fig. 7. The proposed non-delaying switched-capacitor network as a substitute for feedback resistors.

The logic in Fig. 7 guarantees proper operation of the switches. On the positive clock phase, the same phase as the comparator changes state, the series switches are ON. The comparator output, Q, determines if  $V_{ref+}$  or  $V_{ref-}$  is connected to the capacitor.  $V_{ref+}$  and  $V_{ref-}$  could be simply VDD and ground respectively in one implementation. Secondly, on the negative clock phase, the series switches are

open and the shunt switches connect both plates of the capacitor to the input signal common-mode, hence discharging the capacitor and erasing the previous feedback information. The only requirement is that the comparator make a decision and the integrator output settle both within half the clock period,  $T_s$ . Using this method, the modulator performance is improved compared with the resistive approach for a feedback duration of half the clock period.

## V. SIMULATION RESULTS

In order to evaluate the performance of the proposed topology in 50 nm CMOS technology, the transistor level design of the KD1S ADC with eight paths has been simulated using the LTspice simulation program. The modulator's outputs are analyzed and processed in MATLAB. The eight outputs were sequentially accessed for an equivalent 1-bit output. A sinusoidal input signal with an amplitude of 800 mV<sub>pp</sub> is applied ( $VDD = 1$  V) at a frequency of  $f_{in} = 3.54$  MHz. The conversion bandwidth is 15.625 MHz and the OSR is 64. Every path is clocked at a rate of  $f_s = 250$  MHz such that the new ADC effective sampling rate is  $f_{s,new} = 2$  GHz, the equivalent 1-bit output changes every 500 ps.

The time-domain simulation results, the equivalent 1-bit output and input, are shown in Fig. 8. The transient analysis lasted 8.129  $\mu$ s. and the frequency spectrum analysis has been done using FFT points of  $2^{14} = 16384$ . The corresponding modulator output spectrum is shown in Fig. 9.

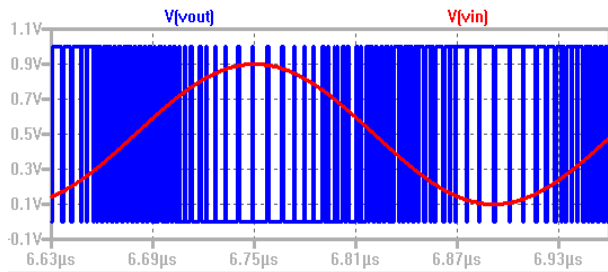


Fig. 8. Time-domain simulation result for the proposed CT-KD1S topology.

It's interesting to note in Fig. 9 how the first-order noise shaping is very well established. The simulated SNR is 44.95 dB and the simulated SNDR is 44.41 dB corresponding to  $N_{eff} = 7.17$  bits.

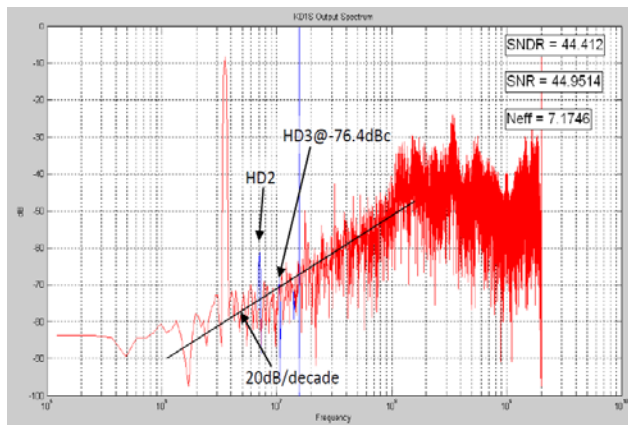


Fig. 9. The modulator output spectrum corresponding to output in figure 8.

## VI. CONCLUSION

The proposed KD1S modulator presents a wideband true first-order noise shaping. The modulator sensitivity to the input dependent comparator delay has been decreased and therefore the modulator is robust to jitter which is the main difficulty for designing any high-speed ADC.

## REFERENCES

- [1] Razavi, B., Aytur, T., Lam, C., Yang, F.-R., Yan, R.-H., Kang, H.-C., Hsu, C.-C., and Lee, C.-C. "Multiband UWB transceivers," Proc. IEEE Custom Integrated Circuits Conference, pp. 141-148, Sept 2005.
- [2] Floyd, B. et al, "Silicon Millimeter-Wave Radio Circuits at 60-100 GHz," IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 213-218, Jan. 2007.
- [3] Gustavsson, M., Wikner, J. J., and Tan, N. N., "CMOS Data Converters for Communications," 1st Ed., Kluwer, 2002.
- [4] Verma, A., Razavi, B., "A 10b 500MHz 55mW CMOS ADC," International Solid-State Circuits Conference, pp. 84-86, Feb. 2009.
- [5] Saxena, V.; Baker, R.J., "A K-Delta-1-Sigma Modulator for Wideband Analog to Digital Conversion," Proc. 53<sup>rd</sup> IEEE international Midwest symposium on circuits and systems (MWSCAS), pp. 1029-1032, Aug. 2010.
- [6] Lee, C. C.; Flynn, M. P. , "A 14 b 23 MS/s 48 mW Resetting sigma-delta ADC," IEEE Trans. on Circuits and Systems – I: Regular papers. pp. 1-11, Jan. 2011.
- [7] Baker, R.J., "CMOS: Mixed-Signal Circuit Design," 2nd Ed., Wiley-IEEE, 2008. Website: <http://CMOSedu.com>
- [8] I. Galton and H. T. Jensen, "Oversampling Parallel Delta-Sigma Modulator A/D Conversion," IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing, Vol. 43, No. 12, pp. 801-810, Dec. 1996.
- [9] R. Khoini-Poorfard, L. B. Lim, and D. A. Johns, "Time-Interleaved Oversampling A/D Converters: Theory and Practice," IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing, Vol. 45, No. 8, pp. 634-645, August 1997.
- [10] E. T. King, A. Eshraghi, I. Galton, T. S. Fiez, "A Nyquist-Rate Delta-Sigma A/D Converter," IEEE Journal of Solid-State Circuits, vol. 33, no. 1, pp. 45-52, Jan. 1998.
- [11] A. Eshraghi, T. S. Fiez, "A Time-Interleaved Parallel  $\Delta\Sigma$  A/D Converter," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 50, no. 3, Mar. 2003.
- [12] A. Eshraghi, T. S. Fiez, "A Comparative Analysis of Parallel Delta-Sigma ADC Architectures," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 51, no. 3, Mar 2004.