A Compact Delay-Locked Loop for Multi-Phase Non-Overlapping Clock Generation

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***Abstract* — This paper presents the design, layout, and simulation results for a compact, low-power, low-jitter, delay-locked loop for multi-phase non-overlapping clock generation. A 500 nm CMOS process is used for the design with the total layout size being 810 µm x 95 µm. The operating frequency range is 20 – 100 MHz. The output clock jitter with 400 mV peak-to-peak noise on VDD is 250 ps at 100 MHz. The DLL's outputs consist of eight phases of true and complement, non-overlapping, clock signals (32 total clock signals) buffered to drive standard 8-MOSFET-1-Capacitor switched capacitor circuits. The power dissipation is under 20 mW from a 5 V power supply.**

Keywords – Delay-Locked Loop, DLL, clock generator, nonoverlapping clock generator, phase detector, loop filter, voltage-controlled delay line, VCDL.

I. INTRODUCTION

Delay-locked loops (DLLs) have become ubiquitous in digital circuits. For example, for the last ten years DLLs have been included on all double-data rate (DDR) dynamic access memories (DRAMs), Fig. 1 [1]. These all-digital designs are robust but lack the tuning range of an analog-controlled DLL [2]. This paper presents an analog-controlled DLL that is compact, low power, and tolerant to power supply noise. The DLL is used with clock generation circuitry to generate 32 phases of clock signals for use in multi-phase switched capacitor circuits.

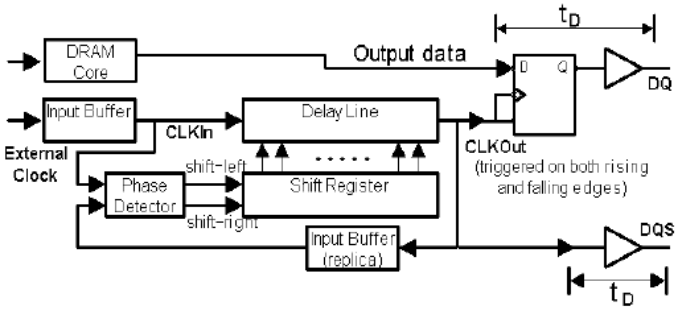

Figure 1. Block diagram of a digital DLL from [1].

A. Benefits of a DLL

Delay-locked loops (DLLs) are a lower jitter alternative to phase-locked loops (PLLs) when there is a reference clock available at the desired frequency [3]. A PLL uses a variable oscillator that is, generally, voltage-controlled to generate the output clock signal. A DLL uses a variable delay line that is controlled to phase shift the output signal to achieve phase-lock with the reference clock. A PLL integrates the phase difference of its input data and its oscillator to control the oscillator *frequency*, which results in a second-order feedback loop. A DLL, on the other hand, integrates the phase difference between the reference clock and its delay line output to control the *phase* of its output, which results in a first-order feedback loop. A first-order feedback loop is easier to stabilize and ultimately results in better jitter performance for a DLL when compared to a PLL.

B. Challenges

The main challenges faced when designing a DLL include the locking range (set by the maximum and minimum delays of the delay line), the resolution of the delay line (for a digital delay this is at least a gate delay), and making the DLL's output immune to power supply noise. While there are trade-offs with any design the one presented here uses an analog-controlled delay line that results in good delay range and resolution. The major concern, when using an analog delay, is the sensitivity to power supply noise.

II. DLL AND CLOCK GENERATOR BUILDING BLOCKS

The DLL consists of a phase detector, charge pump, loop filter, and a variable delay line. Figure 2 shows a block diagram of the DLL.

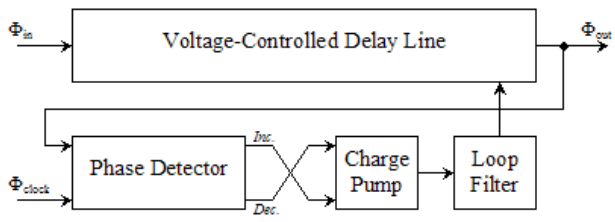

Figure 2. DLL block diagram

In this case, the input clock is both the input data (Φ_{in}) and the reference clock (Φ_{clock}) since the DLL is used for clock generation rather than to align output data with the reference clock (another common use for DLLs). The output of the DLL

(Φ_{out}) is used as the input to a non-overlapping clock generation circuit as shown in Figure 3.

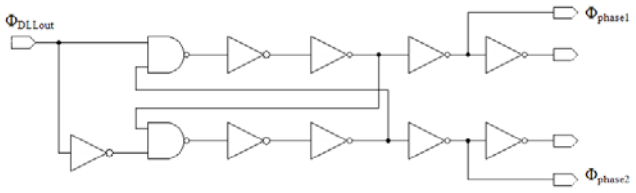

Figure 3. Nonoverlapping clock generation circuit

A. *Phase Detector*

The schematic and layout of the phase detector (PD) circuit is shown in Figures 4 and 5. The transistors are sized with small widths to reduce power consumption and layout size. This PD design is robust and well-used [3]. Notice, in the layout seen in Fig. 5, the abundant use of both well and substrate contacts.

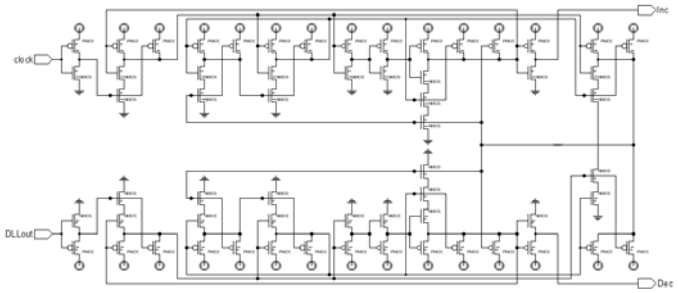

Figure 4. Phase detector schematic

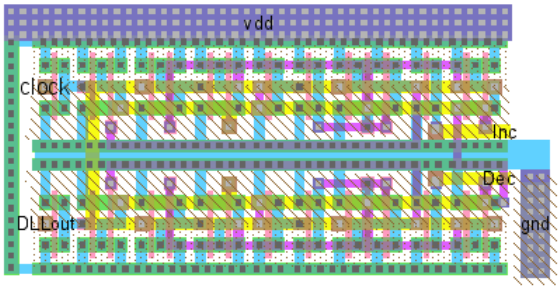

Figure 5. Phase detector layout

B. *Charge Pump and Loop Filter*

The schematic and layout of the charge pump is shown in Figures 6 and 7. The loop filter consists of five parallel NMOS capacitors on the charge pump output. Because current sources are used in this design, noise on either the power supply or ground, ideally, doesn't affect the operation of the circuit. Noise on VDD, for example, couples directly to the gates of the PMOS devices keeping their source-gate voltages constant. Similarly, noise on ground couples directly to the gates of the NMOS devices resulting in constant gate-source voltages. Noise on ground, however, does couple directly into the charge pump's output. As we'll see this control voltage is used to bias an NMOS device in the delay element. It's also desirable, in this delay element, to keep the gate-source voltages of the NMOS devices used in the delay element constant, so the coupling between the control voltage and ground is desirable (and why we use an NMOS device and not a PMOS device).

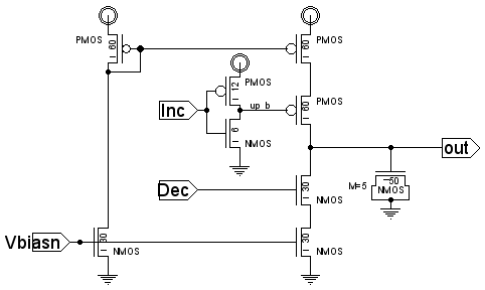

Figure 6. Charge pump and loop filter schematic

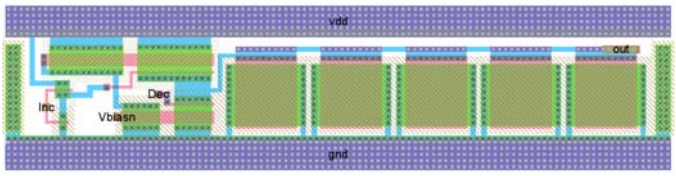

Figure 7. Charge pump and loop filter layout

As just mentioned the loop filter capacitor voltage (*out*) is the control signal input to the voltage-controlled delay line. The charge pump charges or discharges the loop filter capacitor depending on the output signals from the PD. When the input clock (*clock*) and delayed clock (*DLLout*) inputs to the PD are in phase, the *Inc* and *Dec* outputs of the PD will both be low and the loop filter capacitor will neither be charged nor discharged by the charge pump.

The cascode PMOS and NMOS devices on the charge pump output help to isolate the loop filter from power supply noise. They also supply large output impendence for a large RC time constant when the *Inc* and *Dec* inputs are both low and the loop filter capacitor voltage is decaying.

C. *Beta-Multiplier Reference*

The charge pump circuit bias voltage (*Vbiasn*) is generated by a beta-multiplier reference (BMR), Figs. 8 and 9. The BMR is self-biased and thus has an ideally flat response as VDD varies, thus reducing the susceptibility to power supply noise as shown in Figure 10.

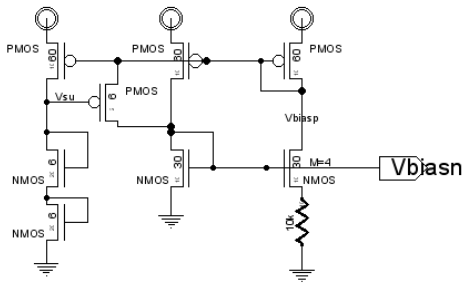

Figure 8. Beta-multiplier reference schematic

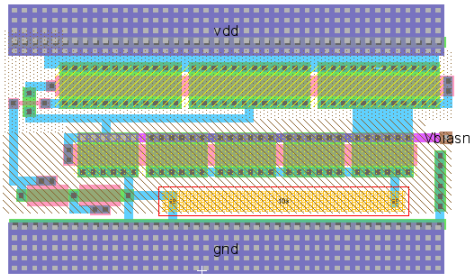

Figure 9. Beta-multiplier reference layout

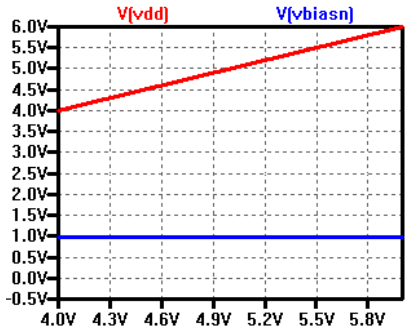

Figure 10. BMR simulation sweeping VDD

D. *Voltage-Controlled Delay Line*

The voltage-controlled delay line (VCDL) consists of eight delay stages in series and a bias circuit (for the delay stages). The concise schematic of the VCDL and bias generator are shown in Figure 11.

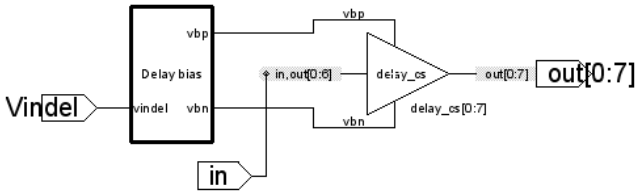

Figure 11. VCDL schematic

Each delay stage consists of a current-starved inverter followed by two additional inverters to clean up the signal and ensure fast edge transitions. The schematic of a VCDL delay stage is shown in Figure 12. Notice the decouple capacitor (the NMOS device on the right) in the schematic. It's important that the variation across the delay element be slowed, using decoupling capacitors, so that the loop response can compensate for variations in VDD. If this is the case then simpler, low-power circuits, can be used without a hit to VDD sensitivity.

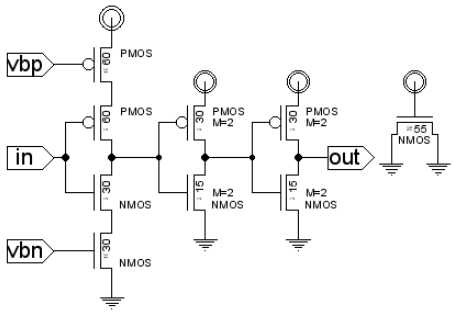

Figure 12. VCDL delay stage schematic

The bias current in the current-starved inverter stage, and thus the delay of the stage, is set by the bias voltages *vbp* and *vbn*, Fig. 13. These bias voltages are ultimately controlled by the input to the VCDL (*Vindel*), which is connected to the loop filter capacitor voltage (*out*). The full VCDL circuit layout is seen in Fig. 14. Again note the use of an abundant number of well and substrate contacts on the top and bottom of the layout.

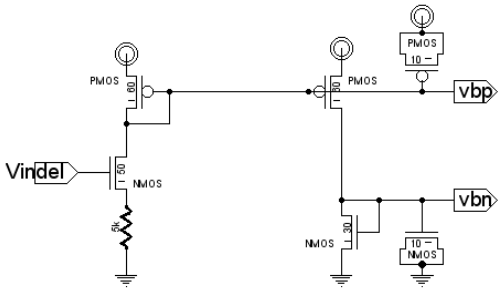

Figure 13. VCDL delay stage bias circuit

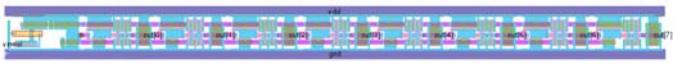

Figure 14. VCDL layout

E. *Non-overlapping Clock Generator*

The DLL output is the input to the non-overlapping clock generation circuit. The schematic of the non-overlapping clock generator is shown in Figure 3 and the layout is shown in Figure 15. The circuit generates two non-overlapping clock signal outputs (labeled *p1* and *p2* in the layout) and their complements (labeled *p1i* and *p2i* in the layout).

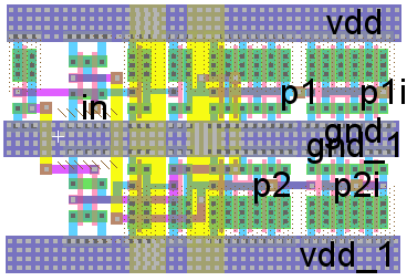

Figure 15. Non-overlapping clock generation circuit layout

III. Full Circuit Layout

The layout of the full DLL and clock generator circuit is shown in Figure 16. There are eight delay stages, with the output of each delay stage being fed to a non-overlapping clock generator circuit. Therefore, there are 32 clock signals generated by the circuit. The full circuit takes up an area of 810 µm x 95 µm in the 0.5 µm CMOS process.

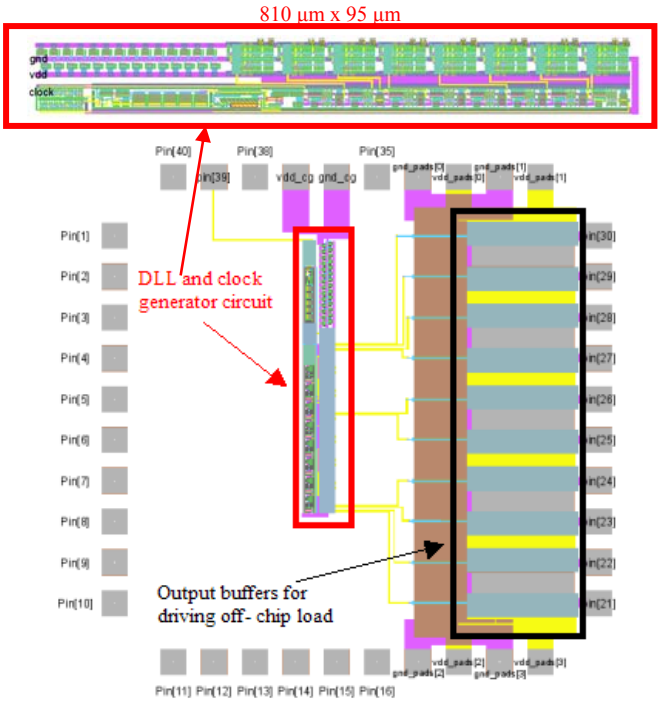

Figure 16. DLL and clock generator circuit layout with padframe

IV. Summary

Table 1 provides a summary of the DLLs simulation results. With 400 mV peak-to-peak noise added to the VDD supply, the jitter is 250 ps at 100 MHz as seen in Fig. 17.

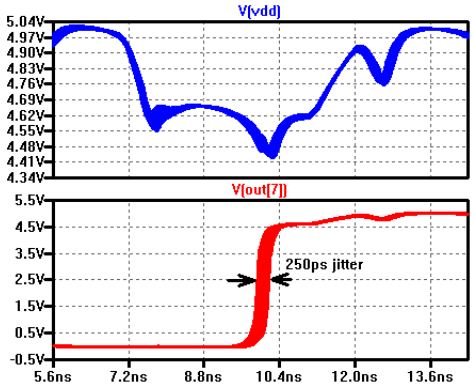

Figure 17. Eye diagram simulation with 400 mV pk-pk noise on VDD

Figure 18 shows the simulation results with a 100 MHz input clock. The first stage outputs (*p1[0]* and *p2[0]*) and the last stage outputs (*p1[7]* and *p2[7]*) are shown. Each stage has two non-overlapping clock outputs and their complements. The complement signals are not shown.

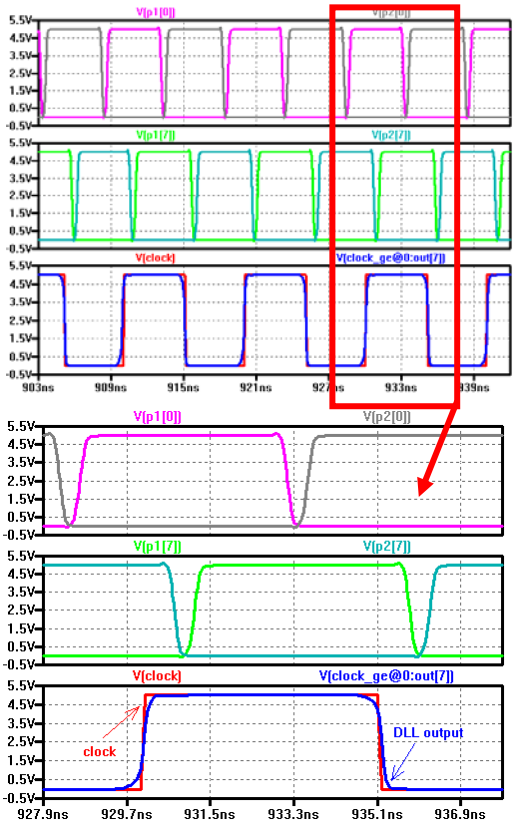

Figure 18. Non-overlapping clock generation simulation

Finally, the chip has been submitted for fabrication. Experimental results will be reported as well as additional details after testing is completed.

TABLE I. Summary of Results

Process	0.5 µm CMOS
VDD	5 V
Operating Frequency	20 Mhz – 100 Mhz
Layout Area	810 µm x 95 µm
Peak-to-Peak jitter	250 ps @ 100 Mhz
Power dissipation	17.5 mW (includes buffers)

References

[1] Lin, F., Miller J., Schoenfeld A., Ma, M. and Baker, R.J., "A Register-Controlled Symmetrical DLL for Double-Data-Rate DRAM," *IEEE Journal of Solid State Circuits*, Vol. 34, No. 4, pp. 565-568.

[2] Lin, F., Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops, Electrical Engineering Doctoral Dissertation, University of Idaho, 2000.

[3] R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, Revised 2nd ed., *Wiley-IEEE*, 2008.