Integration of IC Industry Feature Sizes with University Back-End-of-Line Post Processing: Example Using a Phase-Change Memory Test Chip

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***Abstract*— We have demonstrated that back-end-of-line (BEOL) processing can successfully be performed in a university environment on die that have been fabricated at a foundry. This processing option enables universities to integrate state-of-the-art feature sizes with low resolution photolithography capabilities, such as achieved with a contact aligner, typically available at universities. With this capability, new device technologies and materials can be explored at the university level, where the basic research on the technology can occur without the timelines and expectations that are placed on product development in an industrial setting. By incorporating state-of-the-art feature sizes with these research efforts, the research results will be more applicable and more easily transferable to an industrial environment. In our project, we have demonstrated the integration of a foundry processed chip with the BEOL university processing through the fabrication of a small phase-change memory array with CMOS access transistors and addressing circuitry wherein the phase-change memory material was processed BEOL at Boise State University.**

Keywords- BEOL, MOSIS, phase-change memory, chalcogenide.

I. Introduction

As industrial state of the art microfabrication feature sizes shrink, academic research in any area that depends on microfabricated devices becomes more obsolete unless the technology being researched can keep up with, or scale, in a way that is directly applicable to the industry standard. The rate of innovation required to achieve industrially competitive feature sizes has also accelerated, in most cases leaving behind all but the most intensively funded university microfabrication facilities. Yet investigating characteristics of new materials often requires the academic approach and the focused research environment found at universities. The large disconnect between academic and industrial technological abilities often hinders the development of useful collaborations between academia and industry. This can produce a large wasted research effort on the part of both industry and the university since many costly industrial investigations end up getting abandoned due to a lack of fundamental understanding of device operation. Similarly, many costly university efforts simply repeat work that has been previously done in industry, or may proceed down a path that industry has already deemed impractical at modern feature sizes. A more collaborative and useful relationship between the two types of research environments may provide a significant cost savings as well as a faster advancement in technological development.

It is with the goal of developing fabrication and processing abilities for exotic materials and technologies potentially useful for industry that we have explored ways to achieve fabricated devices using state-of-the-art feature sizes. We have successfully demonstrated an option that is cost-effective for universities: fabricating state-of-the-art front-end-of-line (FEOL) processes at a foundry on the die level, and integrating these die with back-end-of-line (BEOL) exotics material processing at the university. There are very few reports in the literature that describe test chip fabrication integrating CMOS circuitry with post-processing of exotic materials [1-3], and in fact, none of these reports provide a full integration of the foundry work with university BEOL processing.

We have demonstrated this integration through the fabrication of a phase-change memory test chip which incorporates FEOL CMOS access transistors and array addressing circuitry with the exotic BEOL materials processing for phase-change memory development. This option was selected since phase-change memory device operation is fairly well-understood and could provide a good example of integration of the university-level exotic materials processing with CMOS processing. Phase-change chalcogenide-based nonvolatile memory research has attracted considerable interest recently due to the potential device scalability for a next-generation solution to replace Flash memory, and its inherent radiation resistance [4-6]. Investigation into new nonvolatile memory devices utilizing experimental materials requires fabrication of test chips to demonstrate functionality and proof-of-concept. We have utilized the MOSIS fabrication service for test chips because the service offers low cost fabrication for

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small numbers of chips with commercially available CMOS processes.

This paper describes the fabrication of phase-change memory devices for nonvolatile memory research by manufacturing test chips through MOSIS that are designed with exposed electrodes for exotic materials post-processing. Back-end-of-line (BEOL) processing was completed at Boise State University's Idaho Microfabrication Laboratory (IML) to produce nonvolatile memory test devices with chalcogenide materials. The completed chips were electrically evaluated.

Upon receipt of the test chips from MOSIS, the die were visually inspected and transistors were tested to verify functionality and to provide a baseline for post-processing comparison. Prior to BEOL processing, each bare die was fixed to a handle wafer for compatibility with photolithography, deposition and etch tools at the IML (Figure 1).

Basic steps for BEOL processing for the phase-change memory devices consist of blanket depositions of germanium chalcogenide followed by tin chalcogenide, and a sputtered tungsten top electrode. Top electrodes of the devices and bond pads were then defined by photolithography. An ion mill etch removed tungsten and chalcogenide films not covered by photoresist, clearing the films from both the insulation layer and bottom electrode bond pads.

Measurements to characterize electrical response included measurement of programmed resistance, currents, and the switching threshold voltages. These measurements were performed on two-terminal devices and devices fabricated in the drain of a MOSFET (Mbits). Test structure transistors were measured pre- and post-processing to assess the influence, if any, of the BEOL processing on the transistor characteristics.

II. Experimental Procedures

A. Layout and Mask Design

The test chip was designed using the AMI C5 process and laid out using the Electric VLSI Design system as previously described in [7]. Even though this is a 0.5 µm process which is far from state of the art, it demonstrates that a university back-end-of-line process can be integrated with a commercially viable process. The test chips were submitted to the MOSIS fabrication service [8]. Design simulations were performed

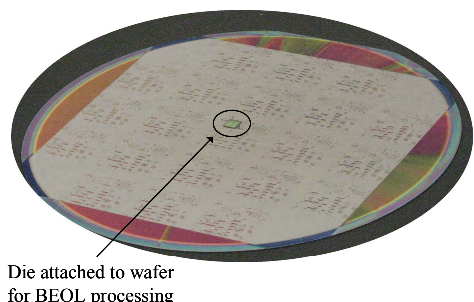

Figure 1. Single die attached to 100 mm handle wafer.

using SPICE models. The design layout included peripheral circuitry, three different sizes of memory bits, 1.8, 3.6 and 5.4 µm vias with and without access transistors, two 64-bit arrays with 0.6 µm vias and 70 µm x 70 µm bond pads. The design of the test structures contained contacts up to the Metal3 layer since AMI's C5 process is a three metal process.

Alignment marks were incorporated into the chip design to accommodate the resolution limitations of the Quintel Q-4000 contact aligner used to pattern the top electrode. Alignment marks were designed with smaller error margins than device overlap tolerances to guarantee adequate coverage of electrodes over device vias. Chips were requested unpackaged, with bottom electrodes exposed through openings in the passivation layer.

For BEOL processing of the chips, a clear field mask was designed and sent for fabrication to the Rochester Institute of Technology Semiconductor & Microsystems Fabrication Laboratory Mask House [9]. The mask designed using Electric was in accordance with the fabrication equipment available at the IML at Boise State University. Accommodating the resolution of the contact aligner for BEOL processing was the most critical consideration in the mask design.

B. Post-processing BEOL

Upon receipt, chips were visually inspected. Electrical data was collected on transistor test structures on selected bare die for linear ID-VG, saturated ID-VG, and ID-VD with 0, 1, 2, 3, 4, 5 V VG sweeps.

Prior to BEOL processing, each die was fixed to a 100 mm handle wafer using Ablebond epoxy 84-3 and cured at 150 °C in a muffle furnace for 1 hour. The die was located on the wafer to allow for alignment with the top electrode mask either using dimensions obtained from the top electrode mask layout, or using alignment marks included in the top electrode mask pattern etched into thermally-grown oxide on the handle wafer. A die attached to the handle wafer is, again, shown in Figure 1.

Two 100-mm control wafers without a die, but with the single device design of similar architecture as previously reported [10] to the two-terminal devices on the MOSIS chip, were processed simultaneously with the wafer containing the MOSIS chip.

Following epoxy heat cure, the die was Ar^+-sputter cleaned using a Veeco ME 1001 ion mill with 550 eV beam voltage, 300 eV source voltage, 300 mA beam current and – 45° etch angle, with a process time of 6 s. This sputter clean was used to remove any metal oxides from the metal 3 surface prior to chalcogenide deposition.

Within 24 h of the sputter clean, chalcogenide films were thermally evaporated using a CHA Industries SE-600-RAP evaporator equipped with three-wafer planetary rotation at a base system pressure of 2×10^{-6} Torr. The film was evaporated on the die/handle wafer, two single device control wafers, and a witness Si wafer fragment, simultaneously. In this way, all 3 wafers and the wafer fragment received the same film. The deposition rate was monitored with a single crystal head Inficon IC 6000. The first memory stack consisted of 300Å germanium (III) selenide, synthesized as described by

Campbell et al. [11], and followed by 500Å SnTe (Alfa Aesar) with an air break between films. The second chalcogenide stack was produced in a similar manner using SnSe (Alfa Aesar) instead of SnTe. The tungsten film was sputter deposited at 50 watts power, 8 x 10^{-6} Torr base pressure (350Å), in a Sputter Sciences CrC150 single wafer tool. Photolithography to define top electrodes and bond pads was performed using Megaposit SPR-220.30 photoresist, a Quintel Q-4000 Contact Aligner and Megaposit MF-26A developer.

The device defining Ar^+ ion mill etch was performed under the same tool conditions as the Ar^+-sputter clean, using a sputter etch time of 2 minutes and 20 seconds. Photoresist was left in place for electrical testing.

C. *Electrical Characterization*

Electrical measurements were performed on the die, pre- and post-BEOL processing, using a Micromanipulator 6200 microprobe station, and a Hewlett-Packard 4145B Semiconductor Parameter Analyzer. Electrical contact to the die was made using Micromanipulator probes with tungsten tips.

III. Results and Conclusions

Four die with two control wafers accompanying each were fabricated, using two different dual chalcogenide stacks. A completed chip with photoresist in place on top electrodes is shown in Figure 2. Affixing each bare die to a handle wafer permitted easy handling and processing of the die, and introduced no complications. The epoxy withstood two ion mill processing steps, spin coating, and contact alignment in general with no problems. On occasion the pressure applied during intimate contact of the die with the top electrode mask caused an edge of the die to crack.

Alignment of the top electrode mask to the chip on the template wafer was complicated by several factors, including practical resolution limits on the mask aligner and photoresist edge bead issues on the die, which distorted the apparent alignment. Ultimately alignment was achieved by verifying correct placement of the top electrodes over the vias and that no bond pads overlapped, through the contact aligner viewer and again following photoresist development.

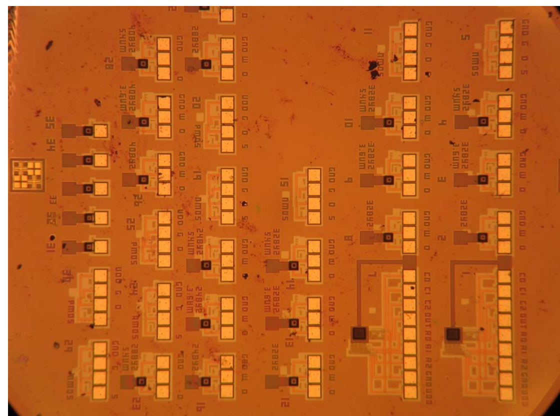

Figure 2. Photograph of completed test chip.

Electrical testing revealed no electrical short or open issues resulting from misalignment. Figure 3 shows a completed NMOS transistor-controlled Mbit with a 3.6 µm via. Figure 4 shows a resistor bit with a 1.8 µm via.

Electrical characterization of phase-change devices was performed by forcing the current and measuring the voltage using the HP 4145 semiconductor parameter analyzer. Two-terminal devices and devices with an access transistor were measured and found to function normally as phase-change devices. Figure 5 shows an IV curve of a two terminal phase-change device from a completed test chip with Ge_2Se_3/SnSe layers, a possible multi-resistance state material stack, and illustrates the 'double' snap-back indicative of multi-resistance response.

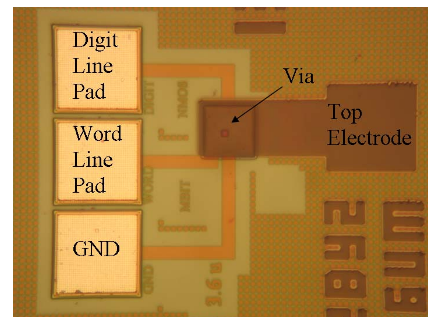

Figure 3. Completed Mbit.

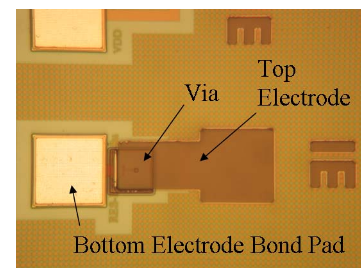

Figure 4. Completed two-terminal device.

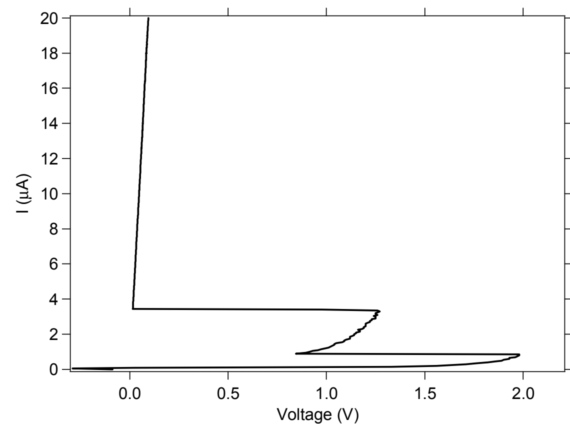

Figure 5. IV curve from Ge_2Se_3/SnSe two-terminal device.

Figure 6 compares IV curves for NMOS transistors as received (pre-process) and after the BEOL process flow has been completed (post-process). Transistor behavior appears unchanged by the processing.

Integration of older generation university-based photolithography processes with CMOS die fabricated through MOSIS with a 0.5 μm process has been successfully demonstrated to result in functional phase change memory devices. Post processing of CMOS single die allows for development of new device technologies with great flexibility. Exotic materials processing on a research and development scale, which is not an option in commercially available contract processes, can be integrated with CMOS circuitry using this technique.

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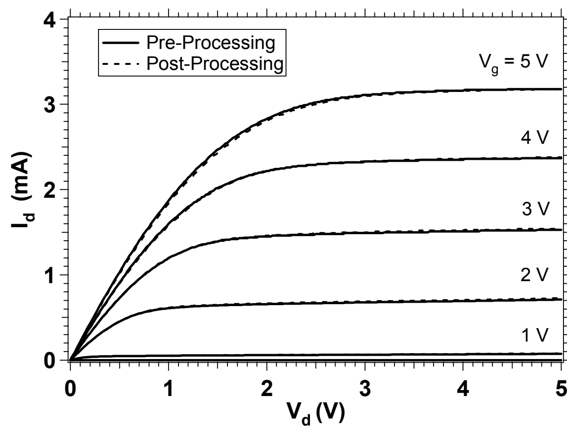

Figure 6. Comparison of IV curves for NMOS transistors pre- and post BEOL processing.

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