Resistive Memory Sensing Using Delta-Sigma Modulation

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***Abstract* – The design of four resistive memory sensing circuit topologies employing Delta-Sigma (ΔΣ) modulation are presented. Operation of the designs and a comparison between simulations and experimentation is given. The designs were fabricated in a 500 nm CMOS process. Measured results indicate that the resistive values ranging from a chosen reference resistance to several hundred kΩ can be sensed reliably.**

*Keywords- **CMOS, Delta-Sigma Modulation Non-Volatile Memory, Resistive Memory, Sensing***

I. INTRODUCTION

Nonvolatile memories are widely used in electronic devices for data storage including cellular phones, digital cameras, and portable storage media. A resistive memory element generally employs an access transistor in series with a resistive element (1T-1R) [1] or a cross-point array with the resistive element at the intersection of a row and column line [2]. A '1' or a '0' is stored by changing the resistance of the memory element.

Sensing the resistive memory element poses several challenges. In phase change random access memory (PCRAM) or magnetic random access memory (MRAM), which uses resistive memory elements, the difference in resistance between a logic one and a logic zero can potentially be a very small value [2]. The sensing circuit should be able to differentiate between these two narrowly separated states while at the same time not affect the state of this memory element. Delta-Sigma modulation based sensing scheme has the advantage over traditional sensing circuits [2] in being able to distinguish resistance values varying within a fraction of the actual value being sensed [3]. DC measurements/sensing using ΔΣ techniques can be very practical and robust [4-6].

This paper describes four different Delta-Sigma modulation based techniques for sensing resistive memory. The development of these topologies is based on a sensing circuit that contains a reference resistor and a comparator. The discussion and associated equations for the four sensing topologies are presented in Section. III. Section IV presents a comparison between chip measurement results and simulation results. Section V summarizes the results and comments on future work.

II. THEORY OF OPERATION

Delta-Sigma modulation based sensing is a powerful and practical circuit technique to measure the resistance of a resistive memory element [3]. An example ΔΣ sense amp circuit is seen in Fig. 1.

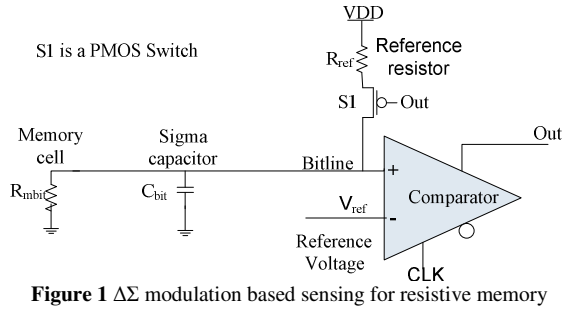

Figure 1 ΔΣ modulation based sensing for resistive memory

As shown in Fig. 1, the capacitor C_{bit} is charged through a reference resistor $R_{ref.}$ This capacitor constantly discharges through a selected memory element R_{mbit}. The feedback loop employed with the comparator attempts to maintain the voltage across the capacitor, and therefore the memory element, to the value of the reference voltage. The capacitor acts like an integrator (sigma), summing the difference (delta) between the current supplied via R_{ref} and the current sunk by R_{mbit}. By connecting R_{ref} to the capacitor each time the capacitor voltage drops below V_{ref} the time average current into the capacitor can be calculated based on the duty cycle of the recharging pulse generated by the comparator [3]. Knowledge of the time average current flowing into the capacitor yields the current flowing into $R_{mbit,}$ since the current charging the capacitor must be equal to the current discharged from the capacitor by the resistive memory element [3],[5]. By knowing the value of the average voltage being set across R_{mbit} and the value of the current flowing through it, the memory element's resistance can be determined [3].

In a real implementation of the circuit, the actual resistance of the memory element is not calculated. Instead, the number of clock cycles charging the capacitor is counted and is compared to a reference count [3]. The reference count is selected to represent a count value in between the logic 0 and logic 1. Hence a count greater than the reference count indicates one logic state and a count value lesser than the reference count indicates another logic state. For memories exhibiting multi-state capabilities, two or more reference counts are selected to differentiate between the different states and can be compared with the actual count to determine the current state of the memory cell. Since ΔΣ techniques use averaging, they have the advantage that a wide range of resistance values can be sensed and that they can be immune to device parasitics, mismatch, and supply noise [5].

III. DISCUSSION OF TOPOLOGIES

A. *Reference resistor based Delta-Sigma Sensing*

The bit line capacitance of a memory array acts as the sigma capacitance C_{bit}, i.e. C_{bit} from the Delta-Sigma technique discussed in Section I. A comparator is used to clamp the average voltage across the memory cell to a reference voltage (V_{ref}). During a sense operation, based on the current state of the memory cell (erased or programmed), the bit line voltage either stays at constant voltage V_{ref} or discharges to ground respectively. This change in bit line voltage is due to the current flowing though the memory cell draining the sigma capacitor's charge. The inverting output '*Outi*' shown in Fig. 2 goes low every time the voltage across the memory cell falls below the reference voltage level. This charges the sigma capacitor back to the reference voltage level by turning the PMOS switch S1 ON. *N* is the number of times the Delta-Sigma Sense Amp (DSSA) is clocked. *M* is the number of times *Out* goes high so that charge is supplied to the sigma capacitor through the reference resistor. This pulls the bit line voltage towards the reference voltage (or V_{ref}).

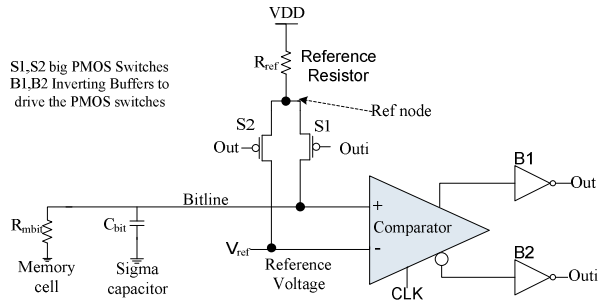

Figure 2 Reference resistor based ΔΣ sensing

The equations for the reference resistor-based ΔΣ sensing topology are derived below. The resistances of the PMOS switches S1 and S2 are very small in all the topologies discussed in this paper and hence their effect is neglected.

For the average voltage on the sigma capacitor to remain constant, the average amount of charge entering the sigma capacitor in one clock cycle (duration of clock period is *T* and the frequency is f_{clk}) is Q_{ref}, should be equal to average amount of charge leaving the sigma capacitor in one clock cycle i.e. Q_{mbit} .

$$Q_{ref} = Q_{mbit} \tag{1}$$

The average voltage across the memory cell is $V_{ref,}$ hence the average current through the memory cell I_{mbit} is given by

$$I_{mbit} = V_{ref} / R_{mbit} = \left(VDD / \left(2 \times R_{mbit}\right)\right) \tag{2}$$

The current flowing through reference resistor to charge the sigma capacitor I_{ref} is given by

$$I_{ref} = \left(VDD - V_{ref}\right) / R_{ref} = \left(VDD / \left(2 \times R_{ref}\right)\right) \tag{3}$$

Since *M* cycles are used to charge the sigma capacitor out of *N* clock cycles, the average reference current charging the sigma capacitor in one cycle is $I_{ref} \times (M/N)$. Using charge conservation shown in (1)

$$I_{mbit} \times T = I_{ref} \times (M/N) \times T \tag{4}$$

Hence the average current through memory cell (R_{mbit}) i.e. $I_{mbit,}$ is equal to average current supplied to sigma capacitor (C_{bit}).

$$I_{mbit} = I_{ref} \times (M/N) \tag{5}$$

$$\left(VDD / \left(2 \times R_{mbit}\right)\right) = \left(VDD / \left(2 \times R_{ref}\right)\right) \times (M/N) \tag{6}$$

$$R_{mbit} = R_{ref} \times (N/M) \tag{7}$$

The ratio of the number of times the non-inverting output 'Out' goes high (M), to the number of times the DSSA is clocked (N), gives us the ratio of the reference resistance used to the resistance of the memory cell.

$$\frac{M}{N} = \frac{R_{ref}}{R_{mbit}} \tag{8}$$

The minimum resistance that can be measured is the reference resistance. The maximum resistance that can be sensed is limited by the number of times the comparator is clocked,

$$R_{mbit,MAX} = R_{ref} \cdot N \tag{9}$$

The maximum Bit line charge variation is given by $I_{ref} \times T$ [6] or

$$\Delta V_{bit} \times C_{bit} \le I_{ref} \times T \tag{10}$$

$$\text{Bitline swing } \Delta V_{bit} \le \frac{VDD}{2 \times R_{ref} \times C_{bit} \times f_{clk}} \tag{11}$$

B. *Reference resistor based Delta-Sigma Sensing with offset*

Minimizing the voltage across the resistive memory element reduces the stress across the memory cell, thus avoiding a flip in the logic state of the memory cell. For this reason a comparator with built in offset on the reference terminal can be used. The voltage at the reference terminal is driven, via the feedback action, to $V_{ref} + V_{os}$, where V_{os} is the offset of the comparator. The memory cell is connected in between the bit line and a reference voltage (V_{ref}). This way, the average voltage across the memory cell is V_{os}. The equations governing the operation of this topology are summarized as below [6]

$$R_{mbit} = R_{ref} \times \left(V_{os} / \left(VDD/2 - V_{os}\right)\right) \times (N/M) \tag{12}$$

$$\text{Bit line swing } \Delta V_{bit} \le \frac{\left(VDD/2 - V_{os}\right)}{R_{ref} \times C_{bit} \times f_{clk}} \tag{13}$$

Here again the minimum resistance that could be sensed is the reference resistor, while the maximum resistance that could be sensed is,

$$R_{mbit,MAX} = R_{ref} \times \left(V_{os} / \left(VDD/2 - V_{os}\right)\right) \times (N) \tag{14}$$

C. Swicthed-Capacitor Delta-Sigma Sensing

Using a simple resistor as a reference has the disadvantage of restricting the flexibility to adjust the reference resistance value. A switched-capacitor resistor, Fig. 3, can be used to adjust the resistance by changing the clock frequency f_{clkSC}, (15) [6].

$$R_{ref} = \frac{1}{f_{clkSC} \times C} \tag{15}$$

A non-overlapping clock generator is used for $Ø_1$ and $Ø_2$ clocks. In switched-capacitor Delta-Sigma sensing (see figure 3), when $Ø_1$ is low, C_{cup} is charged to *VDD*. When $Ø_2$ is low, this charge from C_{cup} is supplied to the sigma capacitor. If the voltage across the sigma capacitor goes below the reference voltage, then the PMOS switch connected to the bit line turns on, and C_{cup} transfers charge on to the bit line. This charges the sigma capacitor back to approximately the reference voltage. The number of clock cycles charging sigma capacitor *M* is again recorded.

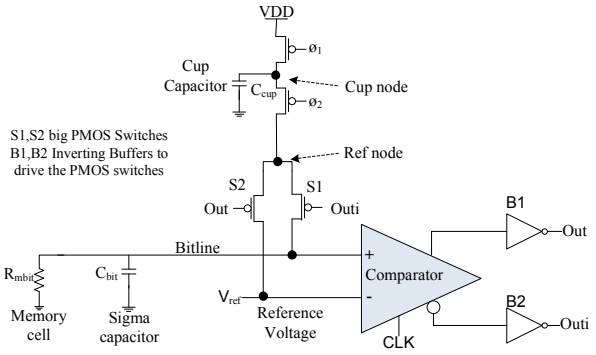

Figure 3 Switched-capacitor ΔΣ sensing

Following the same procedure used in the Reference resistor based ΔΣ sensing topology (see III.A), the equations for the switched-capacitor topology [6] are given by

$$Q_{mbit} = Q_{cup} \tag{16}$$

$$I_{mbit} \times T = I_{cup} \times (M/N) \times T \tag{17}$$

$$I_{mbit} = I_{cup} \times (M/N) \tag{18}$$

$$V_{ref} / R_{mbit} = (Q_{cup} / T) \times (M/N) \tag{19}$$

$$V_{ref} / R_{mbit} = (Q_{cup} / T) \times (M/N) \tag{20}$$

$$(VDD/(2 \times R_{mbit})) = C_{cup} \times (VDD - VDD/2) \times (1/T) \times (M/N) \tag{21}$$

$$R_{mbit} = (1/(f_{clk} \times C_{cup})) \times (N/M) \tag{22}$$

$$R_{mbit,MAX} = (1/(f_{clk} \times C_{cup})) \times (N) \tag{23}$$

$$\text{Bitline swing } \Delta V_{bit} = (C_{cup}/(C_{cup} + C_{bit})) \times (VDD/2) \tag{24}$$

D. Switched-Capacitor Delta-Sigma Sensing with offset

As discussed in "Reference resistor based Delta-Sigma Sensing with offset", sensing scheme based on comparator with offset minimizes the stress across the resistive memory cell. A comparator with built-in offset is used for this purpose along with a switched-capacitor resistor as the reference resistor that can be varied with the clock frequency. The equations for this topology follow [6]

$$R_{mbit} = (1/(f_{clk} \times C_{cup})) \times (V_{os}/(VDD/2 - V_{os})) \times (N/M) \tag{25}$$

$$R_{mbit,MAX} = (1/(f_{clk} \times C_{cup})) \times (V_{os}/(VDD/2 - V_{os})) \times (N) \tag{26}$$

$$\text{Bitline swing } \Delta V_{bit} = (C_{cup}/(C_{cup} + C_{bit})) \times (VDD/2 - V_{os}) \tag{27}$$

IV. Chip Test Results and Comparison with Simulation Results

A test chip was designed, Fig. 8, using the Electric VLSI Design System [7] in AMI's C5 500 nm CMOS process, through the MOSIS fabrication service. The chip includes the four variants of Delta-Sigma sensing schemes as described in this paper.

All four DSSA topologies are tested using either f_{clk} = 10 MHz or f_{clk} = 15 MHz and sense time of *N* = 500 or 750 clock cycles (50 μs). Note that the sense time scales with the clock frequency. The sensed resistance values are calculated by method described below. A base output count (M_{base}) is measured for a known resistor value (R_{base}). To ascertain the value for an unknown resistor (R_{sesnse}) based on output count (M_{sense}), we know that

$$R_{base} \propto 1/M_{base} \tag{28}$$

$$R_{sense} \propto 1/M_{sense} \tag{29}$$

$$R_{sense} = R_{base} \times (M_{base}/M_{sense}) \tag{30}$$

Discrete resistors are used instead of the resistive memory element bit to evaluate the performance of the four DSSA, the results are presented in plots seen in Figs. 4-7. The sensed resistances shown in the plots can be made linear, by increasing the sense time i.e., the number of times the comparator is clocked. From the plots, we can see that the simulated resistances vary from the actual resistance values; this is due to the fact that the charge being transferred to the sigma capacitor is dependent on the varying bit line voltage. This issue can be easily addressed in the future by adding a PMOS switch with its gate connected to the reference voltage to make the charge being supplied to sigma capacitor independent of the bit line voltage. The results from the design simulation and chip testing were found to match closely in all topologies with variations likely due to the mismatch of transistors in comparator, the assumed values for the parasitics, including the large off-chip capacitances. These parasitic capacitances can be estimated from the measured results. They can then be added to the simulations to show a

near exact match between measurements and simulation. However, since this doesn't add value to the design, or influence the final results in a practical sensing circuit, we simply point it out before concluding.

V. Conclusion

This paper presented the theory and experimental verification of four different topologies useful for sensing resistive memory using Delta-Sigma techniques. Future work will include: attempts to ensure that the sense-amps can be laid out on pitch with a memory array, selection of the most robust topology for a specific memory technology, and integration of the sense-amps with new non-volatile memory technologies.

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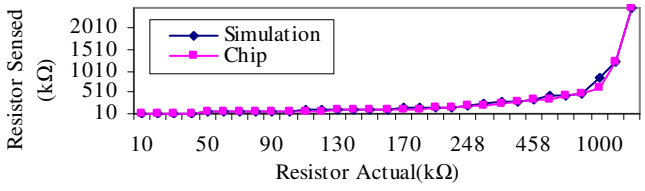

Figure 4 Resistor sensed vs. resistor actual for reference resistor-based Delta-Sigma Sensing, see Sec. III.A with *fclk* = 10 MHz, *Rref* = 5kΩ, *Cbit* = 82 pF, *N* = 500. Rmax=2.5MEG (eq. 9)

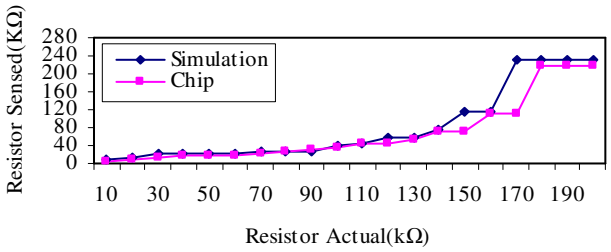

Figure 5 Resistor sensed vs. resistor actual for reference resistor based Delta-Sigma Sensing with offset, See Sec. III.B with *fclk* = 15 MHz. *Rref* = 5 kΩ. *Cbit* = 144 *pF*. *N* = 750.

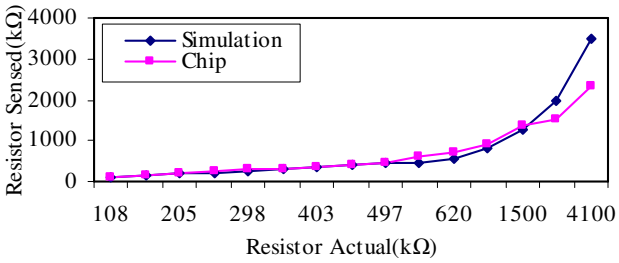

Figure 6 Resistor sensed vs. resistor actual for switched-capacitor Delta-Sigma sensing see III.C *fclk* = 10 MHz, *Rref* = 27.77kΩ, *Cbit* = 17.6 pF, *Ccup* = 3.6 *pF*, *N* = 500. Rmax=13.8MEG (eq. 23)

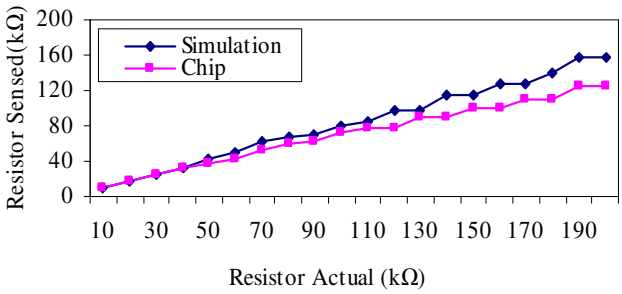

Figure 7 Resistor sensed vs. resistor actual for switched-capacitor Delta-Sigma sensing with offset see Sec. III.D *fclk* = 10 MHz, *Rref* = 27.77 kΩ, *Cbit* = 17.6 pF, *Ccup* = 3.6 pF, *N* = 500.

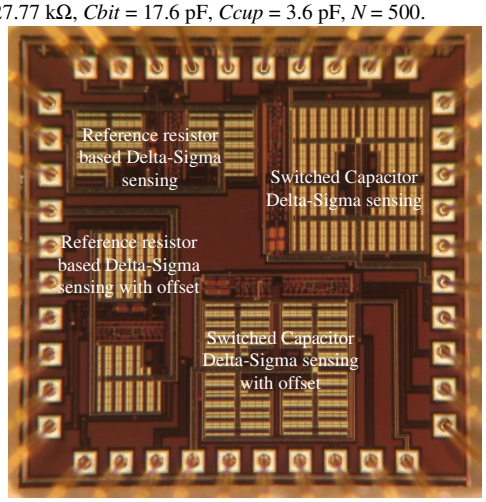

Figure 8 Microphotograph of the test chip designed