Full-Feedforward *K*-Delta-1-Sigma Modulator

Kaijun Li, Vishal Saxena, Geng Zheng, and R. Jacob Baker

***Abstract*—This paper discusses the design of a second-order full-feedforward *K*-Delta-1-Sigma (KD1S) modulator with a fast feedback loop around the quantizer. The proposed second-order KD1S modulator employs inherent interleaving with shared op-amp and *K*-quantizing paths that has the potential to achieve significantly higher conversion bandwidths than traditional delta-sigma ADCs. A second-order full-feedforward ADC using an 8-path KD1S modulator and ideal components achieves an SNR of 70 dB (or 12-bit resolution) for a conversion bandwidth of 6.25 MHz with 800 MHz effective sampling rate. For the same bandwidth, the proposed second-order KD1S modulator is simulated in 130 nm CMOS achieving 58 dB SNR (or 10-bit resolution).**

***Index Terms*— Analog-to-digital converter, delta-sigma modulation, *K*-Delta-1-Sigma, KD1S, noise-shaping, full-feedforward, wideband ADC.**

I. INTRODUCTION

Continued CMOS scaling has made analog design more challenging. In particular, the intrinsic gain of transistor has dropped dramatically as CMOS technology evolves into nanometer range. This means it is hard to design high gain amplifiers in modern CMOS processes, which are the critical building blocks in analog design. On the other hand, the continued scaling of transistor feature size reduces the power consumption because of the lower supply voltage while at the same time increasing the transistor's operation speed due to the increased transistor f_T.

Analog-to-digital converters (ADCs) act as an interface between the analog and digital worlds. For high-speed operations in baseband application, Nyquist rate ADCs such as the Flash ADC benefit from scaling of CMOS technology, and find themselves in those applications within the multiple GHz range [1], [2]. Nevertheless, high power dissipation and low-resolution limit the use of the Flash ADC. For instance, a Flash ADC with a power dissipation of several Watts can't be used in portable or handheld applications, simply because it will drain the battery too quickly [3]. For high-speed applications, pipelined ADCs can be used with moderate resolutions (10-14 bits) in the 100-500 MHz range [4]. However, intensive calibration in digital domain is usually employed to achieve this high-resolution at the cost of increased area, latency, and power dissipation. Furthermore, the ADCs or DACs inside the digital calibration block are difficult to design due to the degradation of the transistor's intrinsic gain in nano-CMOS. Thus it is necessary to investigate other ADC topologies which are inherently tolerant to device mismatches and process variation.

II. DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTERS

Delta-sigma ADCs are known for their high-resolutions or higher *signal-to-noise ratio* (SNR) and low to moderate conversion rates. The *Delta-Sigma Modulator* (DSM) employs oversampling to spread the quantization noise over a wider bandwidth, and noise-shaping to further attenuate the in-band quantization noise to achieve higher resolutions using an internal coarse ADC. The modulated noise can be filtered out digitally which means that much of the analog signal processing is transferred to the digital domain. Thus DSMs trades off digital circuit complexity for analog circuit complexity which is favorable for CMOS scaling [6].

The *oversampling ratio* (OSR) is defined as

$$OSR = \frac{f_s}{2 \cdot BW} \quad (1)$$

Normally, OSR is chosen to be reasonably large to achieve required a SNR based on the order of DSM. This indicates that DSM has to employ higher sampling frequency (f_s) for a given bandwidth application. Therefore, the traditional delta-sigma ADCs can't achieve Nyquist-rate sampling as desired for wideband data conversion.

III. TIME-INTERLEAVED DELTA-SIGMA MODULATORS

The time-interleaved delta-sigma ADC is constructed by placing delta-sigma ADCs in parallel and applying the input signal to all of the channels simultaneously [6]-[9]. Each parallel channel operates independently, and the digital outputs from all channels are recombined to extend the overall bandwidth. However, such schemes, as shown in Fig. 1, achieve only a 0.5 bit resolution improvement (or 3 dB increase in SNR) for every doubling in the number of channels [9].

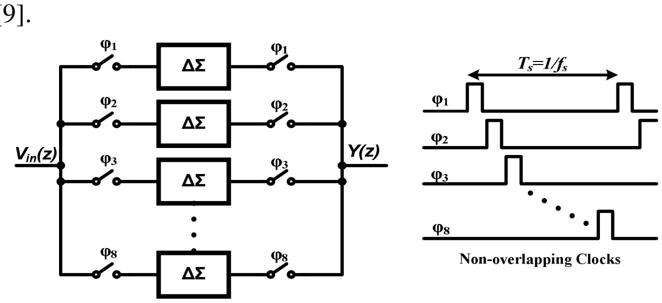


Figure 1 A time-interleaved or parallel delta-sigma modulator.

Instead of obtaining *true-noise-shaping* in frequency where the quantization noise is moved all the way to the frequency $K{\cdot}f_s/2$, time-interleaved delta-sigma ADC results in rippled noise-shaping in the *noise transfer function* (NTF) as shown in Fig.

2. Thus time-interleaved DSMs bring little performance improvement for a significant increase in area and power consumption.

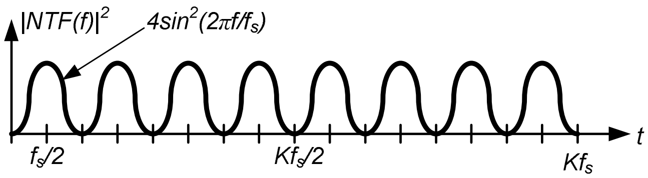


Figure 2 Noise shaping response for a first-order time-interleaved DSM.

IV. Proposed *K*-Delta-1-Sigma Modulator

A. KD1S Topology

Consider a *K*-path Delta-Sigma modulator with a shared integrator among the *K*-paths. This topology termed as *K-Delta-1-Sigma* (KD1S) modulator is shown in Fig. 3 [5]. The concise KD1S modulator configuration view of Fig. 3 and K non-overlapping clock phases are illustrated in Fig. 4.

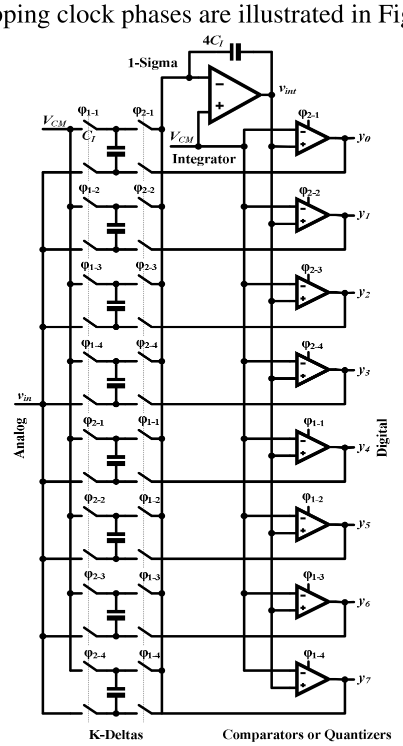


Figure 3 The *K*-Delta-1-Sigma modulator topology.

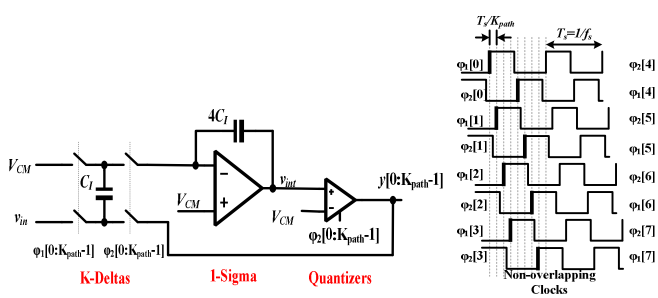


Figure 4 The concise *K*-Delta-1-Sigma modulator topology.

In Fig. 4, the KD1S modulator constitutes *K* phases clocked at f_s, where the effective sampling rate of the modulator is determined by the spacing between two adjacent edges of the clock phases and given as

$$f_{s,new} = K_{path} \cdot f_s \tag{2}$$

One of the benefits of sharing a single opamp is that the forward path mismatches are averaged out when the feedback signal are spread out across the *K*-paths. Another benefit is less power consumption when compared to conventional time-interleaved DSM. The op-amp's unity gain frequency (f_{un}) only needs to be a small multiple of f_s, and this alleviates the requirement for op-amp design in ultra high-speed (GHz range) applications.

The noise transfer function for ideal first-order KD1S is

$$NTF(f) = 2\sin\left(2\pi f / K_{path} f_s\right) \tag{3}$$

with the effective number of bits is given by

$$N_{\text{eff}} = N - 0.566 + 1.5 \cdot \log_2(OSR \cdot K_{path}) \tag{4}$$

Thus the first-order KD1S topology achieves a 1.5 bits gain in resolution per doubling in the number of paths as is shown in Fig. 5. In other words, doubling of the number of paths has the same effect as doubling the *OSR*.

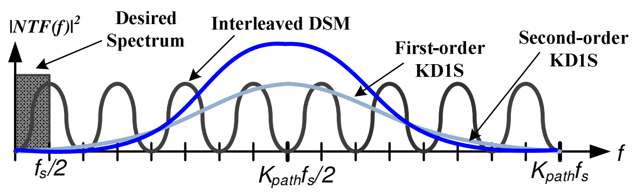


Figure 5 True wideband noise shaping using a *K*-Delta-1-Sigma Modulator.

B. Full-Feedforward Architecture

Figure 6 shows a conventional *chain of integrators with distributed feedback* (CIFB) structure.

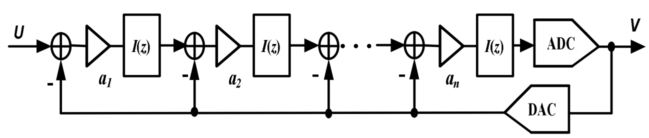


Figure 6 Block diagram of the conventional CIFB structure.

The *chain of integrators with distributed feedforward* (CIFF) structure is complement to CIFB structure as is shown in Fig. 7. Full-feedforward DSM belongs to CIFF structure and its block diagram is shown in Fig. 6 [11]. Normally coefficient c_0 is set to be equal to 1 in order to obtain unity STF, and so the distortion will be independent of the input signal.

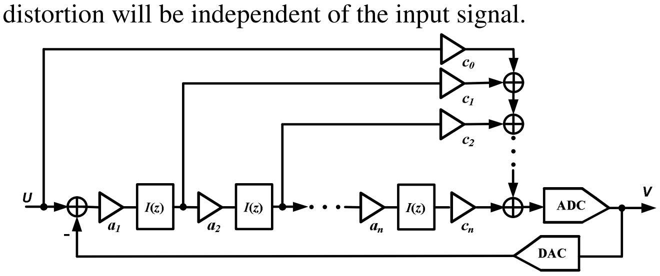


Figure 7 Block diagram of full-feedforward structure.

The block diagram of second-order full-feedforward DSM is shown in Fig. 8. Its *noise transfer function* (NTF) is given by

$$H_e(z)=\frac{\left(1-z^{-1}\right)^2}{(a_1a_2c_1c_2)z^{-2}+(a_1c_1-2)z^{-1}+1} \tag{5}$$

The coefficients can be chosen to achieve best performance and maintain loop stability [11].

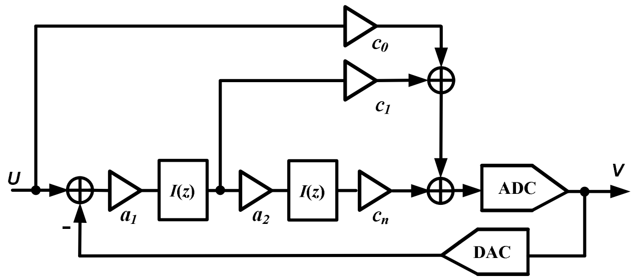


Figure 8 Block diagram of second-order full-feedforward structure.

C. Fast Feedback Loop around the Quantizer

It has been reported that the feedback loop around the quantizer has the effect of alleviating the delay requirement in DSM design [12], [13]. Here, the fast feedback is applied to the full-feedforward KD1S modulator.

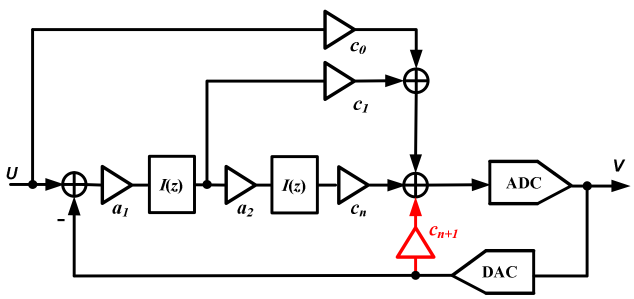


Figure 9. Fast feedback around the quantizer in proposed KD1S modulator.

Fig. 10 shows the SNR drops for different comparator delays, and the fast feedback helps KD1S modulator maintain good performance. In the following section's discussion over the integrators' output levels and the fast feedback proves to be effective in reducing the output swing of integrators.

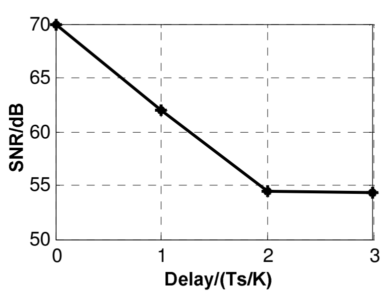


Figure 10. Fast feedback around the quantizer in proposed KD1S modulator.

D. Circuit Block Diagram

In order to achieve the summer in a *discrete-time* (DT) switched-capacitor implementation, the circuits shown on the right-hand side of Fig. 10 are used. The transfer function of these circuits is given by:

$$Y(z)=\frac{\sum_{i=1}^{n}X_i(z)\cdot C_{fi}}{\sum_{i=1}^{n}C_{fi}}=\frac{\sum_{i=1}^{n}X_i(z)\cdot c_i}{\sum_{i=1}^{n}c_i} \tag{6}$$

where C_{fi} is the capacitance in the i-th feedforward loop.

It is noted that in order to realize the true feedforward coefficients c_is, additional amplification $\sum_{i=1}^{n}c_i$ is needed. However, for a single-bit quantizer, the amplitude information is not present, and the amplification circuitry can be omitted [11].

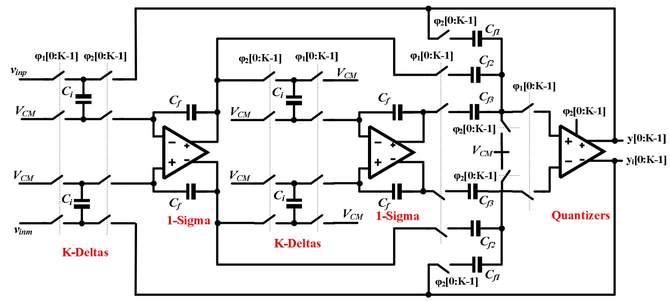
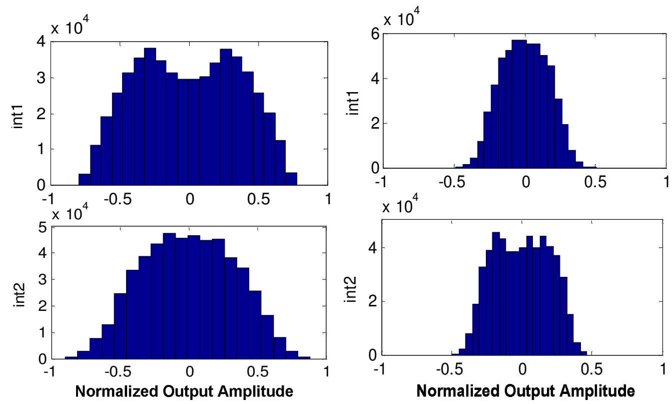


Figure 11 Concise circuit block diagram of proposed KD1S modulator.

In the circuit implementation shown in Fig. 11, the input feedforward path in Fig. 8 is omitted without affecting the noise transfer function, since this path is open when calculating the noise transfer function.

E. Output Levels of the Integrators

The internal signal swing indicates the headroom requirements for the opamps used as integrators in DSM. Reduced internal signal swing allows for more efficient opamp architectures to be used [14] [15].



(a) (b)

Figure 12 Output level histograms of the first and second integrators for a conventional second-oder CIFB modulator (a) and proposed full-feedforward KD1S modulator (b).

Figure 12 shows the histogram of the internal signal swing for the conventional second-order CIFB KD1S modulator and proposed second-order full-feedforward KD1S modulator. The proposed full-feedforward KD1S modulator exhibits reduced output levels in both integrators compared to the conventional topology. This may lead to improved quantizer's overload level for the modulator, and hence better dynamic range. From power perspective, a DSM with less internal signal swing will dissipate less power.

F. Behavioral Simulation Results

The behavioral simulation results for the proposed second-order full-feedforward KD1S with ideal components are illustrated in Fig. 13.

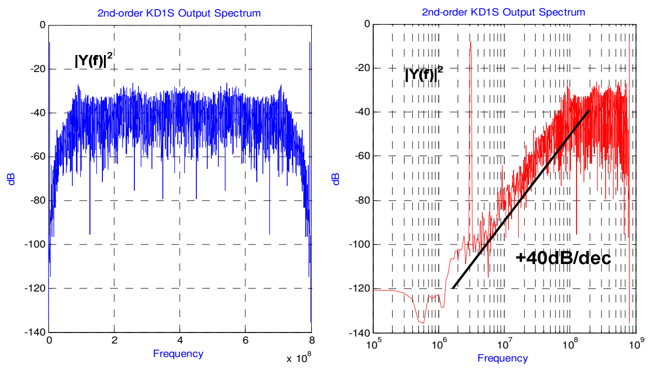


Figure 13 Simulation results (PSD of the output with linear and log frequency axes) for a second-order full-feedforward KD1S modulator using ideal components.

Here K_{path}=8, and a clock frequency (f_s) of 100 MHz is employed. The effective sampling rate $f_{s,new}$ is equal to 800 MHz. The 8 channel digital outputs are post-processed in MATLAB, and the achieved SNR for a signal bandwidth of 6.25 MHz (i.e. $K_{path}\cdot OSR$=64) is equal to 70 dB or 12 bits in resolution. This establishes the true second-order noise shaping in a KD1S modulator.

V. SPICE Simulation Results

The proposed second-order *full-feedforward K-delta-1-sigma modulator* (FFKD1S) with fast feedback around quantizer was simulated in an IBM 130nm technology. The output spectrum of the modulator is shown in Fig. 14. A sinusoidal input with amplitude of 0.8 V pk-pk (V_{DD}=1.2V) and a frequency of 2 MHz is used. The measured SNR(using MATLAB) for a signal bandwidth of 6.25 MHz ($K_{path}\cdot OSR$=64 with $f_{s,new}$ = 800 MHz) is 58 dB which is equivalent to 10-bit of resolution.

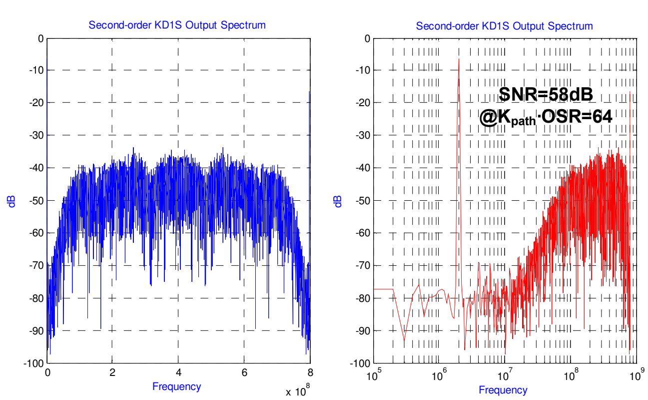


Figure 14 Measured Spectrum and SNR vs. input amplitude plot for the KD1S modulator.

The SNR drop is partially due to the comparator delay and finite unity gain frequency (f_{un}) and finite open-loop gain of the opamp.

VI. Conclusion

The proposed second-order full-feedforward *K*-delta-1-sigma modulator with fast feedback around quantizer exhibits true wideband noise shaping. Simulation results have been presented to corroborate the theory. The topology appears to have significant potential to provide a production-worthy method for implementing high-speed ADCs in nano-CMOS technologies.

References

[1] P. Schvan, et al, "A 24GS/s 6b ADC in 90nm CMOS," *ISSCC Dig. Techn. Papers*, pp. 544-545, Feb. 2008.

[2] K. Poulton, et al., "A 20-GSample/s 8b ADC with a 1-MByte Memory in 0.18-um CMOS," *ISSCC Dig. Techn. Papers*, pp. 318-319, Feb. 2003.

[3] B. Murmann, "A/D Converter Trends: Power Dissipation, Scaling and Digitally Assisted Architectures," Proc. *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 105-112, Sept. 2008.

[4] Verma, A., Razavi, B., "A 10b 500MHz 55mW CMOS ADC," *International Solid-State Circuits Conference*, pp. 84-86, Feb. 2009.

[5] Baker, R.J., "CMOS: Mixed-Signal Circuit Design," 2nd Ed., Wiley Interscience, 2008. Website: http://CMOSedu.com

[6] I. Galton and H. T. Jensen, "Oversampling Parallel Delta-Sigma Modulator A/D Conversion," *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 43, No. 12, pp. 801-810, Dec. 1996.

[7] E.T. King, A. Eshraghi, I. Galton, T. S. Fiez, "A Nyquist-Rate Delta-Sigma A/D Converter, " *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 45-52, Jan. 1998.

[8] Eshraghi, T. S. Fiez, "A Time-Interleaved Parallel ΔΣ A/D Converter," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 50, no. 3, Mar. 2003.

[9] Eshraghi, T. S. Fiez, "A Comparative Analysis of Parallel Delta-Sigma ADC Architectures," *IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 51*, no. 3, Mar 2004.

[10] Saxena, V., Li, K., Zheng, G., and Baker, R.J., "A K-Delta-1-Sigma Modulator for Wideband Analog-to-Digital Conversion," *Proceedings of the 52nd Midwest Symposium on Circuits and Systems*, pp. 411-415, August 2-5, 2009.

[11] Yao, L., Steyaert, M. and Sansen, W., "Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS," Springer, 2006

[12] Z. Li and T. S. Fiez, "A 14 Bit Continuous-Time Delta-Sigma A/D Modulator with 2.5 MHz Signal bandwidth." *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, September 2007.

[13] Hart, A.; Voinigescu, S.P., "A 1 GHz Bandwidth Low-Pass ΔΣ ADC With 20–50 GHz Adjustable Sampling Rate", *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1401-1414, May 2009.

[14] A. Gharbiya and D. A. Johns, "Fully Digital Feedforward Delta-Sigma Modulator," *IEEE PhD Research in Microelectronics and Electronics*, Lausanne, Switzerland, July 25-28, 2005.

[15] S. Kwon and F. Maloberti, "Op-Amp Swing Reduction in Sigma-Delta Modulators," *Proc. IEEE ISCAS*, pp. I-525 – I-528, 2004.