Noise-Shaping Sense Amplifier for MRAM Cross-Point Arrays

Matthew B. Leslie and R. Jacob Baker

***Abstract*—A sensing technique using a voltage-mode architecture, noise-shaping modulator, and digital filter (a counter) is presented for use with cross-point MRAM arrays and magnetic tunnel junction memory cells. The presented technique eliminates the need for precision components, the use of calibrations, and reduces the effects of power supply noise. To obviate the effects of cell-to-cell variations in the array, a digital self-referencing scheme using the counter is presented. Measured experimental results in a 180-nm CMOS process indicate an RMS sensing noise of 20 μV for a 5-μs sense time. Further increases in sense time are shown to increase the signal-to-noise ratio. The current used by the sense amplifier and counter was measured as 10 μA when running at 100 MHz or 10 mA when 1000 sense amplifiers are used with a memory subarray having 1000 bitlines.**

***Index Terms*—Current-mode sensing, magnetic random access memory (MRAM), magnetic tunnel junction (MTJ), noise-shaping modulator, self-referenced sensing, voltage-mode sensing.**

I. Introduction

MAGNETIC random access memory (MRAM) is a promising low-power nonvolatile memory technology that may one day supplant FLASH and DRAM. Cross-point topology MRAM arrays [1] result in higher density memories when compared to memory architectures that use isolation devices. Theoretically, the cross-point memory cell size can be reduced to $4\mathrm{F}^2$ in two dimensions, and below $4\mathrm{F}^2$ in three dimensions [2]. However, sensing schemes for cross-point MRAM arrays are challenging due to both the absence of an isolation device and the associated sneak resistance paths of nonselected cells [3]. In these sensing techniques, the potential across the sneak resistance is driven to zero while current through the accessed memory cell is sensed (called current-mode sensing). This work describes sensing circuitry based on the principle of noise-shaping where the voltage on a digit line is sensed (called voltage-mode sensing). The architecture presented in this work, including a self-referencing technique, makes cross-point arrays using MRAM considerably more practical.

II. Cross-Point Array

The magnetic tunnel junction (MTJ) cell is the fundamental component of a cross-point MRAM array. Each MTJ cell is composed of (at least) a pinned magnetic layer, a tunneling oxide, and a free magnetic layer, as seen in Fig. 1. The magnetic field of the free layer can orient either parallel or antiparallel to that of the pinned layer. Parallel programmed cells exhibit relatively less resistance, R_P, than that of an antiparallel programmed cells, R_{AP}. Experimental results have documented magnetoresistive changes from 20% to 50% in MTJs [4]. Typically, MTJs used in cross-point arrays utilize thicker tunnel oxides, and thus, larger resistances (for example, $R_P = 800$ kΩ and $R_{AP} = 1$ MΩ) than MRAMs using cells with isolation devices (a cell with one transistor and one magnetoresistance junction, 1T1MTJ).

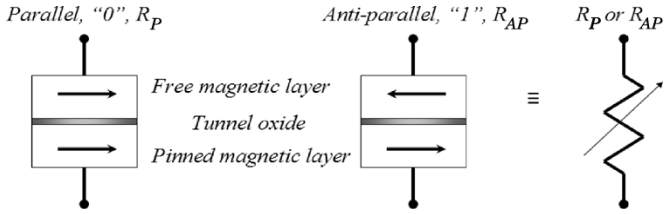

Fig. 1. Resistive memory cell using a magnetic tunnel junction.

III. Current- and Voltage-Mode Sensing

A schematic of an N by M cross-point MTJ array is shown in Fig. 2. Fig. 3 shows the equivalent schematic representation. The key thing to notice is the loading of the sneak resistances, the parallel combination of the MRAM cells, on the bitline.

A. Current-Mode Sensing

Fig. 4 shows a current-mode sense topology used in MTJ cross-point arrays [5]. The active row line is driven to ground while all unused row lines are driven to, using the example voltage in the figure, 500 mV. Ideally then, the voltage across the sneak resistance is zero (both sides are held at 500 mV). The current through the cell being sensed charges a capacitor. When the capacitor is charged to an arbitrary value, the comparator output goes high and the counter stops.

This topology has several problems that render it impractical. To begin, driving all of the unused row lines in the array up to 500 mV results in a considerable waste of power. Next, the operational amplifier (op-amp) in the sensing circuit tries to hold the voltage across the sneak resistance to zero. In a practical circuit, the op-amp will have both an offset and finite gain. Even if, through calibrations (which are required using this technique), the offset can be limited to 1 mV, the effects are to limit both the size of the array that can be used and the sense's signal-to-noise ratio (SNR). Note also that the length of the sense time is finite

Manuscript received March 13, 2005; revised December 5, 2005. This work was supported by Micron Technology, Inc.

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Digital Object Identifier 10.1109/JSSC.2005.864103

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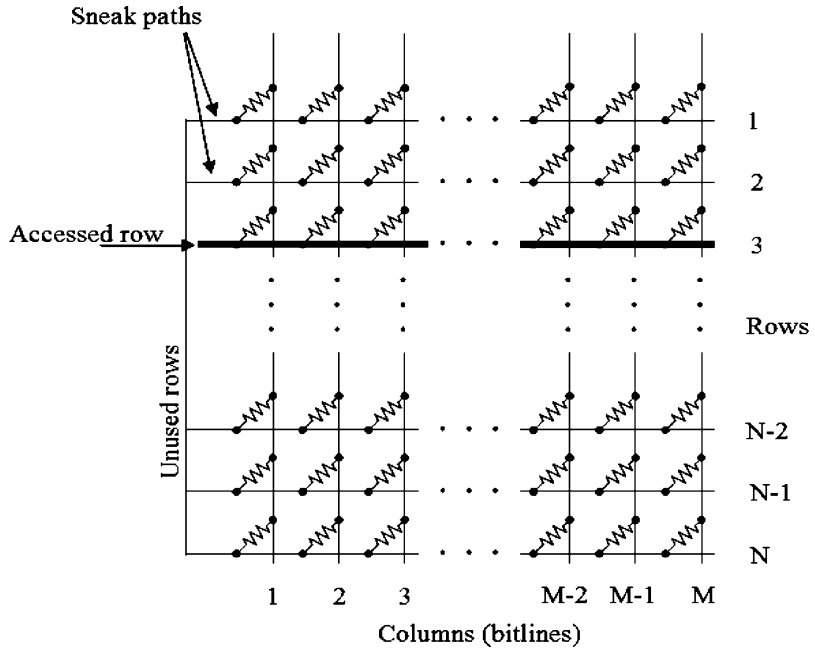


Fig. 2. Schematic representation of a cross-point array of MTJs.

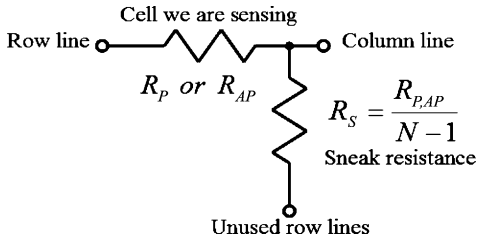


Fig. 3. Equivalent schematic of the resistances seen on a bitline in the cross-point array.

(unlike the scheme we have developed here using voltage-mode techniques). If, with process, voltage, or temperature shifts, the MTJ's resistance or the op-amp/capacitor change, then the sense time changes. Using voltage-mode techniques, the sense time can be infinite with the SNR ultimately limited by the forward gain of the sense amplifier and the number of bits in the counter.

Finally, the current-mode sense technique has limitations due to integrating flicker ($1/\mathrm{f}$) noise [6]. Integrating $1/\mathrm{f}$ noise (an output power spectral density with a $1/\mathrm{f}^3$ shape) results in an RMS value of noise that increases linearly with sense time. As discussed in Section IV, sensing for longer periods of time does not result in an increase in the measured SNR.

B. Voltage-Mode Sensing

Fig. 5 shows the proposed sensing topology using noise-shaping and voltage-mode techniques. To sense a cell's logic value (its resistance) using voltage-mode sensing, a voltage (here 500 mV) is applied to the row line. The column line is connected to the input of the sense amplifier made with a noise-shaping modulator and a counter. Unlike the current-mode techniques, the power is minimized by driving only a single row line in the array above ground. Notice that if there is noise on the row line voltage, it is desensitized by the voltage divider formed with the sneak resistance. Significant variations on the row line voltage have little effect on the column line voltage. This is not the case in the current-mode techniques seen in Fig. 4. A mere 1-mV change in the current-mode sense amplifier's column line can drastically affect the sense and will result in errors. Using the noise-shaping amplifier, our sense amplifier output can run indefinitely, ultimately limited by the number of bits in the counter. An important thing to note is that the signal transfer function of a noise-shaping (modulator) amplifier is a constant at DC [7]. The output $1/\mathrm{f}$ noise is referred directly back to the sense amplifier's input. Sensing for longer periods of time increases the SNR of the sense operation (we are not integrating the $1/\mathrm{f}$ noise as discussed in Section IV).

IV. Noise-Shaping Sense Amplifier

Fig. 6 shows the block diagram of the noise-shaping sense amplifier and its transfer function (including both the signal and noise transfer functions). The reader unfamiliar with noise-shaping techniques, sometimes called sigma-delta or delta-sigma techniques, can refer to [6, ch. 17] for an introduction, or [7, ch. 32] for a more advanced description of the methods.

A. Circuit Design Considerations

The desired input signal (column line voltage) to the sense amplifier is a DC voltage. At DC, the signal transfer function, as seen in Fig. 6, reduces to a ratio of MOSFET transconductances, g_{m1}/g_{m3}. This ratio can be used to amplify the input signal for faster sensing times. The circuit implementation of the modulator is seen in Fig. 7. Two operational transconductance stages are required to keep the forward gain through the modulator large. The gain $-g_{m1}$ is realized through a pMOS differential amplifier and wide-swing folded-cascode operational transconductance amplifier (OTA). A pMOS differential

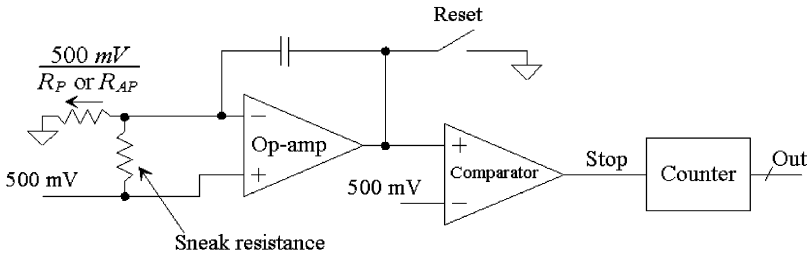


Fig. 4. Current-mode sensing; the traditional method used in cross-point arrays.

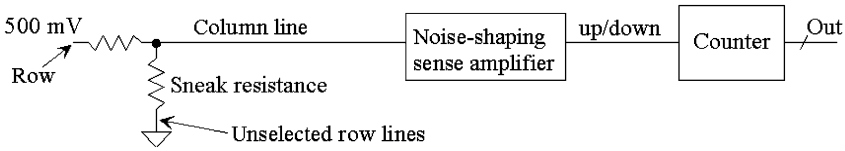
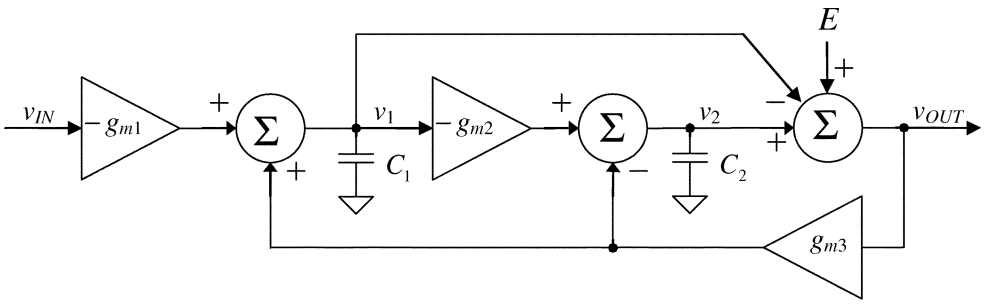


Fig. 5. Voltage-mode sensing (this work).



$$v_{OUT} = v_{IN} \cdot \overbrace{\frac{\frac{g_{m1}}{C}s + \frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + g_{m3}\frac{C_1+C_2}{C_1C_2}s + \frac{g_{m2}g_{m3}}{C_1C_2}}}^{\text{Signal Transfer Function}} + E \cdot \overbrace{\frac{s^2}{s^2 + g_{m3}\frac{C_1+C_2}{C_1C_2}s + \frac{g_{m2}g_{m3}}{C_1C_2}}}^{\text{Noise Transfer Function}}$$

Fig. 6. Block diagram and transfer function of a noise-shaping sense amplifier.

amplifier is used because its input common-mode voltage includes ground. The gain $-g_{m2}$ is the result of an nMOS differential amplifier fed to a folded-cascode stack identical to the stack used in the first stage. A clocked comparator with an S-R latched output compares v_1 and v_2. Through the feedback, the comparator keeps these voltages nearly equal. The amplified input signal is changed into a current, $g_{m1} \cdot v_{\text{in}}$, that drives the capacitor C_1 and thus changes v_1. Similarly, a current, $g_{m2} \cdot v_1$, drives C_2, further amplifying the input signal (and thus the large forward gain seen by the input signal). Through the feedback around the sensing circuit, the comparator controls a feedback current to subtract out, on average, the input signal current generated by the input voltage to keep the voltages across C_1 and C_2 constant. The current feedback and controlled by the comparator has a gain of g_{m3}. This current comes from the gate-enabled current source/sink driven by the output of the comparator.

The output of the noise-shaping amplifier is a digital waveform with a DC component equal to its input multiplied by the gain at DC (g_{m1}/g_{m3}). However, to obtain this value as a digital word the waveform must be filtered. The up/down counter seen in Fig. 5 performs this function. The output of the counter is initialized to zero at the beginning of the sense. The one-bit output of the sense amplifier is fed to the input of the counter. This counting scheme integrates (low-pass filters) the digital bitstream output of the sense amplifier [7] (the counter behaves as an averaging filter with a sinc-shaped frequency response).

B. Noise

The $1/\text{f}$ noise present in MOS technology is a serious concern for small-amplitude measurements [6]. Conventional sense topologies (current-mode sensing) integrate flicker noise resulting in an output power spectrum proportional to $1/\text{f}^3$. As a result, the SNR for a given sense cannot be increased with increasing sense time (the SNR moves toward a constant value with increasing sense time). To show this is indeed the case, consider calculating the increase in the desired signal

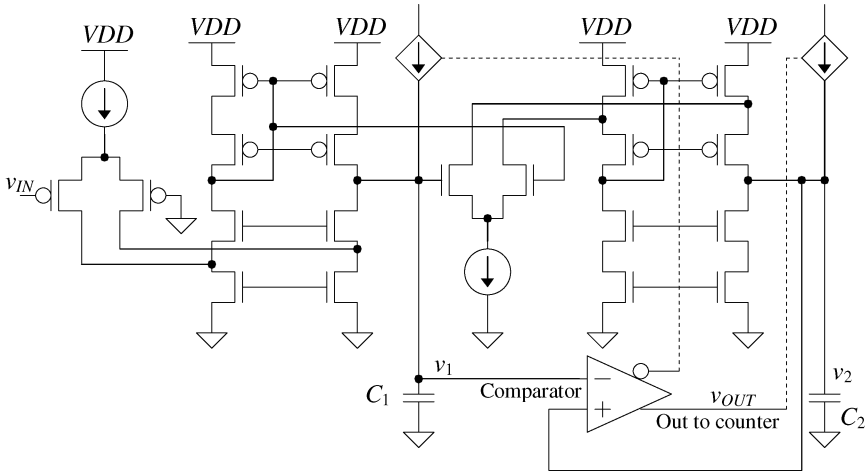


Fig. 7. Schematic representation of the noise-shaping sense amplifier.

amplitude, S, with sensing time, T, when using an integrator (Fig. 4):

$$S = \int_0^T V_{\rm DC} \cdot dt = V_{\rm DC} \cdot T. \quad (1)$$

The input-referred $1/\mathrm{f}$ noise for a MOSFET is characterized in the frequency domain using a power spectral density (PSD) of

$$V_{1/f}^2(f) = \frac{\rm FNN}{f} \text{ with units of } \frac{V^2}{\rm Hz}. \quad (2)$$

The numerator, called the flicker noise numerator (FNN), is a constant value but dependent on biasing conditions, device size, and the process technology used. When MOSFETs are used to form an integrator, their input-referred $1/\mathrm{f}$ noise is integrated along with the desired signal. To calculate the RMS value of the integrator's output noise spectrum, we integrate the PSD over the frequency spectrum of interest (ranging from a low frequency, f_L, to a high frequency, f_H) using

$$V_{\rm RMS} = \sqrt{\int_{f_L}^{f_H} V^2(f) \cdot df} = \sqrt{\int_{1/T}^{\infty} V^2(f) \cdot df}. \quad (3)$$

As seen in this equation, we can get an estimate for the RMS noise, for a finite measurement time, by replacing the lower integration boundary, f_L, with $1/T$ (where again T is the sense time), and then taking the upper integration boundary to infinity. The output noise PSD for the integrator in Fig. 4 is estimated using

$$V_{\rm out}^2(f) = \left|\frac{1}{j\omega RC}\right|^2 \cdot \frac{\rm FNN}{f} = \frac{K}{f^3}. \quad (4)$$

The integrator's output RMS noise is then calculated using (3) as

$$V_{\rm RMS,out} = \sqrt{\int_{\frac{1}{T}}^{\infty} \frac{K}{f^3} \cdot df} = \sqrt{\frac{K}{-2}(f^{-2})_{\frac{1}{T}}^{\infty}} = \sqrt{\frac{K}{2}} \cdot T. \quad (5)$$

The SNR for the current-mode sensing circuit in Fig. 4 can be estimated using (1) and (5) as

$$\mathrm{SNR} = \frac{V_{\rm DC} \cdot T}{\sqrt{(K/2) \cdot T}} = \text{a constant value independent of measuring time.} \quad (6)$$

Using noise-shaping (Fig. 5), the input-referred $1/\mathrm{f}$ noise is simply passed to the output of the modulator (the noise-shaping modulator's signal transfer function is a constant at DC as seen in Fig. 6) without integration (important). Because the input-referred $1/\mathrm{f}$ noise is not integrated, we can rewrite (5) as

$$V_{\rm RMS,out} = \sqrt{\int_{1/T}^{f_H} (K/f) \cdot df} = \sqrt{K \cdot (\ln f_H + \ln T)} \quad (7)$$

where we have used the realistic case that f_H is not infinite and thus $\sqrt{\ln(f_H)}$ stays bounded. For example, if $f_H = 1$ kHz then the term $\sqrt{\ln(f_H)}$ is 2.62, while if $f_H = 1$ GHz then it is 4.55. Using noise-shaping sensing techniques, we get an SNR of

$$\mathrm{SNR} = \frac{V_{\rm DC} \cdot T}{\sqrt{K \cdot (\ln f_H + \ln T)}} = \text{a value that can increase with measurement time.} \quad (8)$$

For the majority of the practical situations the SNR will increase somewhat linearly with T. The importance of this is that to increase the sense's SNR when using the voltage-mode techniques developed in this paper, we simply sense for a longer period of time (this is verified experimentally later). Unlike most memory sense techniques, the one presented here, because of the feedback involved, can run indefinitely (the sense is ultimately limited by the forward gain of the sense amplifier or the number of bits in the counter).

V. Self-Referencing

Self-referencing has been identified as an important component for successfully implementing memory using the MTJ [8]. The MTJ cell sensing is completely (digitally) self-referenced in this work. This is important for eliminating the effects of cell-to-cell variations (absolutely critical for a production worthy memory technology). The desired cell is first read

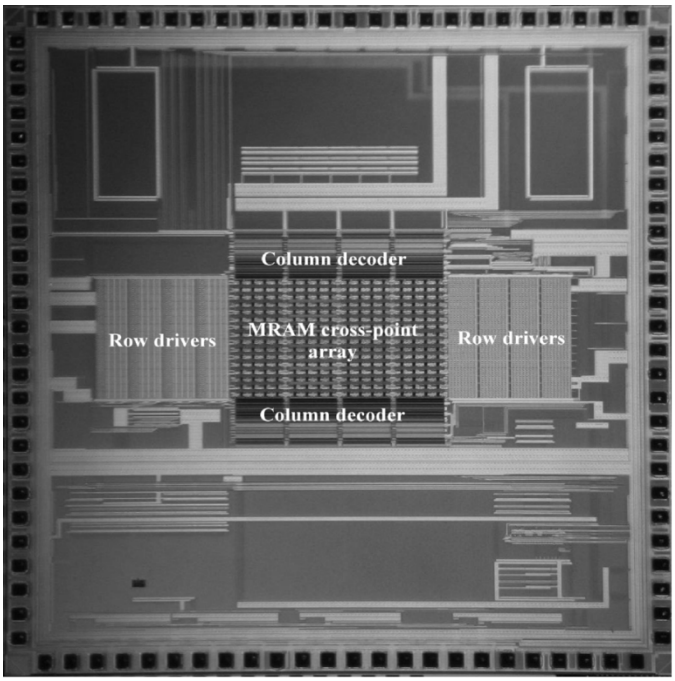


Fig. 8. MRAM test chip.

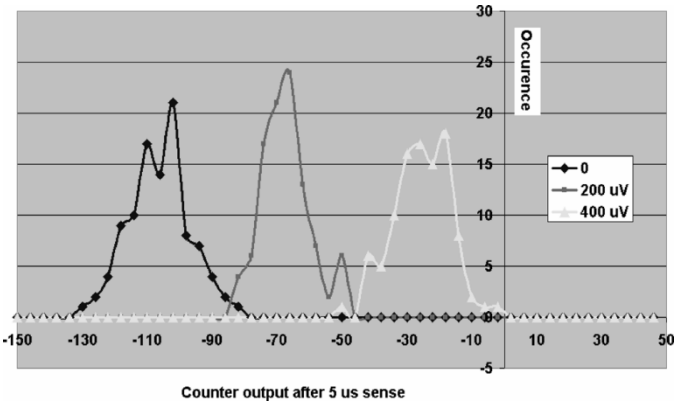


Fig. 9. Experimental results using the noise-shaping sense amplifier.

twice, which results in a digital word on the counter's output. The counter's up/down input is then inverted so it may count in the opposite direction. Next, a known logic 0 is written to the cell and read. Then a known logic 1 is written to the cell and read. Because a logic 1 produces a higher count than a logic 0, if the final digital word stored in the counter is positive (MSB is 1) the original cell stored in memory was a logic 1. If it is negative (MSB is 0), the original cell was a logic 0. After the sense, the cell is rewritten with its original value.

To present a simple example of self-referencing, let us assume counter output codes 22 and 20 correspond to MRAM bits with logic 1 and 0 values, respectively. Further, let us assume that we are sensing a cell in a logic 0 state. We begin by sensing the cell twice, resulting in a counter output code of 40. We then flip the up and down signals on the counter and write a known 0 to the cell. At the end of this sense, the counter contains a value of 20. We then write a known 1 into the cell and sense again. The counter's output then goes to -2, a negative value which indicates the original value stored in the cell was a logic 0. We then rewrite the cell with a logic 0.

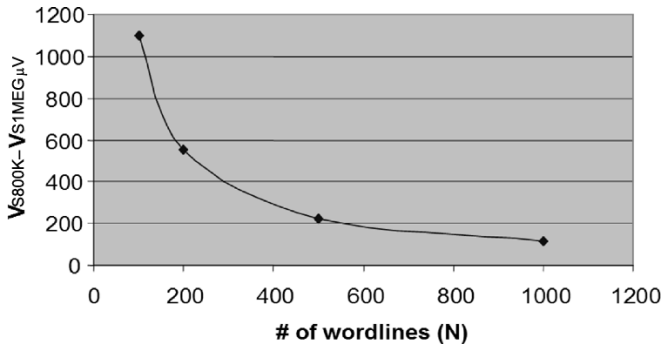


Fig. 10. Sensed signal plotted against the number of wordlines (rows) in the array.

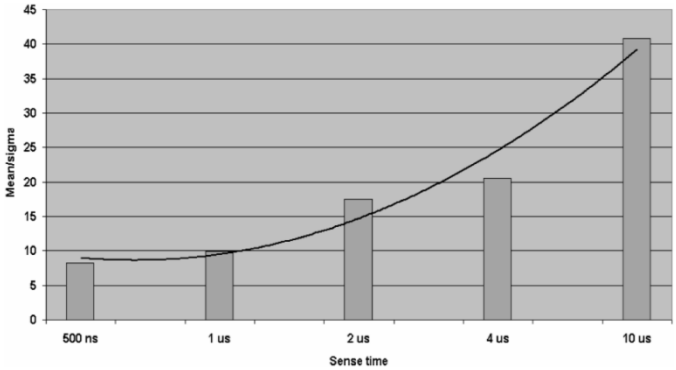


Fig. 11. Measured SNR increases with the sense time.

Self-referencing neutralizes the errors introduced by input offset voltages and MTJ resistance inconsistencies due to process-inherent tunnel oxide thickness variations. In either case, the error will be present in the original (unknown) sense and also the second (known) sense. Because the error from either problem is constant for a given cell during a given sense, the errors simply subtract out from the measurements.

VI. Experimental Results

The prototype sense amplifiers were fabricated in a 180-nm process. Fig. 8 shows a photograph of the test chip. The current draw from each active sense amplifier was 10 μA when operating with a clock frequency of 100 MHz (the clock is used by the comparator and counter). Fig. 9 shows typical measured results (wafer level, where both input and output signals were applied through a probe card). For characterization, the sense amplifier's input signal was generated through an on-chip 1000:1 voltage divider (not with the MRAM array in place). The *y* axis in Fig. 9 is a histogram of the counter output codes. The RMS value of the noise, for this 5-μs sense, is roughly 6 counts corresponding to 20 μV (RMS) of input-referred noise. To get an idea if this level of noise is acceptable, Fig. 10 plots the difference in the column voltages (on the *y* axis) against the number of word lines (rows). To understand how Fig. 10 was generated, refer to Fig. 3. The active row line is driven to 500 mV while the unused row lines are grounded. The cell being sensed has a value of 800 k (parallel) or 1 MEG (antiparallel) while the sneak resistance is set to 900 k$/(N-1)$ where N is the number of rows in the memory array. Note that the sneak resistance can vary from 800 k$/(N-1)$ to 1 MEG$/(N-1)$. It should be noted

that while the sneak resistance varies with the data stored in the memory, it is a constant during any sense operation (we are not changing the data associated with the memory cells connected to the unused rows during a sense operation, and thus the sneak resistance does not vary).

Finally, Fig. 11 shows how the measured SNR increases with sensing time when using voltage-mode techniques (as discussed in detail in Section IV). Here we indicate the increase in SNR with sense time by taking the ratio of the mean of the counter's output to the standard deviation (sigma) for a large number of sense operations.

VII. Conclusion

A new method for sensing in large MRAM cross-point arrays based on voltage-mode techniques was proposed and experimentally verified. The technique, because of the simple signal processing used, reduces the effects of word line voltage variations (noise on the word lines), flicker noise, and thermal noise on the sense's SNR. It was experimentally shown that to increase the SNR, all that is needed is additional sensing time. A simple digital self-referencing scheme was proposed that eliminates the effects of significant cell-to-cell variations.

Acknowledgment

The authors would like to thank Q. Harvard, R. Hilton, T. Holman, J. Osborne, F. Perner, M. Seyyedy, K. K. Smith, and M. Tuttle for helpful discussions during the course of this work's development.

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From 1981 to 1987, he was in the U.S. Marine Corps Reserves. From 1985 to 1993, he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada test site. During this time, he designed over 30 electronic and electro-optic instruments including high-speed (750 Mb/s) fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1993 to 2000, he was a faculty member in the Department of Electrical Engineering at the University of Idaho, Moscow, ID. In 2000, he joined a new electrical and computer engineering program at Boise State University, Boise, ID, where he is currently a Professor and Chair of the department. Also, since 1993, he has consulted for various companies and laboratories including Micron Technology, Amkor Wafer Fabrication Services, Tower Semiconductor, Rendition, Lawrence Berkeley Laboratory, and the Tower ASIC Design Center. He is the author of the books *CMOS: Circuit Design, Layout, and Simulation* and *CMOS: Mixed-Signal Circuit Design*. His research interests are in the areas of CMOS mixed-signal integrated circuit design and the design of memory in new and emerging fabrication technologies.

Prof. Baker holds over 100 granted or pending patents in integrated circuit design. He is a member of Eta Kappa Nu and a licensed Professional Engineer. He was a co-recipient of the 2000 Prize Paper Award of the IEEE Power Electronics Society.