Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics

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ABSTRACT

CMOS NAND gate circuit performance degradation caused by a single pMOSFET wearout induced by constant voltage stress in 2.0 nm gate dielectrics is examined using a switch matrix technique. The NAND gate rise time is found to increase by approximately 64%, which may lead to timing errors in high frequency digital circuits. The degraded pMOSFET reveals that a decrease in drive current by 41% and an increase in threshold voltage by 18% are directly proportional to an increase in channel resistance, thereby substantially increasing the NAND gate circuit timing delay.

INTRODUCTION

Inverter circuit degradation attributed to dielectric wearout or breakdown mechanisms have received recent attention [1-8], yet reports on physical (i.e., not simulated) oxide degradation effects on other logic gates, such as the NAND gate, are minimal. Furthermore, much of the work on inverter reliability has focused on the change of dc voltage transfer characteristics following circuit stressing without investigating the time domain [1, 2, 7, 8]. In these studies, individual MOSFETs cannot be examined, so the type and amount of degradation to one or both MOSFETs can only be inferred. This is not the case with techniques (switch matrix techniques) developed by several of the authors of this paper in which individual MOSFETs in an inverter can be directly characterized following circuit stress [3, 6]. The switch matrix technique has also been used to degrade a single MOSFET (or both MOSFETs) and examine the effect on inverter performance [9]. In both studies, the circuit degradation in the voltage-time (V-t) domain is examined and directly correlated to MOSFET parameters degradation. This has yet to be investigated in other logic gates including NAND gates. Hence, the switch matrix technique is used to study time domain NAND gate reliability in this paper.

It has been proposed by Ogas *et al.* that traditional gate oxide breakdown (GOB) events, such as soft breakdown (SBD) or hard breakdown (HBD), need not occur for circuit performance to deteriorate [4]. Similarly, Carter *et al.* suggest logic circuits are affected dynamically by gate oxide degradation through their simulation of NAND gates and full adder circuit models [10]. Their analysis presents data which depicts a progressive nature of GOB resulting in timing delays of NAND circuits and propagation of these timing delays through the logic path of a full adder circuit [10]. Furthermore, according to simulations by Hawkins *et al.*, as technology nodes continue to decrease, IC parameter variance becomes a greater concern for the timing of logic circuits [11].

Consequently, as transistor gate dielectric thickness (t_{OX}) decreases, device speed increases yet results in detrimental effects such as increased gate leakage current, increased defect generation, and ultimately earlier dielectric breakdown [12]. Therefore, as circuit engineers continue to design with thinner oxides, it is important to examine circuit performance under stressed conditions to identify the most susceptible components to dielectric degradation. This study investigates the NAND gate circuit in response to the progressive breakdown nature of devices with t_{OX} of 2.0 nm. Of particular interest is the reliability assessment of low-level degradation, or wearout, to help determine a critical limit where digital circuits fail through circuit and device characteristics. This paper examines the effect of wearout in one pMOSFET on NAND gate circuit performance.

EXPERIMENTAL

The metal oxide semiconductor (MOS) devices used in this study were fabricated using 0.1 μm CMOS technology. Previous work with MOSFET devices with t_{OX} of 2.0 nm and an oxide area (A_{OX}) of $1x10^{-6}$ cm^2 provided a reference for expected degradation and breakdown regimes [4]. This paper focuses on the low leakage degradation regime (i.e., prior to breakdown), otherwise known as wearout. Wearout is defined as the cumulative effects of oxide degradation over five constant voltage stress (CVS) periods.

The nMOSFET and pMOSFET devices in this study have an A_{OX} of $1x10^{-8}$ cm^2 with a width and length of 10 μm and 0.1 μm, respectively. A novel switch matrix technique (SMT) is used to configure the NAND gate circuit at the wafer level [3, 4]. A CVS technique similar to previous work with inverter circuits is utilized, in which -4.0 V is applied to the gate of the pMOSFET at stress periods of 600 seconds (Fig. 1) in order to induce gate oxide wearout in one pMOSFET of the NAND gate (Fig. 2) [4]. The remaining three MOSFETs are not stressed. After each stress period, device characteristics and NAND gate circuit time domain response are measured. The measured device parameters include gate leakage current (I_G-V_G), maximum drain current ($I_{DRIVE,MAX}$), transconductance ($G_{M,MAX}$), threshold voltage (V_{TH}) and off-

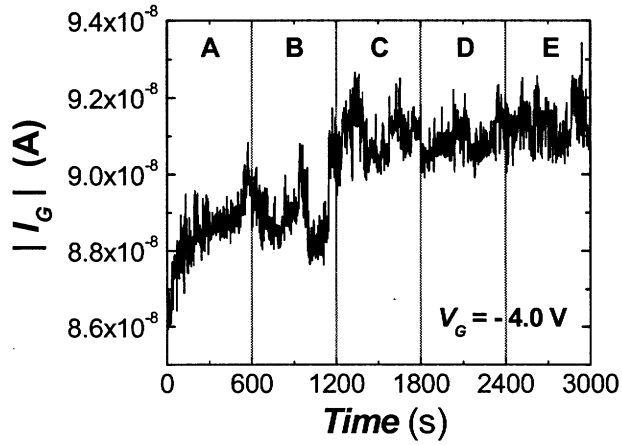

Fig. 1: Constant voltage stress technique indicating the wearout regime. The letters (A-E) every 600s designate where CVS was stopped and circuit and device characteristics were obtained.

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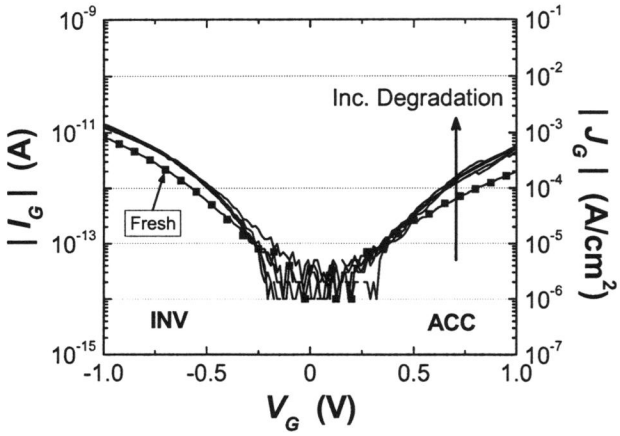
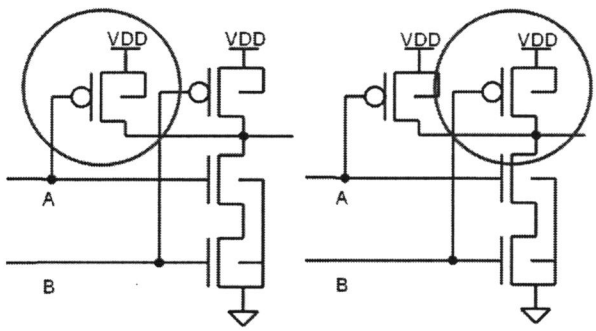


Fig. 2: Gate leakage current response of the degraded pMOSFET attributed to CVS as indicated in Fig. 1.



Position 1 **Position 2**

Fig. 3: NAND gate circuits indicating the position of degraded pMOSFET.

Table I: Possible input configurations for the NAND gate indicating position and I/O state. Shaded regions illustrate logic with critical timing delays for Configurations 1-3 and 2-1.

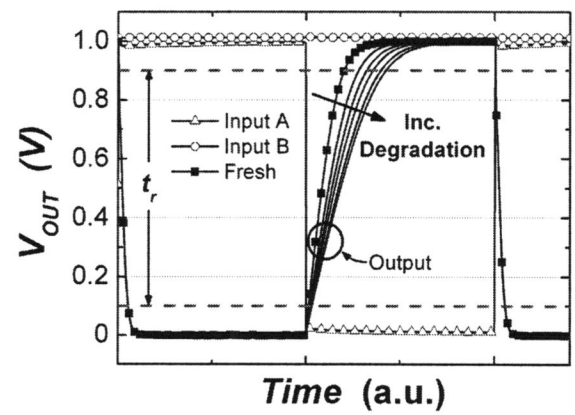
Configuration		Input/Output			
		1	2	3	4
Position 1	Input A	VDD	GND		
	Input B			VDD	GND
	Output	0,1	1	0,1	1
Position 2	Input A	VDD	GND		
	Input B			VDD	GND
	Output	0,1	1	0,1	1

current (I_{OFF}). The NAND gate response is examined for both pMOSFET positions (Fig. 3) in all four input/output (I/O) states (i.e., configuration position # - I/O state #) shown in Table 1. The test and measurement instrumentation used are described elsewhere in [6], with the exception of an additional probestation and eight micropositioners necessary to construct a NAND gate circuit.

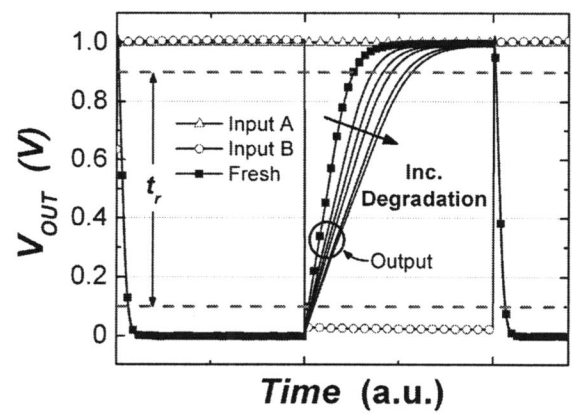
RESULTS AND DISCUSSION

NAND Circuit:

Configuration 1-3 and configuration 2-1 are the only two configurations that exhibit an effect from pMOSFET oxide wearout. Fig. 4 shows the NAND V-t response for the degraded pMOSFET configurations 1-3 and 2-1. The NAND V-t response shows an increase in rise time (t_r) ranging from 64.2% with a standard deviation of ±17.5% for configuration 1-3, and 62.7% with a standard deviation of ±20.2% for configuration 2-1. Previous work on inverter reliability by Stutzke *et al.* shows the pMOSFET is the "pull-up" device, thereby affecting t_r, while the nMOSFET is the "pull-down" device, which affects fall time (t_f) [3]. Since only the pMOSFET experiences wearout, a change in t_f is not expected nor is observed. This follows the results of undamaged nMOSFET response in inverters [4]. Additionally, results observed for wearout support the work of Carter *et al.*, in which an increased time delay is simulated in the NAND gate time-domain response (Fig. 4) for increased wearout [10].



a. Configuration 1-3



b. Configuration 2-1

Fig. 4: Characteristic NAND gate V-t measurements (degradation fresh to E) as a result of wearout in one pMOSFET indicated by (a) Configuration 1-3 or (b) Configuration 2-1.

MOSFETs:

We have shown that pMOSFET wearout causes a significant change in NAND gate circuit response. Therefore, the pMOSFET characteristics are examined to establish the cause of the large change in t_r. The I_G-V_G data in (Fig. 2) suggests that traditional breakdown events have not occurred, since less than one order of magnitude of leakage current is observed. The CVS results (Fig. 1) substantiate these observations. However, it should be noted that a progressive increase of current is observed in the CVS test, which may indicate progressive breakdown [13].

With increased wearout, the pMOSFET DC characteristics show signs of degradation. These changes include a decrease in $I_{DRIVE,MAX}$ (Fig. 5) by 41.0% (± 5.4%), an increase in V_{TH} (Fig. 6) by 18.3% (± 3.6%), and a decrease in $G_{M,MAX}$ (Fig. 6) by 24.2% (± 3.9%). Additionally, a decrease in I_{OFF} (Fig. 7) by 76.6% (± 12.6%) is observed. The above results indicate for the same gate voltage (V_G), the drain current (I_D) is less in a degraded device than in a fresh device (Fig. 6). These changes in parameters can be correlated to a change in channel resistance (R_{CH}).

The drain current of a short-channel MOSFET operating in the triode region can be modeled with the equation [14]:

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}\left(V_G - V_{TH} - \frac{V_D}{2}\right)V_D \frac{1}{1+\left(\frac{V_D}{\varepsilon_{sat} L}\right)} \qquad (1)$$

where μ_{eff} is the effective mobility of carriers measured in the channel, C_{ox} is the oxide capacitance, W is the width of the oxide, L is the length of the oxide, V_G is the gate voltage, V_{TH} is the threshold voltage, V_D is the drain voltage, and ε_{sat} is the electric field at velocity saturation. By taking the reciprocal of the derivative of equation (1) with respect to V_D, we can obtain the channel resistance of a triode-operating MOSFET, R_{CH} [15]:

$$R_{ch} = \frac{2\left(\varepsilon_{sat} L + V_D\right)^2}{\mu_{eff} C_{OX} W \varepsilon_{sat}\left[V_D^2 + 2\varepsilon_{sat} L\left(V_G - V_{TH} - V_D\right)\right]} \qquad (2).$$

If V_D is assumed small, the ε_{sat} terms can be canceled to give R_{CH} similar to the long channel model [15]. The channel resistance is estimated as:

$$R_{CH} \approx \frac{L}{\mu_{eff} C_{OX} W\left(V_G - V_{TH}\right)} \qquad (3).$$

Equation (3) can be used to estimate the channel resistance in the short channel devices used in this study. From equation (3), it is determined that R_{CH} is a function of L, W, μ_{eff}, C_{OX}, and V_{TH}. For this study, L and W are constant. If μ_{eff}, which is optical phonon dominated in the velocity saturation regime, is assumed to be constant across the short channel device and C_{OX} is assumed to change little with wearout, then the majority influence on R_{CH} is V_{TH}. Therefore, R_{CH} is inversely proportional to V_G - V_{TH}. If the gate voltage remains constant while V_{TH} is increasing, the total value of V_G - V_{TH} will decrease thereby resulting in an increase in R_{CH}. Furthermore, Fig. 6 shows that the $G_{M,MAX}$ not only decreases with wearout, but shifts to more negative voltages indicative of a V_{TH} shift in the same direction which correlates to an R_{CH} increase. Inherently, $I_{DRIVE,MAX}$ is inversely proportional to R_{CH}. As $I_{DRIVE,MAX}$ is decreasing, R_{CH} is increasing, as indicated by Fig 5. Additionally, if C_{ox} is decreasing with wearout, R_{CH} will increase according to equation (3). Ultimately, less channel carriers are present and the effective channel resistance is greater in a device that has experienced wearout.

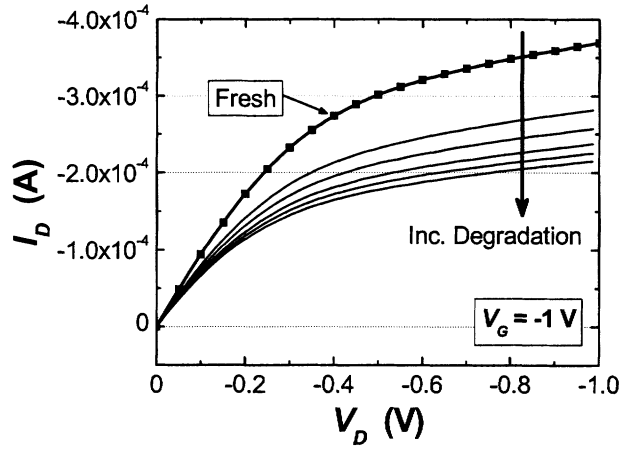


Fig. 5: Typical results (degradation fresh to E) showing a decrease in drive current with increasing wearout in one pMOSFET of the NAND gate.

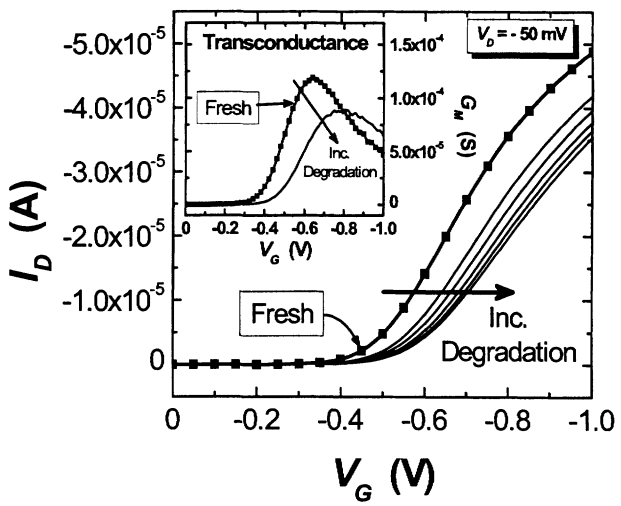


Fig. 6: Typical results (degradation fresh to E) showing an increase in threshold voltage with increasing wearout in one pMOSFET of the NAND gate. The inset illustrates the corresponding decrease and shift to more negative voltages of the maximum transconductance response.

The observed increase in R_{CH} of the pMOSFET directly influences the operation of the NAND logic circuit. The correlation between the t_r of the NAND gate circuit and the R_{CH} of the MOSFETs in the circuit is given by [15]:

$$t_r = (2.2) \cdot R_{CH} \cdot C_l \qquad (4)$$

where t_r is the rise time of the V-t response and 2.2 is a constant based on the t_r calculation from 10% to 90% of the output voltage of a simple RC circuit. The load capacitance, C_l, includes the combined output capacitance of all the MOSFETs in the circuit as well as the system capacitance. It has been experimentally verified that C_l remains constant and does not affect the experimental results. From

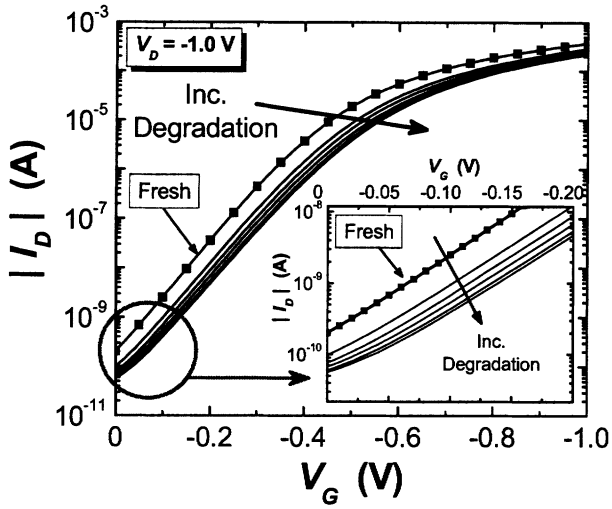


Fig. 7: Typical results (degradation fresh to E) showing a decrease in off current with increasing wearout in one pMOSFET of the NAND gate. The inset illustrates the corresponding decrease in the I_{OFF} regime.

equation (4) it is determined that t_r is directly proportional to R_{CH}. Thus, if a pMOSFET of a NAND circuit exhibits wearout which causes R_{CH} to increase, then the t_r of the NAND circuit will increase. Similar results obtained through the study of inverter circuits demonstrate pMOSFET wearout is responsible for increased t_r [4]. Ultimately, the increase in rise time may affect the critical timing path of digital logic circuits such as clocked registers, which depend on precise timing to function properly.

CONCLUSION

The results reported for wearout in one pMOSFET of a NAND gate circuit indicate a substantial increase in t_r attributed to an increase in channel resistance. These changes in rise time may dramatically affect the ability of the NAND gate to execute logic properly, particularly in applications requiring high switching speeds.

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Questions and Answers

Q: Is the 2.0 nm oxide nitrided?
A: No

Q: Is the degradation recoverable or is it permanent?
A: The degradation is permanent, but we have not tested for recovery at increased temperatures.

Q: Because the model may have limitations, what spice version did you use?
A: We used WinSPICE version 1.05.01.

Q: Did you try to do temperature annealing after stress to see if recovery occurs?
A: No, we currently do not have the capability to perform temperature annealing in our lab. Consequently, no recovery has been observed over a long period of time.