Survey of Oxide Degradation in Inverter Circuits Using 2.0 nm MOS Devices

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ABSTRACT

Degradation in CMOS inverter circuit performance as a result of gate oxide wearout in 2.0 nm pMOSFETs was investigated using a constant voltage stress (CVS) technique. It is demonstrated that inverter performance in the time-domain shows significant deterioration when only the pMOSFET experiences wearout. Experimental results indicate loss of inverter circuit performance in the time-domain given by approximately 36 % to 62 % increase in the rise time. Conversely, DC inverter characteristics are potentially misleading showing that inverter performance was only partially altered. In both cases, inverter degradation is related to the pMOSFET suffering as much as a 40 % decrease in drive current after wearout. This and other large changes in device parameters are compared to a typical logic process revealing that the device parameters are outside the process window. Ultimately, this study suggests that wearout in ultra-thin gate oxides may lead to increased circuit degradation despite the gate leakage current associated with a known circuit component being lower than that required for a typical or traditional BD event to occur.

Keywords—breakdown, circuit degradation, CMOS, MOSFET degradation, inverter, oxide wearout, ultra-thin oxide.

INTRODUCTION

As circuit engineers continue to design with MOSFETs having thinner gate oxides, it is important to examine circuit performance under various stressed conditions to identify the most susceptible components to dielectric breakdown (BD). Furthermore, circuits are designed with specific tolerances built-in; therefore, the overall change in MOSFET parameters may be the issue rather than the BD event. In order for circuit performance to deteriorate, it is not necessary for complete failure of a circuit to occur. Timing interruptions and amplitude changes in the circuit signal need only to take place. Thus, as a component degrades, the circuit tolerances may be surpassed causing circuit disfunction [1]. For example, the "corner" parameters (i.e., process window) of a typical logic process can only tolerate shifts as little as 6 % in drive current (I_{Drive}), 10 % in threshold voltage ($V_{TH,P}$), and 7 % in transconductance ($G_{M,MAX}$) [2]. From a device reliability viewpoint, it is understood that decreasing the transistor gate dielectric thickness, t_{ox}, increases the device speed yet results in detrimental effects such as increased gate leakage current. But the question remains: in what manner do these effects at the device level influence circuit performance characteristics?

Of particular interest is the reliability assessment of BD for determining a critical limit where circuits fail [3]-[5]. Some work has been published examining degradation effects in circuits containing ultra-thin gate oxide devices. The work of Rodriguez *et al.* examined and modeled the effects of BD using a power law (i.e., implying SBD) for SRAM stability [3] and CMOS inverters [6]. In these studies, it is assumed that the integrated effect of both wearout and BD on circuit operation was investigated. Alternatively, there have been reports investigating only BD events in MOSFETs with subsequent comments on the potential effects of only the BD event (choosing not to focus on wearout) in circuits [7]-[8]. However, this survey investigates the degradation in CMOS inverter circuit performance as a result of dielectric wearout in the pMOSFET component with a t_{ox} of 2.0 nm. Wearout is defined in this study as the "cumulative" effects of oxide degradation. Circuit results are then compared to results obtained using 3.2 nm gate oxide pMOSFET devices from previous work [9]. Similar experiments for the nMOSFET are currently being performed.

EXPERIMENTAL SETUP

The devices used for this study are pMOSFETs and nMOSFETs with a length and width of 1 μm and 10 μm, respectively, fabricated using a 0.1 μm CMOS process with a t_{ox} of 2.0 nm. Measurements are taken using an Agilent 4156C precision semiconductor parameter analyzer connected to an Agilent E5250A low-leakage switch matrix. Using switch matrix technology (SMT), a novel technique is employed in which individual devices are connected at the wafer level using eight Cascade Microtech micromanipulators on a probestation enclosed in a Faraday cage. The switch matrix enables configuration of the inverter circuit as well as isolating individual devices for separate characterization and stress testing. A more thorough description of the technique can be found in an earlier work [9]. The algorithm for examining wearout (Fig. 1) begins with characterization of the inverter before stress, defined as the Fresh condition.

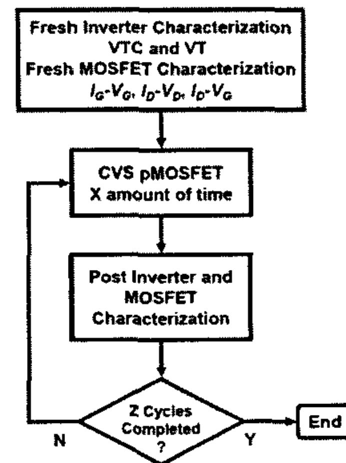

Fig. 1: Algorithm for examining wearout.

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The inverter circuit measurements and the corresponding parameters (see Table I) include, the DC voltage transfer characteristics (VTC) which provide the voltage switching point (V_{SP}), voltage output high (V_{OH}), and voltage output low (V_{OL}) parameters. Also included is the AC inverter time-domain (VT) response in which the parameters rise time (t_r), fall time (t_f), voltage output maximum ($V_{O,MAX}$), and voltage output minimum ($V_{O,MIN}$) are obtained. Fresh device characterization follows, most of which are current - voltage measurements including I_G-V_G (G = gate), I_D-V_D (D = drain), and I_D-V_G. The transconductance is also analyzed (G_M-V_G). The device parameters and their matching device data from which they are extracted are summarized in Table I [10].

Table I: Circuit and device measurements performed and the corresponding parameters.

Circuit Measurement	Circuit Parameters	Device Measurements	Device Parameters
VTC (DC)	V_{SP}, V_{OH}, V_{OL}	I_G-V_G	-
VT (AC)	t_r, t_f, $V_{O,MAX}$, $V_{O,MIN}$	I_D-V_D	I_{Drive} @ $V_D = 1$ V
		I_D-V_G	$V_{TH,P}$
		G_M-V_G	$G_{M,MAX}$

Constant voltage stress (CVS) is applied to the gate of the pMOSFET in cycles of 600 seconds with the drain, source, and well terminals of the pMOSFET shunted to ground, similar to a configuration used by Crupi *et al.* to study BD hardness and location in inversion mode for 2.4 nm pMOSFETs [11]. Several published works were referenced to determine a viable CVS magnitude. Recently, Palumbo *et al.* investigated progressive BD in pMOSFETs with 2.0 nm oxides using CVS at -4.2 V in which no BD runaway was observed [12]. In addition, Lombardo examined the BD transients in nMOSFET devices using CVS in the range of 3.6 to 4.7 V on oxides ranging from 1.5 nm to 2.25 nm [13], in which the authors suggest that a critical voltage (> 4 V) may lead to a decrease in the duration of the BD transient. Incorporating these studies as a point of reference, a CVS voltage of -4 V was utilized. Lower voltages are currently under investigation.

Following each stress cycle, post circuit and device characteristics are obtained (see Fig. 1 and Table I). The total amount of wearout is examined after five cycles are completed, which is referred to in subsequent sections as degradation "Fresh to E".

RESULTS AND DISCUSSION

A typical -4 V CVS result for a 2.0 nm pMOSFET is shown in Fig. 2. Within the area of interest, it is clear that a significant increase in gate leakage current is not observed from t = 0 to t = 3000 s. At t ~ 10,000 s, a noisy appears suggesting progressive BD as seen by Monsieur *et al.* [14] or SBD as suggested by Weir *et al.* [7]. Hard break down (HBD) is indicated by the sudden large increase in leakage current at t ~ 20,000 s. The noise observed at t ~ 10,000 s and sudden increase in leakage current at t ~ 20,000 s is suggestive of "traditional" oxide breakdown. Focusing on the first 3000 s in the area of interest (Fig. 3), the current shows SILC-like (stressed induced leakage current) behavior [7]. The labels A-E in Fig. 3 designate where the test was interrupted to take circuit and device characteristics. Whether or not progressive or SBD is occurring within the area of interest (now referred to as the wearout regime), is difficult to establish. Sudden current increases due to SBD or noise due to progressive BD could be over shadowed by the large direct tunneling current as explained by Pompl *et al.* [8]. This has inspired the development of more complex detection schemes [14], [15] to identify instances of breakdown. Furthermore, upon examining the leakage current shown in Fig. 4, the data show that the pMOSFET oxide undergoes degradation in the wearout regime by 2-3 orders of magnitude increase in gate leakage current for accumulation ($V_G = 1$ V). Note Fig. 4 shows a tighter distribution in the gate leakage for inversion ($V_G = -1$ V). The asymmetry in gate leakage current suggests a more progressive-like behavior as opposed to post-SBD-like behavior (indicated by symmetrical characteristics) as compared by Monsieur *et al.* [14], yet it is not clear. Thus, it is not surprising that the classification of the breakdown mechanisms in ultra-thin gate dielectrics continues to be rigorously investigated [5], [8], [16]-[18]. However, the identification of the degradation or breakdown mechanism is not the objective of this study and will require additional investigation.

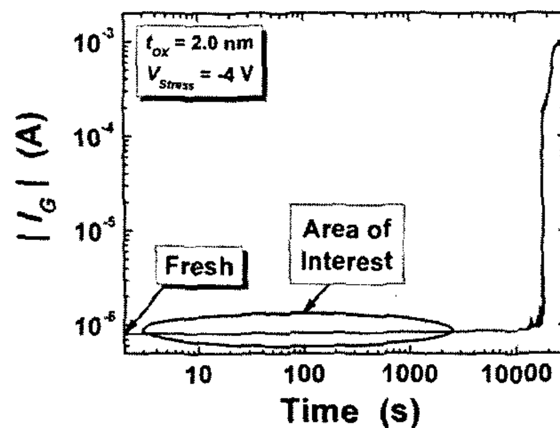

Fig. 2: Typical CVS test for 2.0 nm pMOSFETs showing multiple breakdowns. The area of interest depicts the studied wearout regime.

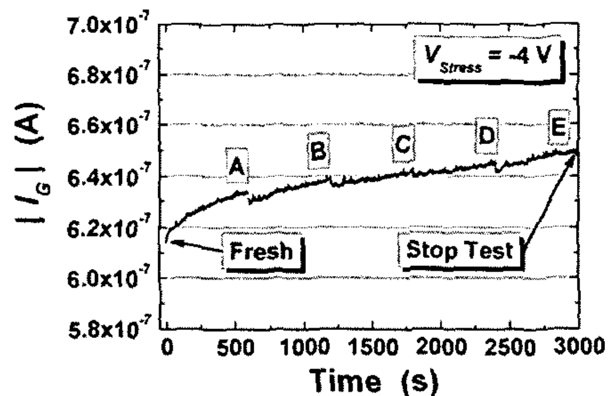

Fig. 3: Typical CVS measurement showing gate leakage current versus stress time in the wearout regime. Intermittent discontinuities [7] in the data, labeled A-E, denote when the stress was interrupted to perform inverter and device measurements.

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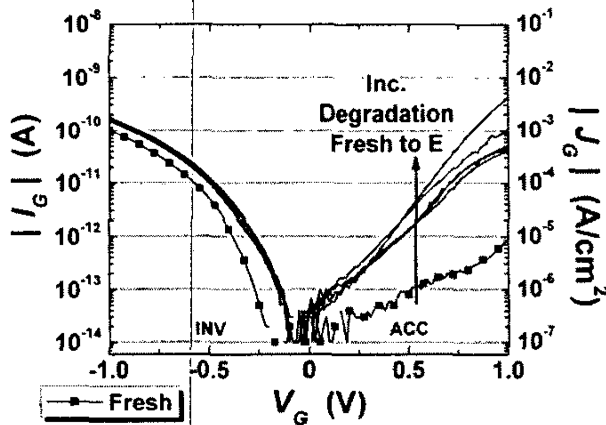

Fig. 4: Gate leakage current showing increased degradation, Fresh to E.

For the inverter VTCs (Fig. 5), an 8 % shift in V_{SP} is typically observed for pMOSFETs having suffered low-level wearout. The V_{SP} approaches zero (left-ward shift), caused by changes in the pMOSFET $V_{TH,P}$ (Fig. 5). Since the pMOSFET is thoroughly isolated from the circuit by the use of SMT during device characterization, a direct correlation between device and circuit degradation is established [9]. This was substantiated through SPICE simulation performed by Stutzke *et al.* to model the relationship of MOSFET threshold voltage on inverter VTC operation, indicating that a V_{SP} shift to the left was characteristic of the pMOSFET $V_{TH,P}$ increasing [19].

As reported by Rodriguez *et al.*, the inverter V_{OH} decreases considerably following various levels of applied negative stress voltage. They attribute the cause of the V_{OH} decrease to the pMOSFET device [6]. However, a change in inverter V_{OH} is not observed in Fig. 5. Additionally, a change in inverter V_{OL} is not observed which is expected since the nMOSFET is Fresh [10]. These combined effects enable the inverter output behavior to transition from 1 V to 0 V, which is consistent with ideal or Fresh circuit components. With the exception of the V_{SP} shift, the degradation in the DC inverter characteristics appears negligible, which may lead to the belief that the wearout regime does not alter circuit behavior.

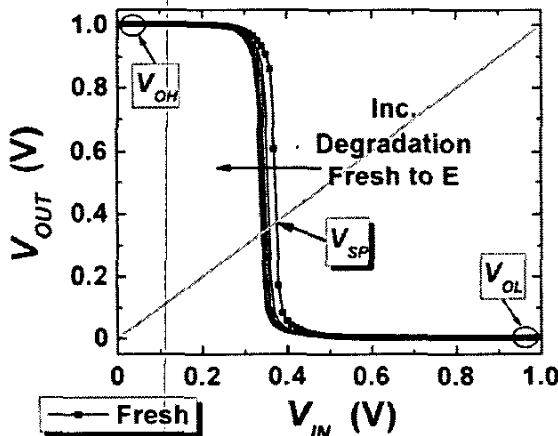

Fig. 5: Inverter voltage transfer characteristics (VTC) showing increasing stages of pMOSFET wearout, Fresh to E.

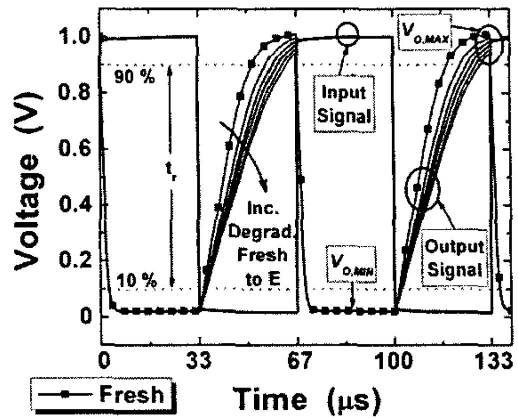

Fig. 6: Time-domain inverter characteristics (VT) showing increasing stages of pMOSFET wearout, Fresh to E.

Alternatively, inverter VT operation (Fig. 6) is influenced much differently as a result of low-level wearout. For this characteristic, degradation Fresh to E shows a change in t_r ranging from 36 % to 62 %. In addition, a change in $V_{O,MAX}$ from 1 V to 0.95 V is observed, compared to a negligible change observed in V_{OH} from the inverter VTC (Fig. 5). Results observed for wearout support the work of Cheek *et al.* in which a more dramatic effect of degradation is observed in the inverter VT response (Fig. 6) as compared to the inverter DC response (Fig. 5) [9]. Note that a change in t_f is not observed, as it is mainly dependent on the nMOSFET response [9].

An important point to understand relative to VT measurements is the signal frequency (Fig. 6). Care must be taken to avoid confusing the input pulse repetition frequency with spectral content. Repetition rates of 15 kHz are used to compensate for the capacitive loading (~ 900 pF) of the measurement setup and subsequently longer delays observed on the output signal of the inverter circuit. However, the delay times scale linearly with capacitive load. This is easily verified experimentally. The relationship is given by [10]:

$$t_r, t_f = 2.2 \cdot R_{ch} \cdot C_l \quad (1)$$

where t_r is the rise time, 2.2 is a constant characteristic of a rise time from 10 % to 90 %, R_{ch} is the MOSFET channel resistance (substitute pMOSFET for t_r and nMOSFET for t_f), and C_l is the capacitive load which includes the output capacitance of both MOSFETs and the load capacitance associated with cabling. While loading effects can be removed from the data to provide VTs with nanosecond time scales, no additional information is gained. The observed effects of the degradation mechanisms in Fig. 6 are still valid and experimentally verified with the test setup.

An additional point of clarification should be noted relative to the time domain measurements. Fig. 6 shows the input signal of the inverter switching from high to low very fast, representative of high speed circuits. An input pulse voltage with fast rise or fall times, as used in this work, contains high-frequency spectral content, in which a step response is a very common wide frequency measurement used in circuits or systems [20]. These high frequencies may be better understood by realizing that the fast rise and fall times of the 15 kHz input signal is constructed using a combination of multiple waves at much higher frequencies as was demonstrated by Jean Baptiste Joseph Fourier [21].

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Further examination of the degradation level E leakage current (Fig. 4) with the corresponding VT performance (Fig. 6) reveals a potential concern. The data indicate that a pMOSFET in the circuit needs only to experience wearout to inhibit high-speed digital performance. Cheek *et al.* observe similar changes in rise time for the inverter time-domain using devices with t_{ox} of 3.2 nm [9]. For this specific case, a current limiting technique [22], [23] was used to study circuit-level oxide degradation based on the likelihood that devices or circuits can exhibit self-limiting behavior, in which the magnitude of the gate or input leakage current is restricted at the time of oxide breakdown. Comparison of experimental data indicates that five orders of magnitude more leakage current was required to produce a similar level of degraded circuit performance in the 3.2 nm devices than these 2.0 nm devices. Consequently, the inverter circuit containing the 2.0 nm devices need only to experience wearout to degrade to the same degree as the inverter circuit containing 3.2 nm devices that have experienced or suffered a traditional breakdown (Fig. 2) [9].

To better understand what device parameters may be responsible for causing such a dramatic decrease in circuit performance, I_{Drive}(@ V_D = 1 V), $V_{TH,P}$, and $G_{M,MAX}$ were examined. A decrease in I_{Drive} by approximately 40 % coupled with an increase in $V_{TH,P}$ in the range of 17 % to 20 % is observed in Fig. 7 and 8, respectively. Additionally, a decrease in $G_{M,MAX}$ by 16 % to 19 % is observed (Fig. 8). These three parameter shifts are related to gate oxide wearout, which provides increased leakage current through the gate oxide, corresponding to less inversion of the channel, and increased channel resistance. These large % shifts in I_{Drive}, $V_{TH,P}$, and $G_{M,MAX}$, are significant changes when compared to the "corner" parameters (i.e., process window) of a typical logic process that can only tolerate process shifts as little as 6 %, 10 %, and 7 % [2], respectively. The implication is, if a circuit or device in a typical CMOS process run experiences wearout, it may deviate considerably from the process window utilized by circuit designers.

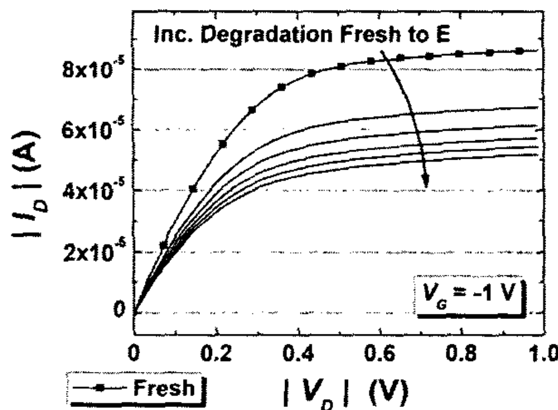

Fig. 7: Typical results showing decreasing drive current with increasing wearout in pMOSFETs.

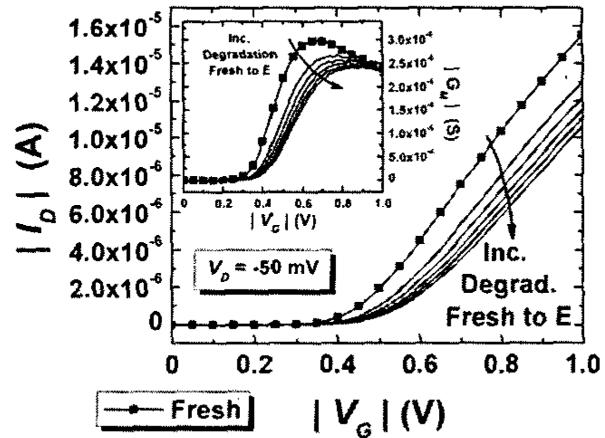

Fig. 8: Typical results showing increasing threshold voltage with increasing wearout in pMOSFETs. The inset depicts the corresponding decrease in transconductance curves.

CONCLUSIONS

It has been shown that the DC inverter circuit performance (VTC) shows minimal change due to pMOSFET devices being stressed in the low-level wearout regime. This may lead to the assumption that wearout does not disrupt circuit behavior. Yet, the time-domain response has decreased considerably. Ultimately, this study suggests that traditional BD need not occur for circuit performance to deteriorate. This low-level device wearout from the 0.1 μm CMOS technology is related to a decrease in device parameters I_{Drive} and $G_{M,MAX}$, with an increase in $V_{TH,P}$, which have been shown to shift beyond the tolerances for a typical logic process. Circuits not designed with these considerations in mind are not guaranteed to perform at intended speeds or accuracy.

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Questions and Answers

Q: Do you have a fresh sample in the Ig-Vg plot on slide 7 of 2 nm data?

A: Two fresh samples are represented by the square and circle symbols in the lowest gate current regime, most visible on the accumulation side of the plot.

Q: How much do you think the change in threshold voltage could be due to NBTI?

A: Since the devices were stressed and tested at room temperature combined with the mass of the wafer and chuck as a heat sink, we predict minimal NBTI effects. Further study is required to accurately determine NBTI effects.

Q: Does this scale with area and obtain a decent Weibull slope? It is believed that this is a soft breakdown rather than SILC. If it scales with area, then it is a pre-softbreakdown event.

A: We have currently tested devices with one area only (W = 10μm, L = 1μm). Further study using devices with different area is required to determine the Weibull slope.

Q: Is this a buried device?

A: No

Q: Did you study the off and on current?

A: The off and on current was studied, showing a decrease in on current by ~ 40% while the off current appeared to fluctuate randomly with respect to fresh characterization.

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