Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach

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Abstract— The effects of noise on gate oxide reliability were examined in nMOSCAPs. Noise is modeled as a voltage spike constructively interfering with a carrier signal. This data correlates to the noise model where device lifetime exponentially decreases with an increase in noise voltage. Noise voltages with the same magnitude as the carrier signal voltage decrease the lifetime by as much as three orders of magnitude. For noise that is one-fifth of the magnitude of the carrier signal voltage, an order of magnitude is observed. As interconnect spacing decreases, the probability of noise and capacitive coupling increases; therefore, the effect of noise on the lifetime of MOS devices may be of great concern.

I. Introduction

The primary reliability stress test method for determining degradation mechanisms and lifetime of gate dielectrics is the constant voltage stress (CVS) test [1], [2]. CVS tests do not necessarily represent stress in IC devices because ICs are operated in either digital or analog mode. An alternative method to more accurately replicate digital and analog device operation is the pulse voltage stress (PVS) test. But our initial research and work done by others on ultra-thin gate oxides, indicates that PVS testing requires equivalent or even longer testing times than CVS testing [3]-[5].

However, PVS tests in which anomalous waveforms were used to stress the gate oxide produced a device lifetime significantly less than CVS. This result led to Multiple Waveform Pulse Voltage Stress (MWPVS) testing. MWPVS experiments are a PVS technique whereby multiple waveforms are combined to replicate a carrier signal with noise interference. These tests resulted in a significant reduction of device lifetime, as compared to both CVS and single waveform PVS. It is quite possible that noise signals can constructively interfere with a carrier signal in digital and analog devices. The fundamental result of the MWPVS test is that constructive interference occurs, due to the superposition principle of waves. Thus, during short time intervals, the voltage amplitude of the carrier signal is increased. In this paper, we examine the effects of noise on device lifetime in which the noise is modeled as a spiking voltage on the carrier signal. We extend our results to cases in which noise can be a reliability issue.

II. Experimental Procedure

A. Devices

The devices are nMOSCAPs with an oxide thickness of 3.2 nm and an area of 2.1×10^{-4} cm^2, which were tested at room temperature. The devices were fabricated in a 0.16-µm/1.8-V CMOS technology with n^+ poly/silicon gate. Stressing was performed in accumulation mode because dielectric breakdown occurs at lower voltages than in inversion mode [6], [7]. Pre- and post-MWPVS gate current-gate voltage (Ig-Vg) measurements were performed to examine the type and amount of degradation that resulted during testing. MWPVS measurements were terminated when the gate leakage current reached a value greater than 1 mA at –2 V, signifying current Limited Hard Breakdown (LHBD) [6].

B. Test configuration

The equipment used in MWPVS experiments include an Agilent 4156C Precision Semiconductor Parameter Analyzer (SPA), two HP 33120A Arbitrary Waveform Generators (WFGs) selected for the phase lock option, a HP 53131A Universal Counter, an HP Infinium Oscilloscope, and a breadboard switch. The nMOSCAPs were tested at wafer lever using a probe station equipped with Cascade Microtech *DCM* micro-positioners enclosed in a Faraday cage. The configuration used for MWPVS is shown in Fig. 1. The WFGs, connected in parallel, were used to output the multiple waveforms. A switch was placed between the WFGs and the device under stress (DUT) to safeguard against over-stressing. The counter was utilized to determine the number of pulses-to-breakdown (P_{bd}). The oscilloscope was used to monitor phase information and to verify the voltage versus time output of the carrier and noise signals before and after pulsing.

Fig. 2 shows the flow chart for the experimental procedures. Initial Ig-Vg measurements were taken on the fresh nMOSCAPs with Vg swept from 0 V to –2 V. This sense voltage was used to avoid stressing the gate oxide. The initial leakage current Ig measured at –2 V for a fresh gate oxide is approximately 1 to 2 pA and a corresponding current density (J_g) of approximately 7 nA/cm^2.

A unipolar carrier signal was used with a frequency, voltage amplitude and duty cycle of 5 kHz, -5 V and 75 %, respectively. For each test set, at least six MOSCAP devices were subjected to a 5 kHz noise signal superimposed on the carrier signal. Each test set is a measurement sequence in which a specific noise signal voltage amplitude and duty cycle is used. The range of duty cycles and voltage amplitudes used in the test sets are shown in Table 1. For the noise model, all test were compared to a baseline test defined as a carrier signal having a voltage amplitude of –5 V and a noise amplitude of 0 V. The results were further compared to CVS at –5 V.

The carrier plus noise stress signals were configured and verified by the oscilloscope. The resulting waveform or pulse stress signal was input to the gate of the device. A set number of pulses reaching the gate was controlled by closing a switch (refer to Fig. 1) for a designated amount of time. A counter was used to output the number of pulses during each stress cycle. These numbers were recorded and used to calculate the time-to-breakdown (t_{bd}). Following each set of pulses, an Ig-Vg sense measurement was performed. This process was repeated until the gate leakage current was greater than 1 mA at –2 V, which signified that current LHBD had occurred [6].

The t_{bd} is proportional to the P_{bd} and is given by:

$$t_{bd} = T \cdot DC \cdot P_{bd} \tag{1}$$

in which the proportionality constant is the product of the period (T), and DC (i.e., product gives the pulse width) of the carrier signal (see Fig. 3).

For initial t_{bd} calculations, a DC of 75 % was used for both the carrier and noise signals. This is a first order approximation and provides the worst-case scenario since the DC of the noise signal was either 25 % or 5 %. An effort is in progress to refine the calculation of t_{bd}.

III. Experimental Results

Pre- and post-MWPVS Ig-Vg sense measurements, shown in Fig. 4, indicate that Stress Induced Leakage Current (SILC) [8] was observed. With increased pulsing, current LHBD was eventually achieved which defined the P_{bd}. The Ig-Vg measurements show that Ig converged around –1 V. Fig. 5 shows the Weibull distribution of failures versus t_{bd} for CVS, single PVS (0 V noise signal), and MWPVS, where a reduction in t_{bd} is observed as the noise spike voltage is increased. This was also observed for higher voltage noise spikes in which device lifetime was approximately the same with noise spikes for DCs of 5 % and 25 %. A reduction in device lifetime is slightly less for the spike voltage of –1 V and a DC of 5 %. It should be noted that the Weibull distribution was not normalized to typical device areas [9].

IV. Discussion and Conclusions

MWPVS results were compared to CVS and single waveform PVS stress tests, at the same applied voltage stress. The t_{bd} from MWPVS are less than t_{bd} for CVS and single PVS in all cases. The MWPVS sense data (Fig. 4) suggests that the change in leakage current, in the range of 0 V to –0.8 V, increases with the presence of noise, due to the increase in stress voltage.

The noise model supports initial MWPVS data indicating that increasing the noise (or spike voltage) exponentially decreases device lifetime as shown in Fig. 6 & 7. The noise model for spike voltages with a DC of 5 % and 25 % are presented in Fig. 6 and 7, respectively. In Fig. 6, it is shown that the data for the noise spike with a DC of 5 % follows the noise model nearly as well as the data with a noise spike having a DC of 25 %. Fig. 7 demonstrates that the data was consistent with the model for a duty cycle of 25 %.

The noise model is based on:

$$\frac{1}{t_{bd,1}} \approx d \cdot e^{c|V|} \tag{2}$$

for PVS, and

$$\frac{1}{t_{bd,2}} \approx d \cdot e^{c|V|} + d' \cdot e^{c(|V|+|dV|)} \tag{3}$$

for MWPVS. The d is a constant proportional to DC of carrier signal, d' is a constant proportional to DC of noise signal, and c is a voltage acceleration factor. The noise amplitude is given by dV. The fractional t_{bd} change, ($t_{bd,1}$ - $t_{bd,2}$) / $t_{bd,2}$, is proportional to:

$$\frac{t_{bd,1} - t_{bd,2}}{t_{bd,2}} \approx e^{-c \cdot dV}, \quad for \quad dV < 1. \tag{4}$$

The significance of (4) is the exponential decrease in device lifetime with increase in noise amplitude.

For high noise signal voltages, -3 V and -5 V, little difference was observed in device lifetime between the 5 % and 25 % DCs. This is significant because it suggests that if a noise spike occurs at these voltages, regardless if the DC is short or long, it may have the same effect on device lifetime. For a noise signal with a magnitude of –1 V, a noise signal with a DC of 25 % shows a shorter lifetime than for a noise signal with a DC of 5 %.

There are several cases in which noise can occur and become a reliability concern in ICs. One potential noise candidate in state-of-the-art ICs is interconnect capacitive coupling [10]. Fig. 8 displays a Precharge-Evaluate dynamic gate with capacitive coupling. During normal circuit operation, a typical input to the gate of the fourth MOSFET (M4) would appear as a varying signal with $V_{DD} \leq$ -5 V. Signal interference from an adjacent interconnect can be coupled at this node leading to an increase in the signal voltage due to constructive interference. Furthermore, when M1 and M2 are off, the output node is pre-charged to V_{DD} and is a high impedance (Z) node. In dynamic gates, the high-Z nodes can appear

capacitive. If coupling exists between this node and a varying signal (e.g., clock pulse), this can lead to capacitive coupling. The magnitude of the carrier signal increases as the capacitive coupling (in the form of noise voltage) increases indicating that as circuit densities continue to increase, noise induced by capacitive coupling becomes an even greater reliability issue.

Baker et al. [11] give an example of another potential area for voltage noise spikes to occur. They discuss the case of an IC chip in which both digital and analog circuits coexist. Noise from the digital system can be introduced into the analog system through the power supply and ground connections. Because of switching, digital circuits can have large amounts of transient current if there is a small amount of resistance in an interconnect. This can result in a voltage spike. In these circuits, a voltage spike can also be produced due to the inductance of the bonding wire.

This report demonstrates the relevance of MWPVS testing in which the voltage amplitude of the carrier signal is combined with a spike voltage and modeled as noise. The data and the model strongly suggest an exponential decrease in device lifetime. Several cases in ICs are given in which noise can be a reliability concern.

Future work in this area includes refining the t_{bd} calculation and further testing. Currently, tests at 20 kHz and 100 kHz are being performed. Measurements will also be performed that represent carrier and noise signals at mixed frequencies in the kHz and MHz regimes.

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Table 1
NOISE SIGNAL PARAMETERS

Duty Cycle	5 %				25 %			
Voltage Amplitude (V)	0	-1	-3	-5	0	-1	-3	-5

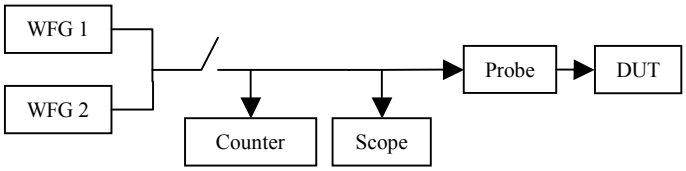

Fig. 1. Configuration for MWPVS experiments.

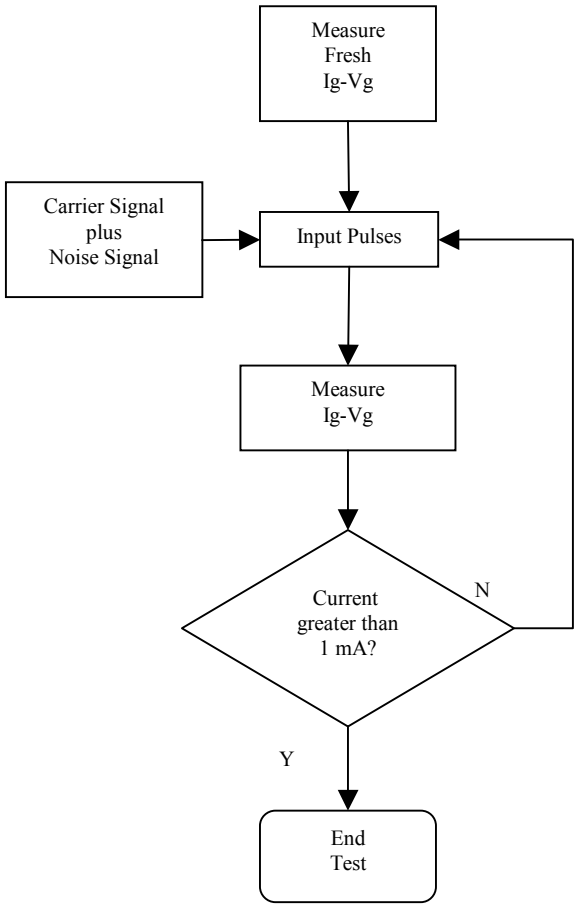

Fig. 2. Flow Chart of experimental procedure.

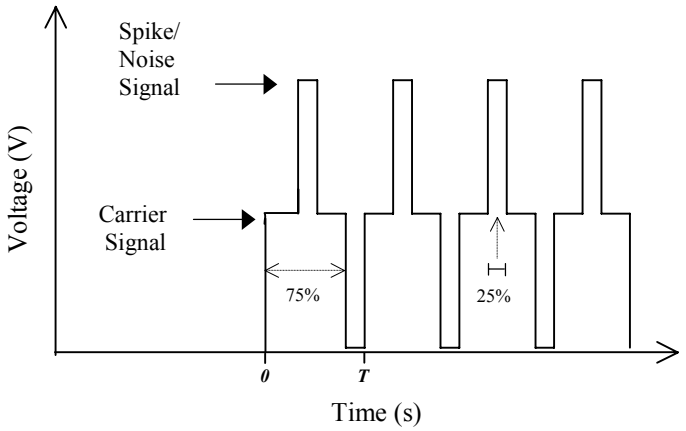

Fig. 3. The input signal to the MOS device during MWPVS experiment. The waveform parameters *T* and *DC* used to calculate t_{bd} for MWPVS are shown.

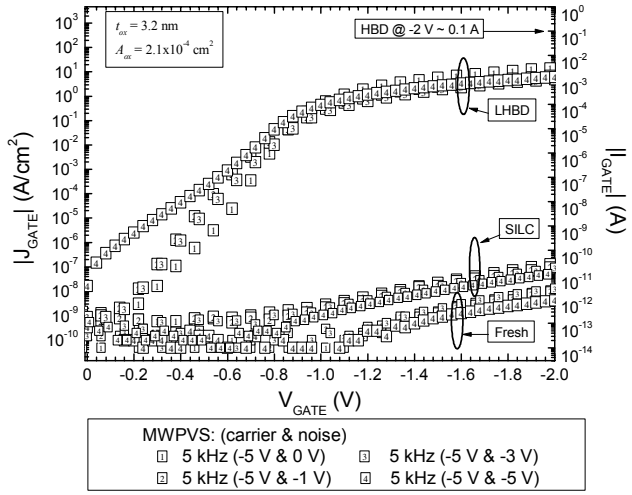

Fig. 4. Pre- and Post-MWPVS *Ig-Vg* data indicating SILC and current LHBD. HBD at –2 V is indicated by the 0.1 mA current compliance.

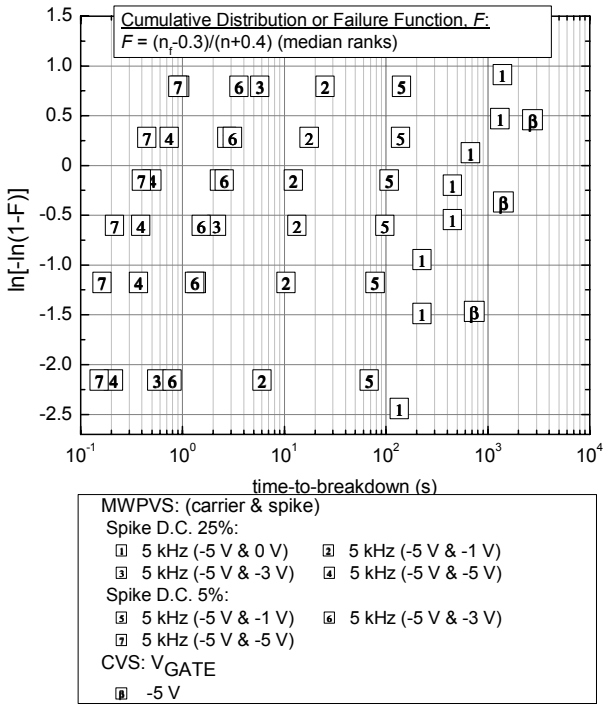

Fig. 5. Weibull plot showing the t_{bd} results from the MWPVS experiments using nMOSCAPs.

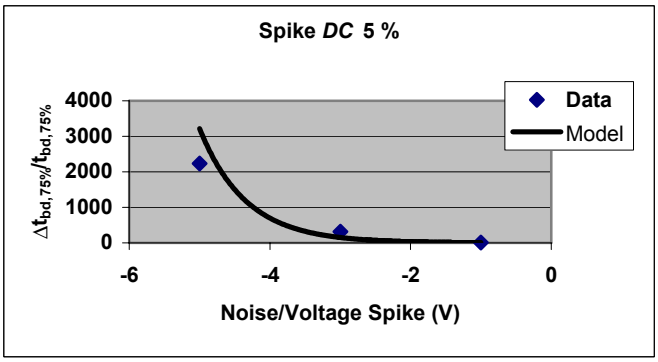

Fig. 6. Noise model for MWPVS for a spike voltage with a *DC* of 5%.

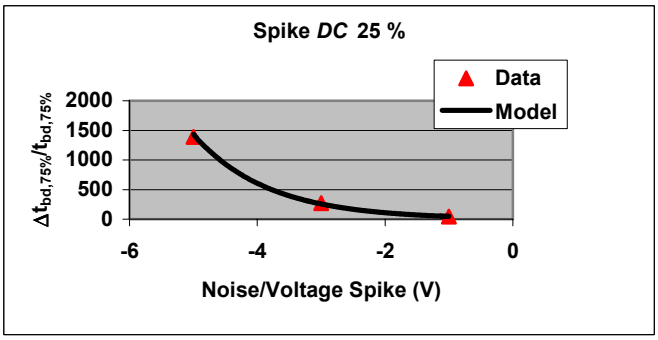

Fig. 7. Noise model for MWPVS for a spike voltage with a *DC* of 25%

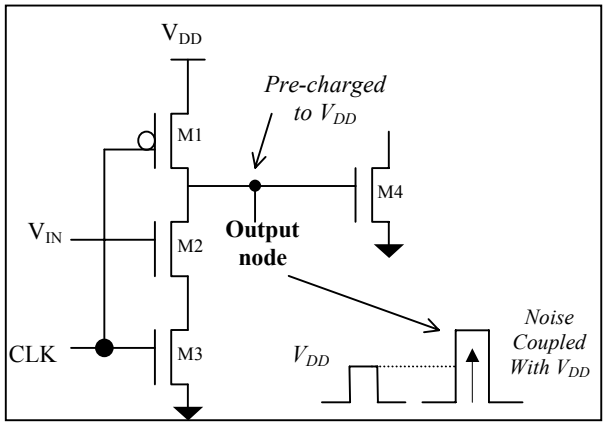

Fig. 8. Dynamic gate illustrating that a noise signal coupled with an output node may result in increased output voltage. The label M designates MOSFET.