Mixed-Signal Design in the Microelectronics Curriculum

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Abstract - This paper discusses educating electrical engineering students so they can do mixed-signal design (MSD). It also discusses why MSD is important and how it fits into a contemporary electrical engineering curriculum. The paper concludes with a practical example of MSD (the design of a memory sensing circuit) that shows the benefits over traditional analog techniques.

I. Introduction

What is mixed-signal design (MSD)? We might think of it as a design where both analog and digital circuits are present on the same chip. However, this definition of MSD would be incorrect in general. A chip containing both an inverter (a digital circuit) and an op-amp (an analog circuit) isn't a MSD. MSDs are the result of partnering analog circuit design with digital signal processing (DSP). In the general sense only circuit designs that integrate analog circuits with DSP should be considered MSDs.

After some thought we should see that integrating MSD into the electrical engineering curriculum will become challenging because of the prerequisites of knowing both DSP and analog circuit design.

II. Moving MSD into the Curriculum

The basic sequence of courses an undergraduate electrical engineering student takes to concentrate in circuit design follows the general path of: 1) basic microelectronics, 2) digital/vlsi integrated circuit design, and 3) analog integrated circuit design. By the time the student has finished this circuit sequence they are usually graduated and their technical elective choices are exhausted. Further, if we add the second requirement that the undergraduate student also take course work in DSP to meet the prerequisites of a MSD course we end up with unrealistic expectations. The obvious solution to getting MSD knowledge is for the student to stay in school and work on a graduate degree. However, after the 5 years (typical) it takes the student to earn the BSEE few have the desire to remain in school for any additional time. To summarize the problem MSD is a needed skill for graduating undergraduate students but it's difficult to fit an MSD course into the BSEE curriculum.

The approach we've taken at Boise State is to teach the relevant DSP topics in the mixed-signal design course in a "just-in-time" format. Traditional DSP techniques can differ considerably from the techniques used in MSD. For example, a traditional digital filter may use a transversal tapped delay line with the multiply and sum type approach. Custom filters, in general MSD, utilize digital differentiators and integrators to implement filters. The techniques used are different than those taught in the typical DSP course. In MSD integer numbers are most often used, layout area is a big concern since the MSD may be a small portion of the overall chip, speed and power can be adjusted more easily than in general purpose digital signal processors, etc. The MSD course at Boise State is offered in the spring as a graduate course. It can, however, be taken by the graduating undergraduates with permission from the instructor.

III. Course Topics

The topics the student should learn in a MSD course can be listed as: data converter design and operation, custom digital filtering, delta-sigma modulation, and system considerations (aliasing, frequency response, signal-to-noise ratio, distortion, etc.) For a course in MSD a textbook has been written by the author [1] with the goals of educating students and providing a practical reference for working engineers. In this section we briefly cover two concepts in MSD that will be useful when presenting the example in the next section.

Delta-Sigma Modulation

A delta-sigma modulator (DSM) is a circuit that outputs the average, over time, of its input. For analog-to-digital conversion this means that the DSM's digital output is the average of its analog input, see Fig. 1. The DSM illustrates a key benefit of MSD and why MSD is becoming more important as CMOS technologies continue to shrink namely the ability to trade time off for accuracy. Low quality analog components can be used.

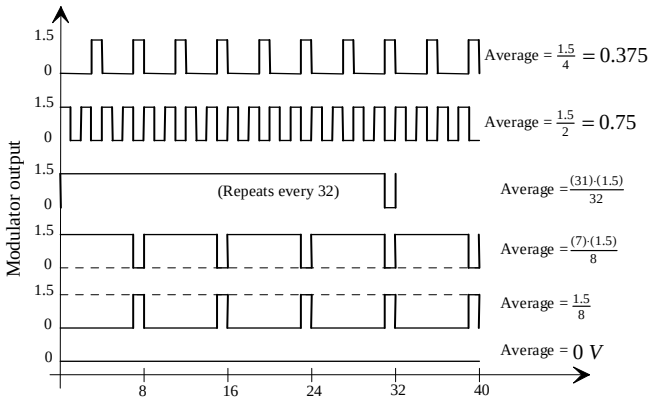

Figure 1 DSM outputs and their averages.

Digital Filtering

The simplest digital filter is one that takes the average of K input samples. Figure 2 shows the basic filtering topology when the filter is used with a DSM. The input signal is $x[nT_s]$ while the output signal is $y[nT_s]$. We can write the relationship between the input and the output as

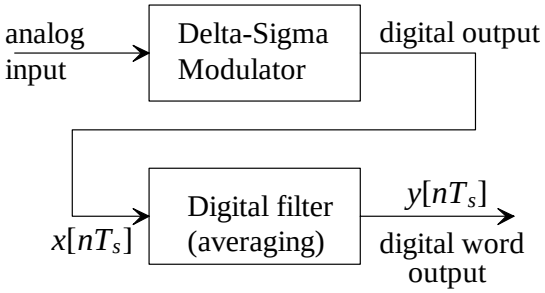

Figure 2 Digital filter used for averaging.

$$y[nT_s] = x[(n-K+1)T_s] + x[(n-K+2)nT_s] ...$$

$$... + x[(n-K+(K-1)T_s] + x[nT_s] \quad (1)$$

taking the z-transform of this equation results in

$$Y(z) = X(z) \cdot (z^{1-K} + ... + z^{-2} + z^{-1} + 1) \quad (2)$$

If we multiply the top and bottom of this equation by $(1-z^{-1})$ we can write the transfer function of the digital averaging filter as

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1-z^{-K}}{1-z^{-1}} \quad (3)$$

knowing

$$z = e^{-j2\pi\frac{f}{f_s}} = \cos 2\pi\frac{f}{f_s} + j \cdot \sin 2\pi\frac{f}{f_s} \quad (4)$$

we can write the frequency response of the digital averaging filter as

$$H(f) = \frac{\text{sinc } K\pi\frac{f}{f_s}}{\text{sinc } \pi\frac{f}{f_s}} \quad (5)$$

The magnitude response of the averaging filter is seen in Fig. 3. Note that averaging can be thought of as simply a lowpass filter. The longer we average (the larger number of K inputs we average) the narrower the bandwidth of the filter. By increasing K the signal-to-noise ratio increases (the digital filter removes noise). While space doesn't allow as to go into this important concern here we point the interested reader to [1] for considerably more background information.

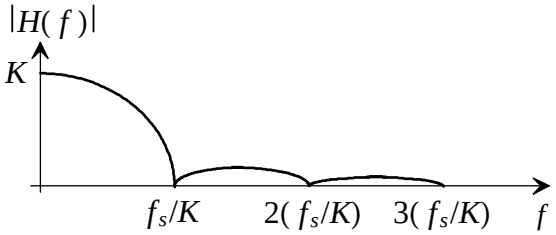

Figure 3 Frequency response of an averaging filter.

IV. An Example

To provide an example of mixed-signal design let's consider sensing for an array of resistive elements found in a magnetic RAM, MRAM, [2] and seen in Fig. 4. The equivalent circuit for the MRAM array is seen in Fig. 5. We are interested in determining the voltage on the bitline. If the number of wordlines (rows) N is large then the sneak resistance $R/(N-1)$ will be small. If we are trying to sense changes in the resistor R_{cell} the smaller this sneak resistance the larger challenge sensing presents.

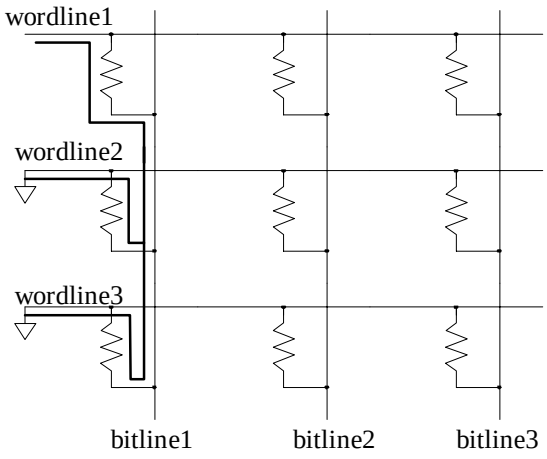

Figure 4 Array of resistive memory cells.

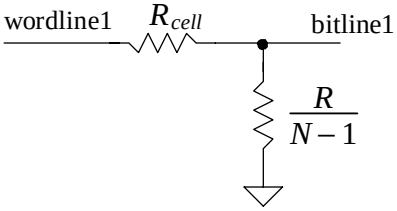

Figure 5 Equivalent circuit for Fig. 4.

Traditional Analog Design

Figure 6 shows the traditional method for sensing. If the op-amp is ideal it holds the bitline at ground potential. This forces the current through the sneak resistance to zero. The current through the memory cell we are trying to sense becomes V_{row}/R_{cell}. If we precharge the capacitor prior to sensing we can use the current through the memory cell to discharge the capacitor. A comparator and counter can be used to determine how long it takes the capacitor to discharge. Longer discharge times indicate a large R_{cell}.

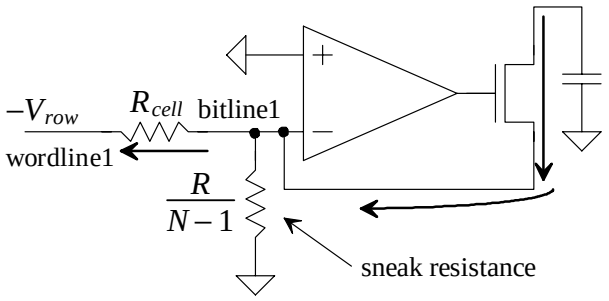

Figure 6 Sensing using traditional techniques.

At first glance this seems like a straightforward method that will result in robust sensing. However, let's look at how imperfections in the op-amp can affect sensing. What happens if the op-amp has an offset or finite gain? The answer is that the inverting op-amp input will not be held at precisely 0 V. If the cell resistance is 1 MΩ or 800k and V_{row} is 1 V then the current we are sensing is $1.25\ \mu A - 1\ \mu A$ or 250 nA. If the array has 1024 rows (= N) then the current through the sneak resistance is $(N-1)V_{os}/R$. If we use 1 MΩ for R and the offset is 1 mV then this sneak current is 1.023 μA or four times as much as our signal current! If the offset isn't constant or the bitline voltage varies because of the finite gain sensing will be impossible. The noise of the op-amp will make the sense operation even more challenging. The flicker noise of the op-amp, because it is integrated, will make attaining large SNRs impossible.

Mixed-Signal Design

Let's consider, for the sensing problem, using a Delta-Sigma modulator of the form seen in Fig. 7. In this figure the bitline voltage is applied to an operational transconductance amplifier (OTA). The OTA changes the voltage on its' input to an output current. This current is integrated by the capacitors. The comparator is clocked at some rate, say 100 MHz (fast enough so the capacitors don't fully charge), that controls the connection of the current sources/sinks. The feedback action will attempt to force the voltages on the capacitors to the same values. Because the output currents from the OTA will not be exactly the same (in the ideal case one will charge and the other will discharge the capacitors) the current sink will be in one position more often than the other. If we take the output of the comparator and feed it to a counter as its clock signal then we get final counter outputs, after averaging *K* inputs, that change with the bitline voltage. These counter codes then represent different cell resistances. The counter does the digital filtering we saw in Fig. 3.

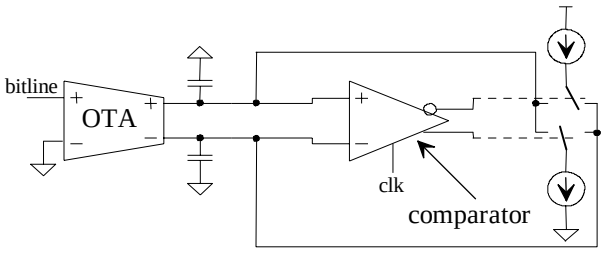

Figure 7 A Delta-Sigma Modulator for sensing.

The DSM of Fig. 7 is a robust circuit. If the comparator makes a wrong decision which causes the current sources/sinks to be connected to the capacitors incorrectly for a clock cycle it doesn't really matter. Because we are averaging the error will get corrected in subsequent comparator decisions. If the OTA gain isn't too high that really doesn't matter either. Its performance is correlated from sample to the next.

Experimental results

Both sensing circuits were fabricated and experimental data was taken. The traditional sensing scheme seen in Fig. 6 had issues with regard to the relationship of the resistors (and thus the currents) and the size of the on-chip capacitor. With process variations the capacitor can discharge too slowly or quickly affecting the time of the sensing operation. This makes, without considering anything else, high SNRs over process, temperature, and voltage changes practically impossible. Because the DSM sensor can run indefinitely this wasn't an issue. Figure 8 shows the outputs of the DSM with different applied voltages and a 1000:1 divider between R_{cell} and the sneak resistance (word line voltages were 400 mV, 200 mV, and ground). The word line voltage was supplied through a wire to the chip and so no special low noise techniques were used to enhance the data. The number of points averaged, *K*, was 1000. Clearly, in this case, MSD has resulted in solving a challenging problem.

V. References

[1] Baker, R.J. "CMOS: Mixed-Signal Circuit Design," *John Wiley and Sons Publishers*, 2002. ISBN 0-471-22754-4

[2] Baker, R.J. "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Meeting*, Boise, ID Oct. 25, 2002.

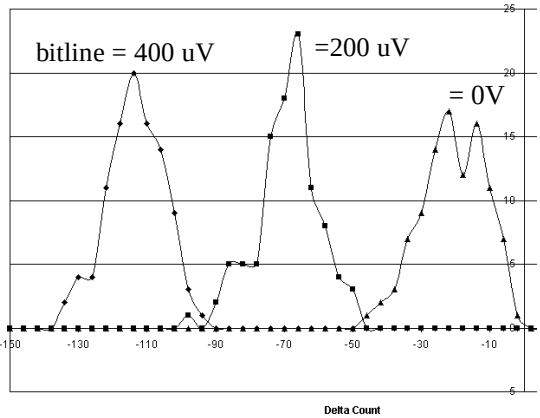

Figure 8 Experimental results using DSM sensing.