Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics

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Abstract

The effects of circuit-level stress on both inverter operation and MOSFET characteristics have been investigated. Individual MOSFETs, with gate oxide thicknesses of 3.2 nm and active dimensions of 25 µm x 25 µm, are connected in an inverter configuration off-wafer via a low-leakage switch matrix. Inverters are stressed with a ramped voltage stress (RVS) of various magnitudes to induce different degrees of gate oxide degradation. In addition, voltage transfer curves (VTCs) of degraded inverters are simulated using a new circuit model. At the transistor level, both the PMOSFET and NMOSFET show increased gate leakage current up to eight orders of magnitude, severely reduced on-currents and transconductances (g_m), and large threshold voltage (V_t) shifts of 100 mV or more. Different trends in inverter performance are observed following positive and negative stress. However, regardless of the stress polarity, circuit-level stress results in inverter performance degradation, such as reduced output swing, switching point shifts, and increased rise/fall times. After the largest positive RVS, the output voltage swing has decreased from 1.8 V fresh, to 1.54 V post-stress. Much larger changes in the inverter voltage (V-t) time domain performance are observed. The minimum output low voltage is similar to that of the VTC, but the rise time increased significantly enough that the output voltage is only pulled up to 660 mV (V_{DD} = 1.8 V) before it switches low. In terms of circuit reliability, it may be possible for subsequent circuit stages to compensate for a few degraded devices, but increased rise/fall and delay times may cause timing issues in high-speed circuits. Furthermore, increased gate or off-state leakage currents can potentially load previous circuit stages or result in increased power consumption.

Introduction

Gate oxide breakdown and reliability has become an important issue because it might be a limiting factor in the future scaling of high performance CMOS integrated circuits [1, 2]. Extensive studies have been conducted on gate dielectric breakdown of individual MOS capacitors and MOSFETs (for an overview, see [3]). However, there have been few investigations of the effects of circuit-level stress on circuit performance and reliability [4-8]. Many of those studies have focused on large integrated circuits with many transistors. In complex circuits, such as digital and RF, it has been demonstrated that hard breakdown (HBD) in multiple MOSFETS does not cause total circuit failure, but these circuits remain functional [7, 9]. And although it has been reported that subsequent circuit stages may be capable of compensating for a few degraded devices [7], increased rise/fall and delay times may result in potential timing issues in high-speed circuits. Furthermore, in complex integrated circuits, it is only possible to examine the effects of stress on the circuit as a whole. In order to better understand potential circuit reliability issues, it is beneficial to be able to observe the effects of stress on the individual

MOSFETs within the circuit. In this study, this is accomplished by stressing simple integrated circuit building blocks (SICBBs) such as transmission gates, current mirrors, and inverters, which are the focus of this study. Therefore, using simple circuits as a foundation for understanding large-scale circuits alleviates the added complexity during stressing and/or characterization at both the device and circuit levels.

Circuit-level Stress Technique

PMOSFET and NMOSFET transistors fabricated in a 0.16-µm/1.8-V CMOS technology, both with gate oxide thickness of 3.2 nm and gate dimensions of 25µm x 25µm, are connected in an inverter configuration off-wafer via an Agilent E5250A low leakage switch matrix (Fig. 1). Stress and characterization tests are performed with an Agilent 4156C Precision Semiconductor Parameter Analyzer, an Agilent 41501B pulse generator, an Agilent Infinium oscilloscope, and a probe station equipped with eight Cascade Microtech DCM positioners enclosed in a Faraday cage. The flow chart in Fig. 2 outlines the following procedures used during circuit-level stress experiments.

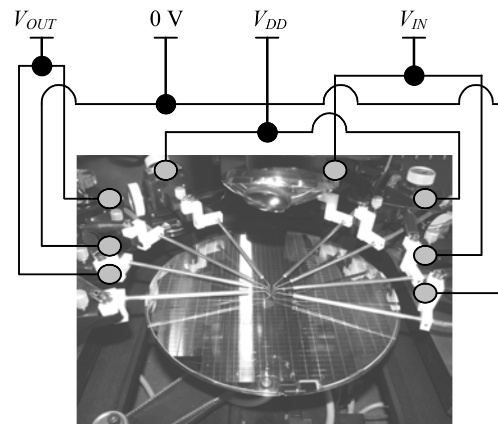


Fig. 1. Wafer-level configuration for circuit-level stress experiments showing the eight connections made off-wafer.

The inverter circuits are investigated under both positive and negative stress conditions. A ramped voltage stress (RVS) is applied from input to output with the V_{DD} and *GND* terminals floating [10], as shown in Fig. 3. The maximum value of the ramped voltage is varied to induce multiple degrees of gate oxide degradation, which

ranged from 0 to +/- 8 V, 0 to +/- 10 V, 0 to +/- 12 V, and 0 to +/- 14 V. A series of pre- and post-stress tests are conducted on the inverter toexamineperformancechangesintheVTCsandV-t

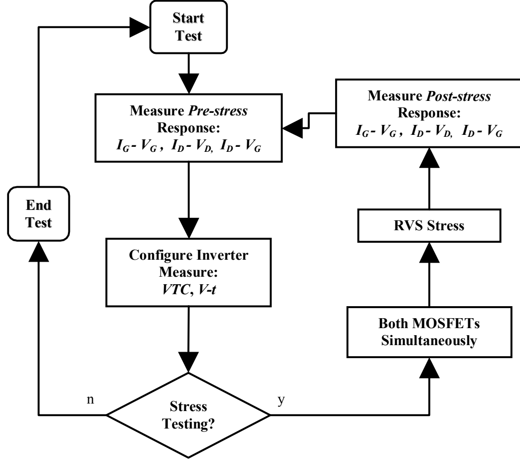


Fig. 2. Flow chart for circuit-level stress experiments.

domain characteristics. For inverter performance measurements, the input voltage (V_{IN}), power supply voltage (V_{DD}), test frequency, and duty cycle, were 1.8 V, 2.5 kHz, and 50 percent, respectively. In addition, all inverter leakage currents are monitored by connecting V_{OUT}, V_{DD}, and *GND* nodes to 0 V.

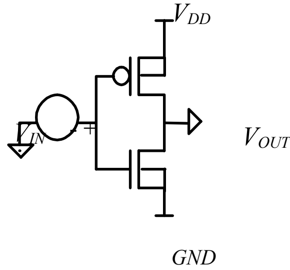


Fig. 3. Inverter circuit schematic used for circuit-level stress testing. The voltage source indicates that stress was induced from the input to the output.

The type and amount of degradation observed for each MOSFET, as a result of circuit-level stress, are identified by comparing pre- and post-stress gate leakage current versus gate voltage (I_G-V_G) measurements. I_G-V_G measurements are taken with the drain (*D*), source (*S*), and bulk (*B*) terminals at ground potential. The DC parameters selected for examining the effects of degradation on individual MOSFET characteristics before and after circuit-level stress are maximum drain current ($I_{D,MAX}$), on-current (I_{On}), off-current (I_{Off}), subthreshold slope (*S*), transconductance (g_m), and threshold voltage (V_t). The absolute value of the data is plotted where appropriate. The PMOSFET and NMOSFET operating modes for positive/negative stress are accumulation/inversion and inversion/accumulation, respectively.

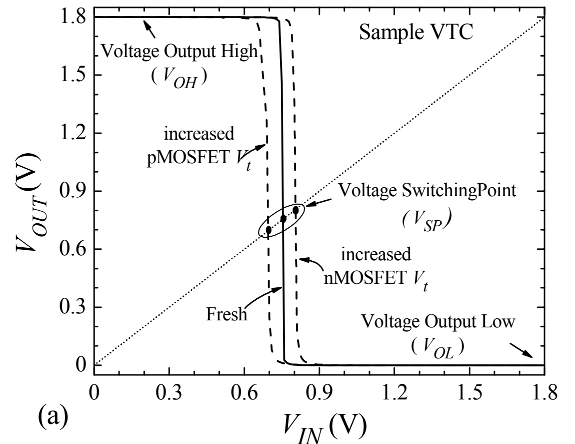
Circuit Overview

An introduction to the fundamental operation of the CMOS inverter circuit is provided and parameters relevant to this study are defined. Assuming ideal conditions, the inverter voltage transfer characteristic (VTC) parameters [Fig. 4(a)] and circuit operation can be described by the following two cases [11]. First, when the inverter input voltage (V_{IN}) is low (0 V) the PMOSFET is operating in inversion mode or is turned "on", while the NMOSFET is operating in accumulation mode or is turned "off". In this case, the PMOSFET device will pull-up the output node (V_{OUT}) to V_{DD} (1.8 V), therefore the PMOSFET is defined as the "pull-up" device. As a result, the noise margin parameter voltage output high (V_{OH}) is 1.8 V, which indicates logic "1". Generally, noise margin is defined by how well the circuit behaves in the presence of noise [11]. The second case is when V_{IN} is high (1.8 V) the PMOSFET is operating in accumulation mode or is turned "off", while the NMOSFET device is operating in inversion mode or is turned "on". In this case, the NMOSFET pulls V_{OUT} down to the lowest operating voltage (0 V), thus the NMOSFET is referred to as the "pull-down" device. Subsequently, the noise margin parameter voltage output low (V_{OL}) is 0 V which corresponds to logic "0". The total voltage output swing of the inverter is then defined as $V_{OH} + V_{OL}$.

In the middle portion of the VTC, ideally at $V_{DD}/2$, is the switching point voltage (V_{SP}), defined when $V_{IN} = V_{OUT}$. For a short time, both devices are "on" enabling current to flow through the inverter. The equation used to calculate inverter V_{SP} is given by:

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{tn} + (V_{DD} - V_{tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{1}$$

where β_n (β_p) and V_{tn} (V_{tp}) are the NMOSFET (PMOSFET) transconductance and threshold voltage parameters [11].



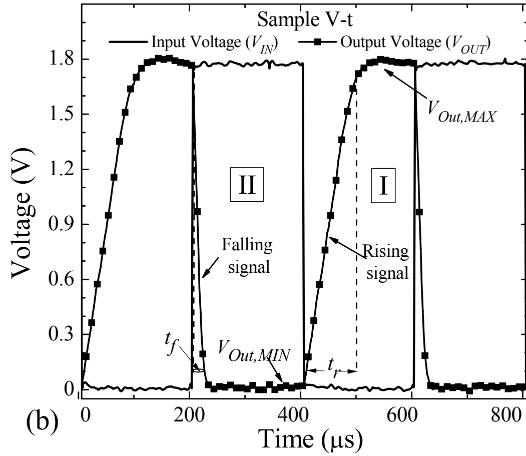


Fig. 4. (a) Simulated voltage transfer characteristics (VTCs) used to define inverter parameters and show the relationship of MOSFET V_t on inverter behavior. (b) Inverter V-t parameters.

In addition to inverter definitions, Fig. 4(a) shows the influence of MOSFET threshold voltage (V_t) on inverter VTCs. The Spice simulations performed for this study indicate that increased V_t of the PMOSFET (V_{tp}) results in the V_{SP} shifting left, while increased V_t of the NMOSFET (V_{tn}) shifts the V_{SP} right.

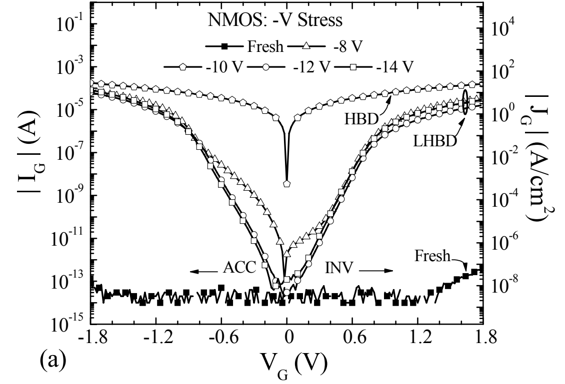
The digital response of the inverter is characterized using the voltage-time (V-t) domain response. Similar to the VTC operation, the inverter V-t domain [Fig. 4(b)] describes two areas of interest, which are designated as region I and II. Region I is defined as the rising signal or PMOSFET pull-up portion. At the maximum output voltage ($V_{Out,MAX}$), this region coincides with V_{OH}. Region II corresponds with the falling signal or NMOSFET pull-down portion. At the minimum output voltage ($V_{Out,MIN}$), this region is equivalent to V_{OL}. For this case, the total voltage output swing of the inverter is defined as $V_{Out,MAX} + V_{Out,MIN}$.

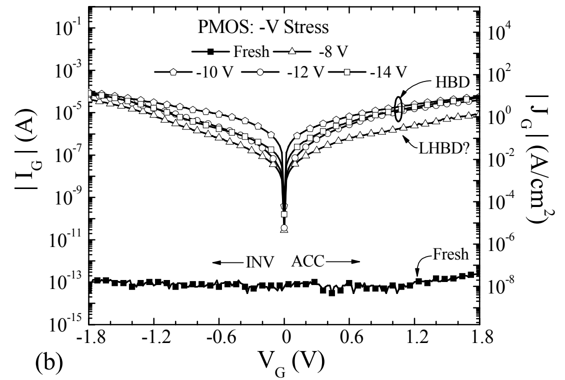
In addition, the rise-time (t_r) and fall-time (t_f) can be determined from Fig. 4(b). The t_r and t_f parameters are the times required for the output voltage to change from 10 % to 90 % of $V_{Out,MAX}$ and from 90 % to 10 % of $V_{Out,MAX}$, respectively [12]. In this study, t_r and t_f are initially larger than expected because of the long transistor channel lengths and extensive cabling used to make connections to the switch matrix.

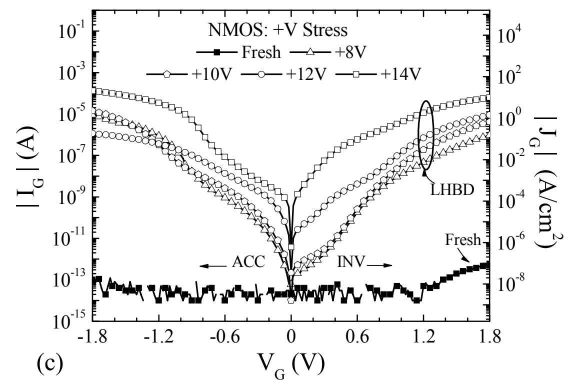
Results

MOSFET Characteristics

Fig. 5 shows gate leakage currents for the NMOSFET [(a)/(c)] and PMOSFET [(b)/(d)] following negative/positive stress. In general, as stress magnitude increases, gate leakage current of both the NMOSFET and PMOSFET increases, as would be expected. Maximum leakage current is typically highest at V_{Gate} = -1.8 V, regardless of the original stress polarity. The NMOSFET typically suffers limited hard breakdown (LHBD) [19, 20] for all stress voltages, while the PMOSFET is more likely to break down to a greater extent at higher stress voltages. Three breakdown modes have been induced in the PMOSFET, as indicated by the labels in Fig. 5(d), but similar modes are observed for each device after both positive and negative stress. Stress induced leakage current (SILC) is present at the lowest positive stress voltage [13]. As the stress magnitude increases, a large range of LHBD is observed, which at times is followed by HBD. In addition, the leakage current for negative stress [(a)/(b)] increases over one order of magnitude at +/- 1.8V, while positive stress [(c)/(d)] increases over two orders of magnitude. Comparison of Fig. 5(a) and (b) reveals that after -12 V stress, the nMOSFET suffers from LHBD while the pMOSFET has undergone HBD. This behavior is present for positive circuit-level stress as well [Fig. 5(c) and (d)].







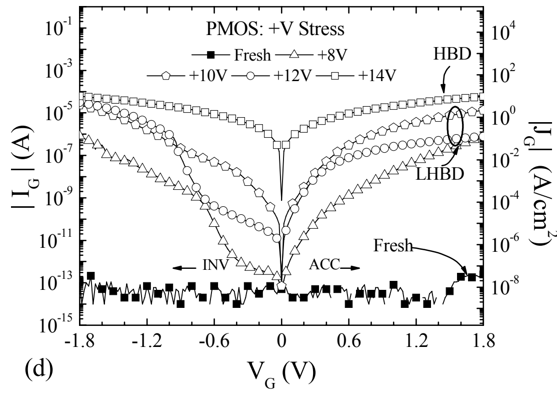
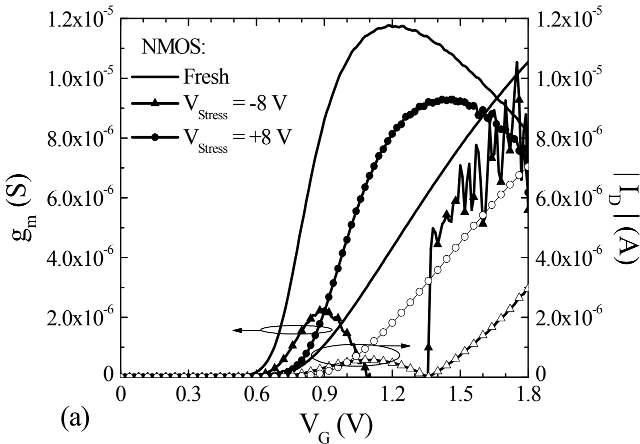


Fig. 5. Post-stress I_G-V_G leakage current data after circuit-level stress. (a) NMOSFET negative stress, (b) PMOSFET negative stress, (c) NMOSFET positive stress, and (d) PMOSFET positive stress. The operating modes of each transistor are indicated in each figure.

Fig. 6 compares pre- and post-stress g_m and linear I_D-V_G results following +/- 8 V stress for the NMOSFET and PMOSFET devices. In general, with increasing stress magnitude (positive or negative), a decrease in g_m and increase in V_t are observed for both NMOSFET and PMOSFET devices. The NMOSFET shows increased degradation in both g_m and linear I_D-V_G behavior than observed in the PMOSFET stressed with the same voltage magnitude, which was typical of all negative voltage stress data.



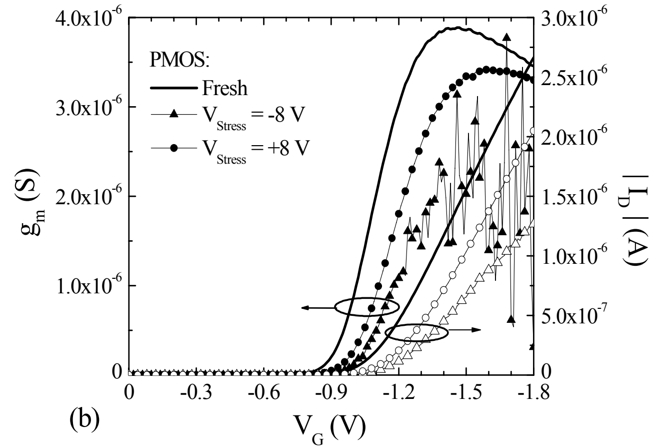
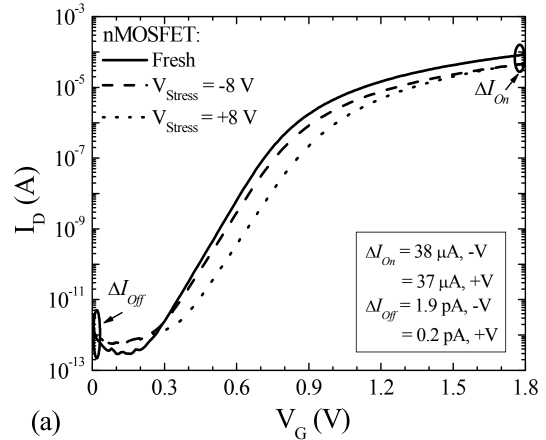


Fig. 6. Comparison of fresh and post-stress g_m and linear I_D-V_G characteristics for (a) NMOSFET and (b) PMOSFET, after +/- 8V circuit-level stress.

Fig. 7 compares the log I_D-V_G (subthreshold characteristics) results following +/- 8 V stress for the (a) NMOSFET and (b) PMOSFET devices. It is observed that the subthreshold slope has increased by at least 15 mV/dec in the NMOSFET and 5 mV/dec in the PMOSFET. Additionally, the change in I_{Off} and I_{On} is given in the figure and designated by ΔI_{Off} and ΔI_{On}. For -8 V stress, ΔI_{On} is observed to be higher for both the NMOSFET and PMOSFET. Conversely, ΔI_{Off} for the PMOSFET (b) shows a greater change after +8 V stress when compared to the NMOSFET.



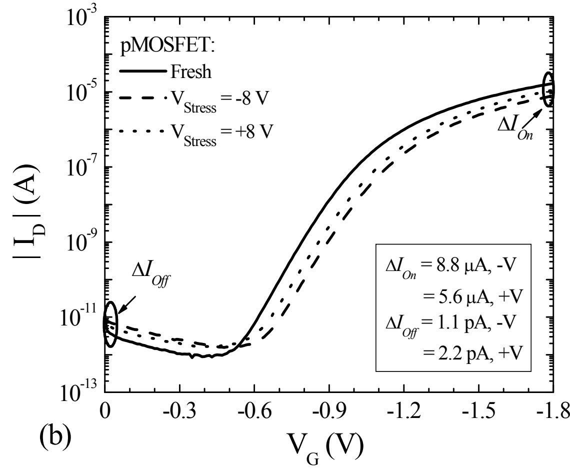


Fig. 7. Comparison of fresh and post-stress log I_D-V_G characteristics for the (a) NMOSFET and (b) PMOSFET devices following +/- 8 V circuit-level stress.

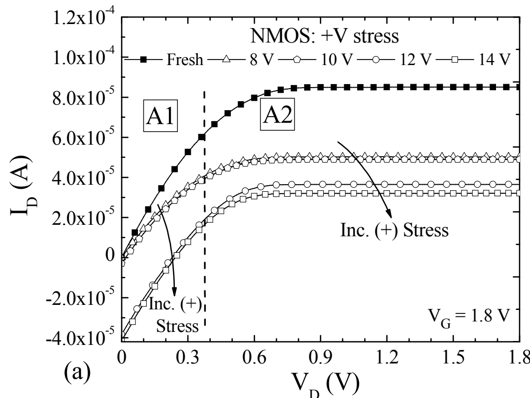
Fig. 8 shows the I_D-V_D characteristics for each device after various degrees of (a)/(b) positive and (c)/(d) negative stress. Curves for $|V_{Gate}|$ of 1.8 V are plotted, but the behavior is similar for lower gate voltages. Generally, as stress magnitude increases, a substantial decrease in $I_{D,MAX}$ is observed. However, from Fig. 8 it is apparent that different trends are observed for positive and negative stress. In order to evaluate these results, each plot identifies two areas of interest: A1 and A2 are designated as the linear and saturation regions, respectively [11]. The relationship between the drain-to-source voltage (V_{DS}), gate-to-source voltage (V_{GS}), and MOSFET threshold voltage (V_t) are given for each area in expressions (2) and (3). Additionally, region A1 requires that for the MOSFET to be turned "on", $V_{GS} > V_t$, otherwise $V_{GS} < V_t$ and the device is "off".

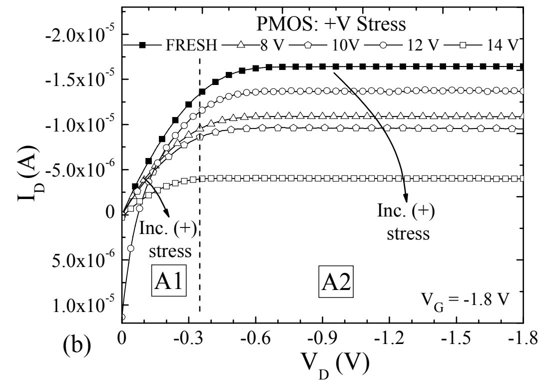
$$V_{DS} \leq V_{GS} - V_t \text{, for A1} \quad (2)$$

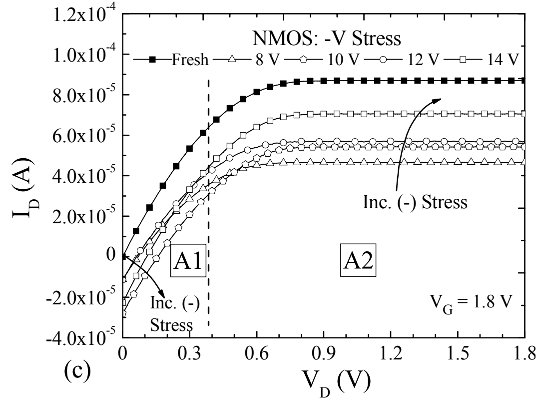
and

$$V_{DS} \geq V_{GS} - V_t \text{, for A2.} \quad (3)$$

From Fig. 8(a) and (b) it is observed that regions A1 and A2 follow a similar trend after positive stress of either the NMOSFET or the PMOSFET. Experimental results show that as the magnitude of the stress increases, $I_{D,MAX}$ decreases.







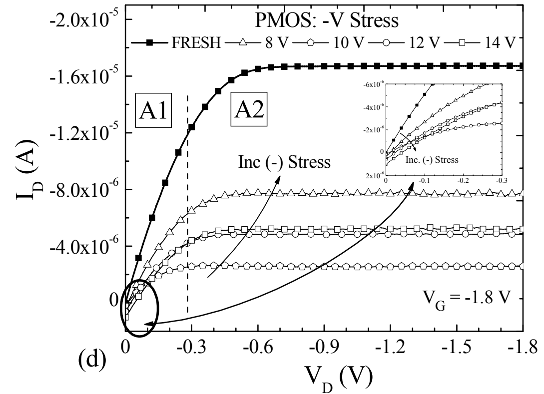


Fig. 8. Comparison of fresh and post-stress I_D-V_D results showing degraded on-currents following circuit-level stress. (a) NMOSFET positive stress, (b) PMOSFET positive stress, (c) NMOSFET negative stress, and (d) PMOSFET negative stress.

However, regions A1 and A2 of Fig. 8(c) and (d) do not follow the same trend. Typically for negative stress, region A1 is similar to the positive stress results, yet the negative results for (c) region A2, indicate that at lower stress magnitudes $I_{D,MAX}$ for the NMOSFET is decreased significantly compared to higher stress voltages. A similar trend for $I_{D,MAX}$ is observed for the PMOSFET (d) for stress voltages greater than -8 V.

Inverter Performance

Experimental and simulated VTCs for inverters stressed in circuit-level configuration are shown in Fig. 9(a) and (b). Solid lines represent experimental data and symbols indicate simulated VTCs.

The circuit model (Fig. 12) used to simulate degraded inverter VTCs is explained in more detail in the following section. In general, as the magnitude of the positive stress increases [Fig. 9(a)], V_{OH} decreases and V_{OL} increases, resulting in decreased inverter output swing. When the stress voltage is ramped to 14 V, V_{OL} increases by 240 mV and V_{OH} is reduced by 20 mV. The changes in V_{OL} are larger and occur at lower stress voltages than those in V_{OH}. V_{SP} initially increases or shifts right with increasing stress magnitude. At the highest stress voltages, V_{SP} decreases and is similar to that of the fresh inverter.

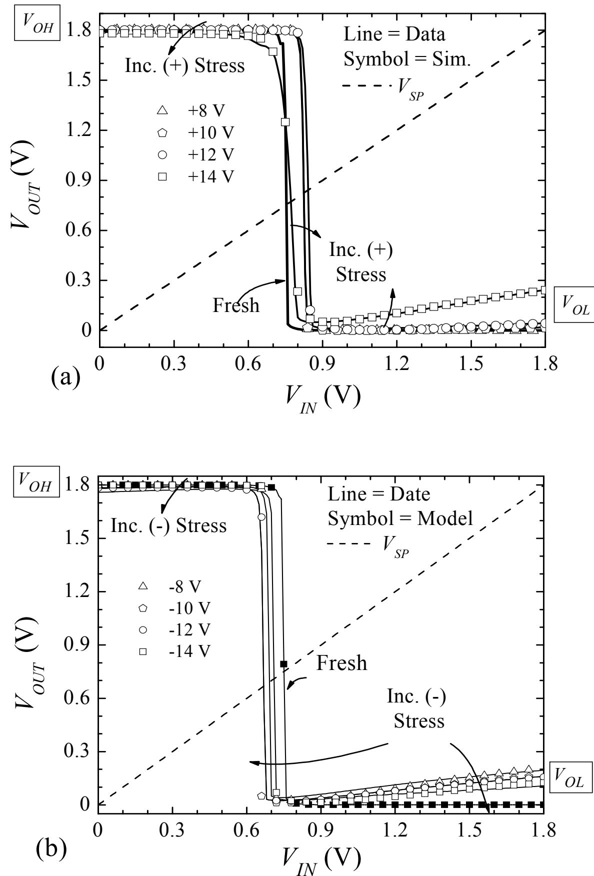


Fig. 9. Inverter VTCs following circuit-level stress. The magnitude of the RVS varied from +14 V to -14 V. (a) Positive voltage stress (b) negative voltage stress. Solid lines represent experimental data and symbols indicate simulated VTCs.

VTC results for negative circuit-level stress [Fig. 9(b)] are similar, but have slightly different trends. Compared to the positive stress case, V_{OH} and V_{OL} tend to decrease with increasingly negative stress. The change in V_{OH} is typically larger for negative stress than for positive stress, while V_{OL} is typically highest at low stress voltages, and then decreases with increasing stress voltage. V_{SP} tends to shift left and initially decreases with increasing stress magnitude, similar to the response observed in V_{OL}.

From the VTCs alone, it appears that the inverter performance has not been severely degraded at lower stress voltages. However, examining the time-domain behavior reveals otherwise. Shown in Fig. 10 are the time-domain responses, to a 2.5 kHz square wave input, of inverters that have been stressed with an (a) positive ramped voltage and (b) negative ramped voltage. In general, after positive/negative stress, it is observed that as the stress magnitude is increased the inverter voltage output swing in the time domain is significantly decreased. It is interesting to note that the trends in region I and region II follow those trends observed in Fig. 9 for V_{OH} and V_{OL}, respectively. However, for region I of (a) and (b), after the largest positive/negative RVS, $V_{Out,MAX}$ has decreased from 1.8 V fresh to 660 mV/440 mV, respectively. In comparison, V_{OH} decreased from 1.8 V fresh to 1.78 V post-stress. Conversely, for region II of (a) and (b), the voltage magnitude of $V_{Out,MIN}$ is very similar to that observed in V_{OL} from the transfer characteristics.

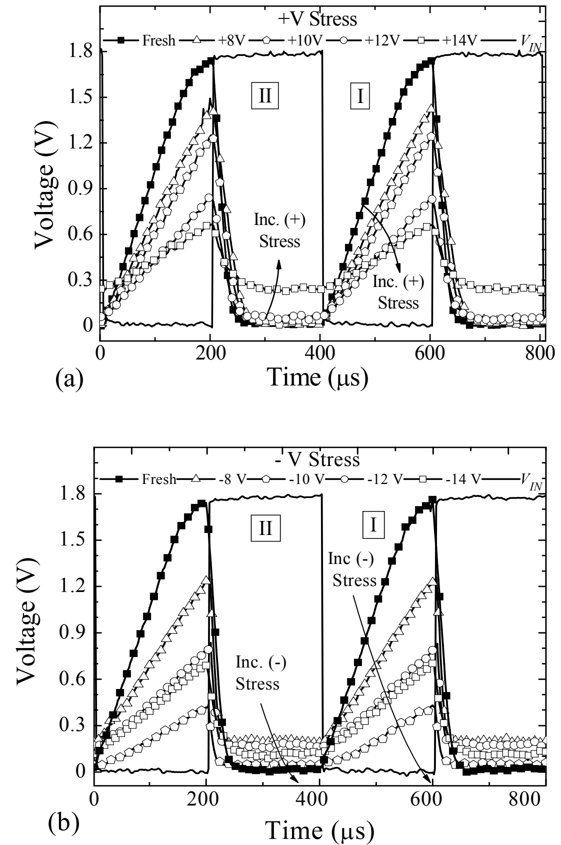


Fig. 10. Inverter V-t characteristics after various magnitudes of RVS. (a) Positive stress response and (b) negative stress response. V_{IN} defines the digital input signal, while Fresh and various stress voltages represent the digital output signal.

Unlike region I which shows that as the stress magnitude is increased (positive or negative) $V_{Out,MAX}$ is significantly decreased, region II shows that opposite behaviors are observed for each stress polarity. For instance, in the positive stress case [Fig. 10(a)], $V_{Out,MIN}$ increases with increasing stress magnitude and reaches a maximum of 248 mV (ideal = 0 V) following +14 V stress. Alternatively, for negative stress [Fig. 10(b)] $V_{Out,MIN}$ increases with decreased stress magnitude to a maximum of 196 mV following –8 V stress.

Inverter input leakage currents following (a) negative and (b) positive voltage stress are shown in Fig. 11. Various degrees of inverter degradation are observed for positive/negative stress. Input

leakage current is typically highest at -1.8 V for both cases. Furthermore, leakage currents for negative stress are generally higher where a difference of 60 μA or more is observed, relative to positive stress of equal magnitude.

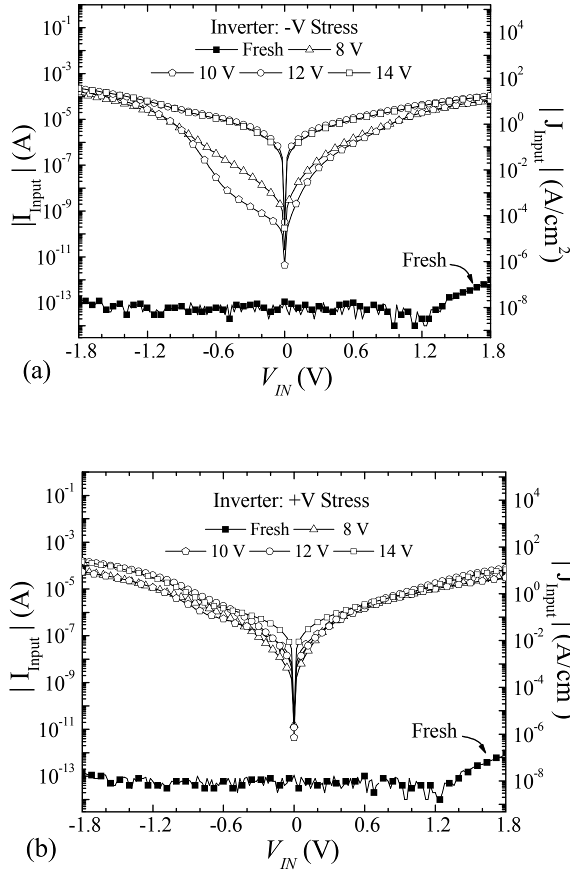


Fig. 11. Pre-and post-stress inverter input leakage current monitored for (a) negative and (b) positive, circuit-level stress experiments.

Circuit Model

Various circuit models for stressed inverters have been proposed [14, 15]. It was reported [14] that the percolation path at the breakdown spot is primarily composed of the phosphorus dopant of the polysilicon gate. This results in an ohmic contact to the n+ source/drain regions of the NMOSFET and formation of a diode at the p+ source/drain regions of the PMOSFET. It has been suggested that an ohmic model does not provide a good fit for experimental data of inverters [15] if the degradation mechanism observed is not comparable to hard breakdown (HBD). Furthermore, the diode effect for both transistors can be explained if the percolation path, or at least the contact to drain regions, is intrinsic silicon.

Fig. 12. Circuit model used to simulate degraded inverter VTCs.

The circuit model used in this study to simulate the operation of degraded inverter VTCs is shown in Fig. 12. The model is similar to that in [14], but different due to a resistor-diode pair introduced to simulate gate-to-drain breakdown in the NMOSFET and the PMOSFET, rather than the PMOSFET alone. The diode emission equation [11] is given by:

$$I_D = I_S \cdot [\exp(V_D / N \cdot V_t) - 1] \tag{4}$$

where the parameters are defined as saturation current (I_S), diode voltage (V_D), emission coefficient (N), and thermal voltage (V_t). Adjusting the variable, N, alters the bias voltage at which the diodes begin conducting.

The resistors from MOSFET gates (V_{IN}) to sources (V_{DD}, GND) are altered to accommodate the statistical distribution of the post-breakdown resistance of the percolation path. In addition, MOSFET threshold voltage shifts are included in the model, which provides a closer fit to the experimental results.

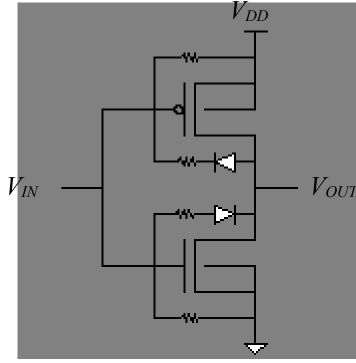
Discussion

MOSFET Characteristics

Changes in MOSFET parameters such as I_D-V_D, g_m, and linear I_D-V_G characteristics were observed for circuit-level stressing. When the gate oxide suffers dielectric breakdown under circuit-level stress, gate control over the channel may be severely reduced (Fig. 8). This can alter the polarity of the current in the linear region (A1) thus inhibiting channel inversion. The differences observed in regions A1 and A2, particularly for negative stress, suggest that changes in the threshold voltage are less for lower voltages, which results in the degraded device turning on more quickly (steeper slope), thus saturating at a lower current level. Furthermore, circuit-level stress results in decreased g_m (Fig. 6), which may be due to stress-generated charge traps that can reduce the number of mobile carriers [16]. This is somewhat substantiated by the higher leakage currents (Fig. 5). Additionally, off-state currents often increase (Fig. 7) which can result in increased power consumption [11].

Several types of oxide degradation occur following circuit-level stress, such as SILC, LHBD and HBD. It has been proposed that HBD is more probable in large area devices [17, 18]; however, the results for individual devices suffering circuit-level stress suggest that these degraded oxides exhibit some degree of LHBD more often than HBD, even at high gate voltages. Of particular interest is the evidence that MOSFETs can independently experience different degradation mechanisms while in the inverter configuration [Fig. 5(a) and (b)]. For either polarity, the device suffering a higher degree of oxide degradation may dominate the breakdown, eventually causing circuit failure. Further, MOSFET inversion mode operation (Fig. 8) seems to be more heavily influenced by negative voltage stress, supported by leakage current data in Fig. 5. This indicates that the PMOSFET is influenced more by inversion stress and the NMOSFET by accumulation mode stress.

Comparing the leakage currents of degraded MOSFETs (Fig. 5) to



those of degraded inverters (Fig. 11), similarities between the two are evident. However, there are some differences that may be attributed to current leakage at the drain, source, and bulk nodes of the devices [13].

Inverter Performance

As reported in recent work [4, 10] and supported by our findings, the VTC of post-stressed inverters show decreased voltage output swing following gate oxide degradation (Fig. 9). However, the difference between these studies shows that for the larger devices used in this study, on-currents can dominate the leakage current even after several orders of oxide degradation. This may explain why the degraded circuit behavior presented in this study, is not as exaggerated as previously reported. Shifts in the inverter switching point (V_{SP}) are also observed when the inverter is stressed (Fig. 9). As reported in [4], this could be due to interface state generation or charge trapping in the oxide [16], or possibly a combination of both. In general, as the stress magnitude is increased, V_{SP} increases. However, a clear correlation between stress magnitude and the amount of shift is not always apparent.

A link between VTC performance and region II of the V-t response can be seen by comparing V_{OL} (Fig. 9) and $V_{Out,MIN}$ (Fig. 10). The post-stress V-t results following positive and negative circuit-level stress, indicate that $V_{Out,MIN}$ is consistent with V_{OL} for both stress polarities. This may be explained by the differing response of the NMOSFET to the polarity of the stress in the saturation region (A2) of the I_D-V_D characteristics [Fig. 8(c)]. For increasing negative polarity, a general increase in I_D is observed in the A2 region which should manifest a decrease in V_{OL} [Fig. 9(b)] and $V_{Out,MIN}$ [Fig. 10(b)]. However, the inverse relation is observed. The opposite occurs for positive stress polarity as seen in Fig. 9(a) and 10(a). The opposing circuit responses to changes in polarity may be due to the leakage currents at the various terminals of the inverter [13].

Unlike $V_{Out,MIN}$, the magnitude of the response for $V_{Out,MAX}$ does not match that of the VTC (Fig. 9 and 10). One particular discrepancy is observed with respect to the rise time. Several factors may attribute to the rise-time increase, such as a decrease in the effective carrier mobility of the PMOSFET due to interface states created during stressing [16], the large area of the devices, or the inverter device ratio being 1:1 (PMOS:NMOS), where a more ideal case would be a ratio of at least 2:1 [11]. Moreover, increased charging time for parasitic capacitances, due to increased leakage currents, may also limit the rise-time. However, if the test frequency is decreased significantly the final $V_{Out,MAX}$ values approach those of the VTCs.

Circuit Model

VTCs of positive and negative stressed inverters (Fig. 9) are fit well by varying a few parameters contained in the model. The development of this model came about after preliminary examination of the individual transistor leakage current components. The data suggests that the drain current is usually lowest and diode-like, whereas the substrate and/or source currents are usually highest and nearly linear (i.e. ohmic). However, these results may vary depending on the MOSFET operation mode being investigated. Consequently, these findings may be a result of the manner in which the inverter is stressed. The ideas presented above will be developed in a future study and supported with experimental data [13].

It has been reported that in certain digital applications, the gate-to-source leakage current may generate a worst case scenario [6]. For this study, further examination of the leakage current components suggests that gate-to-substrate leakage currents may dominate the total leakage current. In addition to the preliminary analysis of the leakage currents, Spice simulations revealed that only gate-to-drain breakdowns seem to affect the inverter VTCs. Conversely, inverter time-domain performance was shown to be severely degraded when little to no gate-to-drain breakdown has occurred (Fig. 10). These discrepancies can potentially be addressed by simulating the voltage-time domain behavior with the model presented in this study, or perhaps by incorporating other circuit elements. To perform this task, additional analysis of all MOSFET leakage currents is required and will also be explored in the upcoming study [13].

Conclusion

The effects of circuit-level stress on circuit operation and individual transistors were investigated. On the transistor level, increased stress of either polarity results in increased gate leakage current, decreased g_m, decreased $I_{D,MAX}$, and increased V_t for the NMOSFET and the PMOSFET. Degraded inverter VTCs were simulated using a new circuit model. In general, increasing stress of either polarity resulted in reduced output swing of the inverter VTC, similar to that reported in [5]. Decreased inverter voltage output swing was also observed in the time domain. However, more significant changes were observed with respect to the inverter rise and fall times. Hence, VTC measurements may show negligible inverter degradation; yet, V-t behavior of the inverter may be severely degraded. Consequently, the V-t data, presented for the first time, introduces a new characteristic for digital circuit reliability. Several published reports call for more suitable circuit reliability criterion [6, 7, 10].

In terms of circuit reliability, subsequent stages in a larger circuit

may be able to compensate for one degraded SICBB [7], increased rise/fall times and delays could potentially cause timing issues in high speed circuits. Additionally, large leakage and off-state currents can be present without severe VTC degradation, leading to loading of previous circuit stages and increased power consumption [11].

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