

# Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs)

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## Abstract

Measurements using a pulse voltage stress (PVS) technique whereby dual pulse waveforms, differing in phase, gave rise to astonishing preliminary results: the lifetime of the devices were substantially reduced as compared to both constant voltage stress (CVS) and single waveform PVS.

We also report on degradation mechanisms in nMOSFETs and their effect on inverter operation. We show for the first time the effect of limited hard breakdown (LHBD) [1,2] on inverter operation.

## Introduction

Currently, the primary reliability stress test method for determining degradation mechanisms and lifetime of gate dielectrics is the CVS test[4, 5]. However, IC devices are operated in either digital or analog mode. CVS tests do not approximate either of these modes. An alternative method to better mimic digital and analog device operation is PVS. But our initial research on ultrathin gate oxides and work done by others indicates that PVS testing requires longer testing times than CVS testing [6-8]. However, experiments using a PVS technique whereby dual pulse width waveforms, differing in duty cycle and phase, resulted in a significant reduction of device lifetime as compared to both CVS and single waveform PVS. It is quite possible that dual waveforms can occur in digital and analog ICs.

The deficiency in experimental studies examining the effect of oxide degradation and breakdown in MOSFETs on simple ICs have prompted several experts in the field to emphasize the need studies of the effects of both SILC[9], SBD[10-11], and LHBD on circuit reliability.

## Experimental Procedures

**Dual Waveform:** nMOSCAPs were used with an oxide thickness and area of 3.2nm and  $2.1 \times 10^{-4} \text{cm}^2$ , respectively. The configuration used to test these devices is shown in figure 1. Two waveform generators (WFGs) in parallel were configured to output 5KHz, 5-V peak-to-peak, 50% duty cycle (D.C.) square wave pulse trains phase shifted by  $90^\circ$ . The number of pulses, read by the counter, was used to determine the equivalent time to breakdown. The results were compared to time to breakdown data from single waveform PVS and CVS stress tests using the same applied voltage stress. Because dielectric breakdown occurs at lower voltages in accumulation [2,3], devices were tested in accumulation.

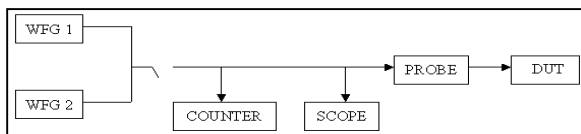


Figure 1: Configuration for dual waveform experiments.

**SICBBs:** A series of pre- and post-stress tests were conducted on each inverter to monitor changes in the transfer and voltage-time (V-t) characteristics. All stress tests were performed on the gate oxide of the nMOSFET with the drain and source floating and well tied to 0V. This set up mimics the nMOSCAP tests described previously. The stress-induced degradation of the nMOSFET was LHBD produced by

a ramped voltage stress (RVS) stress from 0 to -12V. The inverter was configured using an nMOSFET and pMOSFET device, both with a gate oxide area of  $625 \mu\text{m}^2$  and a thickness of 3.2nm. Test conditions:  $V_{IN}=2\text{V}$ ,  $F=2.5\text{KHz}$ ,  $D.C.=50\%$ , and  $V_{DD}=2\text{V}$ .

For both the dual waveform and SICBB experiments, the type of degradation and/or breakdown mechanism of the device was determined by pre- and post-stress I-V tests. The test voltage was low enough to avoid further degradation of the oxide. All experiments were performed in a Faraday cage using an Agilent 4156C.

## Results

**Dual waveform:** Figure 2 shows the V-t output from the oscilloscope during a dual waveform experiment. Because of the superposition principle of waves, constructive interference occurs. Thus, during short time intervals, the amplitude of the original signal is doubled causing the voltage to increase to -10V. Figure 3 shows the Weibull distribution of failures versus time to breakdown ( $t_{bd}$ ) for CVS, single pulse PVS, and dual pulse PVS. The  $t_{bd}$  for the dual pulse tests were about 2 orders of magnitude less than CVS or single pulse PVS. Post-I-V results indicated that breakdown mode was LHBD.

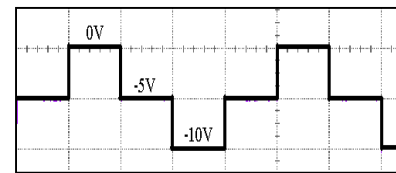


Figure 2: Input signal to the DUT during dual waveform tests.

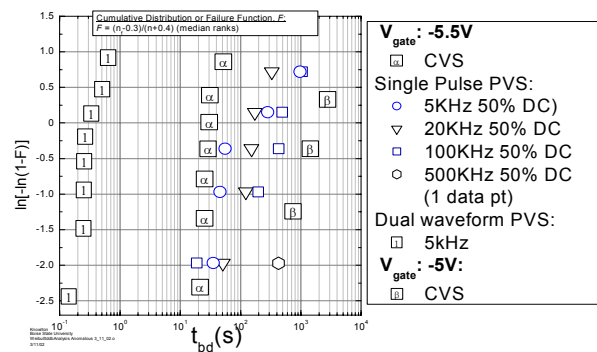


Figure 3: Weibull plot showing the  $t_{bd}$  data from the dual waveform experiments using nMOSCAPs.

**SICBBs:** The pre- and post-stressed inverter V-t characteristics are shown in Figure 4, respectively. The unstressed inverter response is typical. When the input node is 2V (high) the output node is pulled down to 0V (low). However, for the inverter stressed to LHBD, the output voltage level does not reach zero when the input voltage is 2V. This response was verified when compared to the voltage transfer curve (VTC) in Figure 5. The output voltage level in both cases increases from 0V to approximately 250mV on the nMOSFET side.

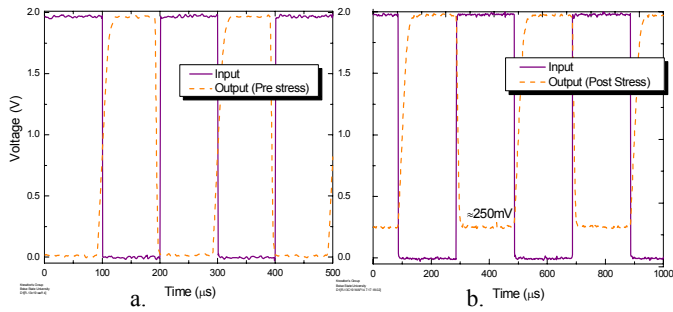


Figure 4: Pre- and post-stress inverter V-t characteristics.

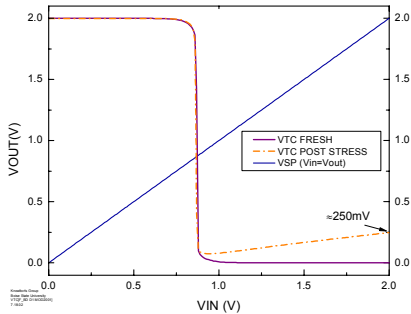


Figure 5: Pre- and post-stress inverter VTC characteristics.

### Discussion and Summary

**Dual waveform:** The significance of the dual waveform results focuses on the superposition of waveforms. During short intervals, the voltage doubles to  $-10V$ , which is greater than the measured breakdown voltage in accumulation ( $-6.5V$ ). These initial results prompt the question: what are the potential reliability issues in CMOS circuits? Circuit level reliability issues include, but are not limited to, noise and capacitive coupling. Figure 6 shows a diagram of a Precharge-Evaluate gate. During normal circuit operation, a typical input to the gate of M4 would appear as a varying signal with VDD 95V. Additional noise or signal interference from an adjacent interconnect can be coupled at this node leading to an increase in the signal voltage due to constructive interference. Figure 6b illustrates the result of a noise pulse coupled with the output node.

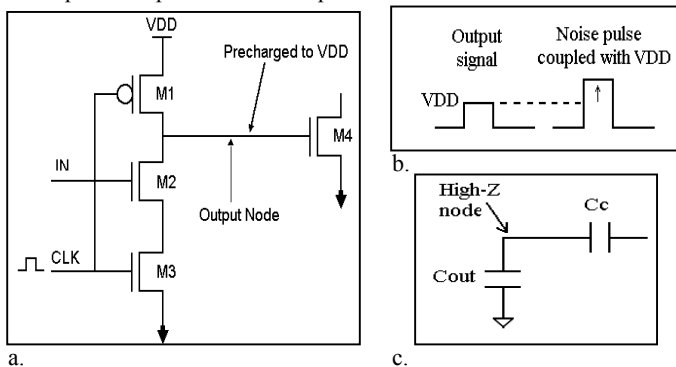


Figure 6: a. Dynamic gate b. Noise coupling. c. Circuit model.

Furthermore, the output node, pre-charged to VDD, is a high impedance ( $Z$ ) node, only when M1 and M2 are off. Thus in dynamic gates these high- $Z$  nodes can appear capacitive, and if coupling exists between this node and a varying signal, (e.g., clock pulse), this can lead to capacitive coupling and ultimately degrade circuit performance. Figure 6c represents a circuit diagram for this type of behavior, where the capacitance at the output node is labeled  $C_{out}$  and the resulting coupling capacitance is given by  $C_c$ . The magnitude of the signal increases as the capacitive coupling increases—indicating that as circuit densities continue to increase, noise and capacitive coupling become an even greater reliability issue. This demonstrates

the relevance of dual waveform testing as described in the previous section.

**SICBBs:** Preliminary results have shown that LHBD influences circuit operation. The degraded inverter characteristics shown in figures 4 and 5 can lead to possible circuit issues, especially for high-speed digital systems, including increased power consumption and reduced noise margins.

As mentioned in the previous section, when the input to the inverter is high and the gate of the nMOSFET has been stressed, the nMOSFET may no longer be able to pull the output to low. In comparison, when the input is low, the pMOSFET may have difficulty pulling the output node to high, unless the drive current from the pMOSFET can compensate for the leakage current through the gate of the nMOSFET. This suggests that in order for the circuit to compensate, more power will be consumed. However, future experiments are required to better understand the relationship between these currents.

Initially, the post VTC characteristic could be interpreted by assuming the gate of the pMOSFET has been stressed. However, from post stress I-V measurements, it is shown that the device has undergone LHBD. The 250mV increase on the output voltage level is due to high leakage current through the gate, which was measured to be  $-491\mu A$ . This increased voltage level indicates that the noise margins can vary.

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