Design and Layout of Schottky Diodes in a Standard CMOS Process

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***Abstract*—This paper addresses several concerns for increasing the frequency range in a Schottky diode detector circuit through a layout design solution. To increase the frequency and active range of the diode, reducing the series resistance was the first concern addressed, this was accomplished by interdigitating the fingers of the Schottky and ohmic contacts. The capacitor was laid out in a manner to decrease charge lost to the substrate through the parasitic substrate capacitance. For added accuracy, an averaging resistor/capacitor was added to isolate the Schottky diode detector circuit from the measuring circuit. With these improvements in the layout design, it is expected that the frequency and dynamic range of the Schottky diodes in the detector circuit will be extended further into the GHz range.**

1. Introduction

Due to their favorable characteristics in high frequency applications, Schottky diodes have been widely used in various RF power detection circuits [1], [2]. Despite the popularity and economic advantages of CMOS the lossy nature of the silicon substrate has made the implementation of CMOS into full-scale microwave use relatively slow going. As frequencies continue to increase the undesirable effects of the silicon substrate become more and more apparent. The purpose of this paper is to describe layout design improvements for RF power measurements in a typical Schottky detector circuit, Fig1. Designs have been introduced and reported with the frequency range extended to 600MHz [2]. When the cost of adding additional process steps is considered, the importance of a layout design solution in a standard fabrication process is paramount. Clever techniques have been reported but these are fabricated with special processes not readily available or financially feasible in a full-scale fabrication facility [3]. The need exists for designs that are easily manufactured and can be implemented directly into a standard process without adding costly procedure steps. The layout design of the Schottky diode can be improved, reducing unwanted parasitics, thereby increasing the frequency range.

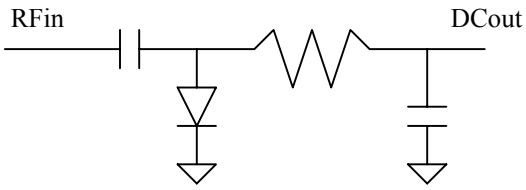

Fig. 1 Diode detector circuit.

2. Schottky diodes

The designs were fabricated through MOSIS [4] with AMI's .5um process. The layout editor, LASI (LAyout System for Individuals), was used in laying out the designs [5], [6]. Schottky diodes are commonly used in high frequency applications because of their favorable high speed switching characteristics [7]. The dominant transport mechanism in a Schottky diode is due to the majority carrier, as opposed to a p-n diode where the minority carrier is dominant. Thus, we have no stored charge effects and a quicker switching time. A Schottky diode is formed when a metal layer is deposited directly onto a low doped n-type or p-type semiconductor region. When the two materials are brought into contact with each other the difference in potential gives rise to a barrier height that the electrons have to overcome for current

to flow. The metal on the low doped semiconductor is the anode and the semiconductor material, contacted through an ohmic contact, is the cathode. As an input signal is applied to the anode, the barrier height either raises or lowers allowing current to flow, or blocking current, from the anode to the cathode. Only n-type Schottky diodes were used for our designs. Our designs did not include p-type diodes due to the almost equal work functions of the p-substrate and the aluminum, thus no difference in potential between the semiconductor and the metal, and no barrier exists. For comparison in designs, three different sized diodes; 30µm, 40µm, 50µm, were laid out in the square and interdigitated configuration. All designs included the capacitor and resistor with the device on the same IC.

3. Diode Design

The first improvement in the design layout was reducing the series resistance of the Schottky diode. This was accomplished by interdigitating the fingers of the ohmic and Schottky or rectifying contacts. The distance between the Schottky and ohmic contacts were reduced to the minimum allowable distance according to the design rules. For the 30µm square diode the distance between the center of the metal region to the semiconductor is 18µm as opposed to the interdigitated layout which reduces the distance between the center of the two contacts to 3.5µm. As the size of the diode increases the distance between the metal and semiconductor also increases, with the interdigitated layout the minimum distance stays the same, the number of fingers and the length increases. Shown in Fig. 2 is a cross-sectional view comparing the two layouts and the series resistance. Note, the representation of the series resistance is a worst case view. Fig. 3 is a layout view of both the square and interdigitated designs.

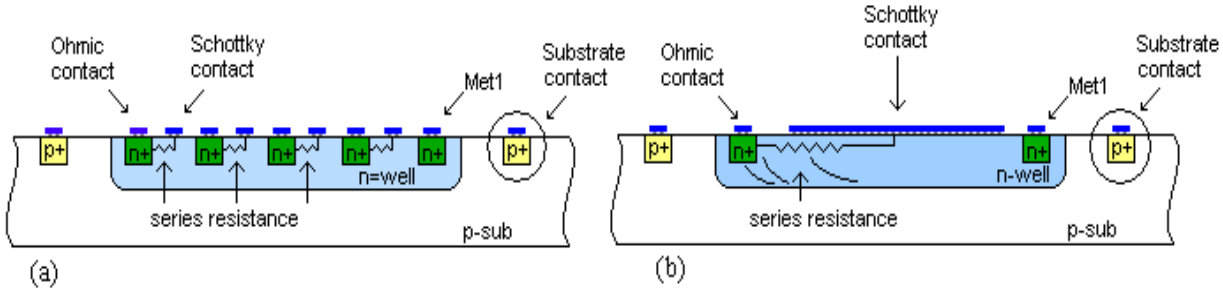

Fig. 2. (a) interdigitated diode cross-sectional view (b) cross-sectional view of the square diode, Note the electrons being swept down to the substrate

The interdigitated layout also offered another advantage over the square layout. As the barrier height is lowered electrons travel from the semiconductor to the metal area offering them an opportunity to get swept down to the substrate, thus losing charge. This was never directly measured but is easy to conceptualize and is shown in Fig.2 (a). Interdigitating the fingers greatly reduced the distance from the anode to cathode, eliminating the likelihood of electrons being swept down to the substrate.

4. Capacitor Design

Further reducing unwanted noise and parasitics we coupled the capacitor together with the device on the same IC rather than coupling the capacitor externally. The charge received on the input end of the capacitor must be transferred through to the rest of the circuit. Using a regular layout design (poly1/poly2 or met1/met2), for the capacitor would have resulted in lost charge through the substrate due to the parasitic capacitance from the top of the substrate to the bottom metal or poly layer. To minimize the amount of charge lost to the substrate only the top metal layers were used. The AMI .5um process allows for 3 metal layers. The capacitor was designed with the top two metal layers only, thus increasing our distance from the substrate, decreasing the parasitice capacitance and minimizing lost charge through the body.

The capacitor was also designed in an interdigitated manner with metal 2 and metal 3 connected together with via 2. The minimum distance allowed, according to the design rules, between the fingers giving us our capacitance. Sizing was set to dominate over the junction capacitance of the n-well and substrate. A quick calculation of the layout provided us with a value of approximately .5pF, this value will be higher when in the actual working circuit because of the fringe capacitance, which was not included in the calculation.

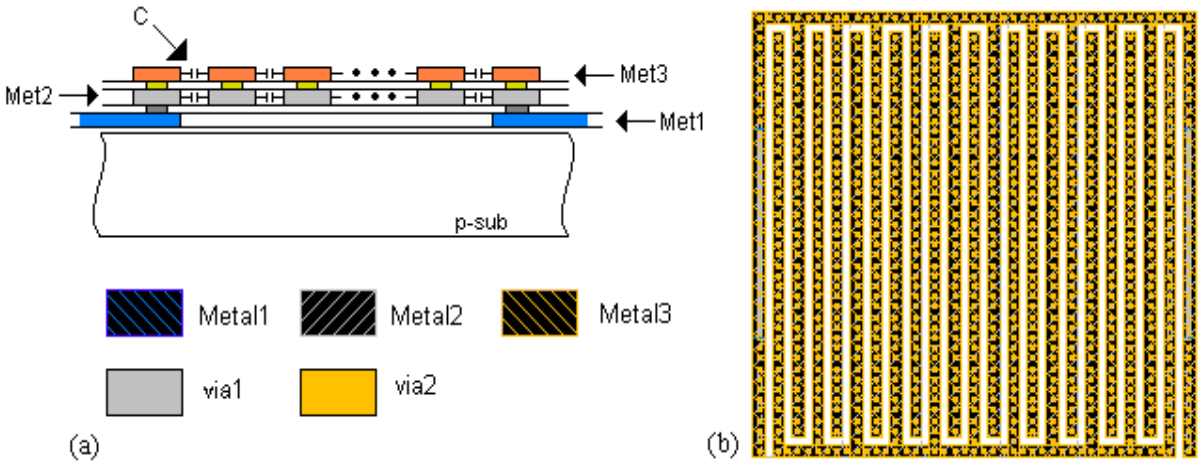

Fig. 3 (a) cross-sectional view of the capacitor showing the top metal layers used for the capacitance (b) layout view of the capacitor including layers.

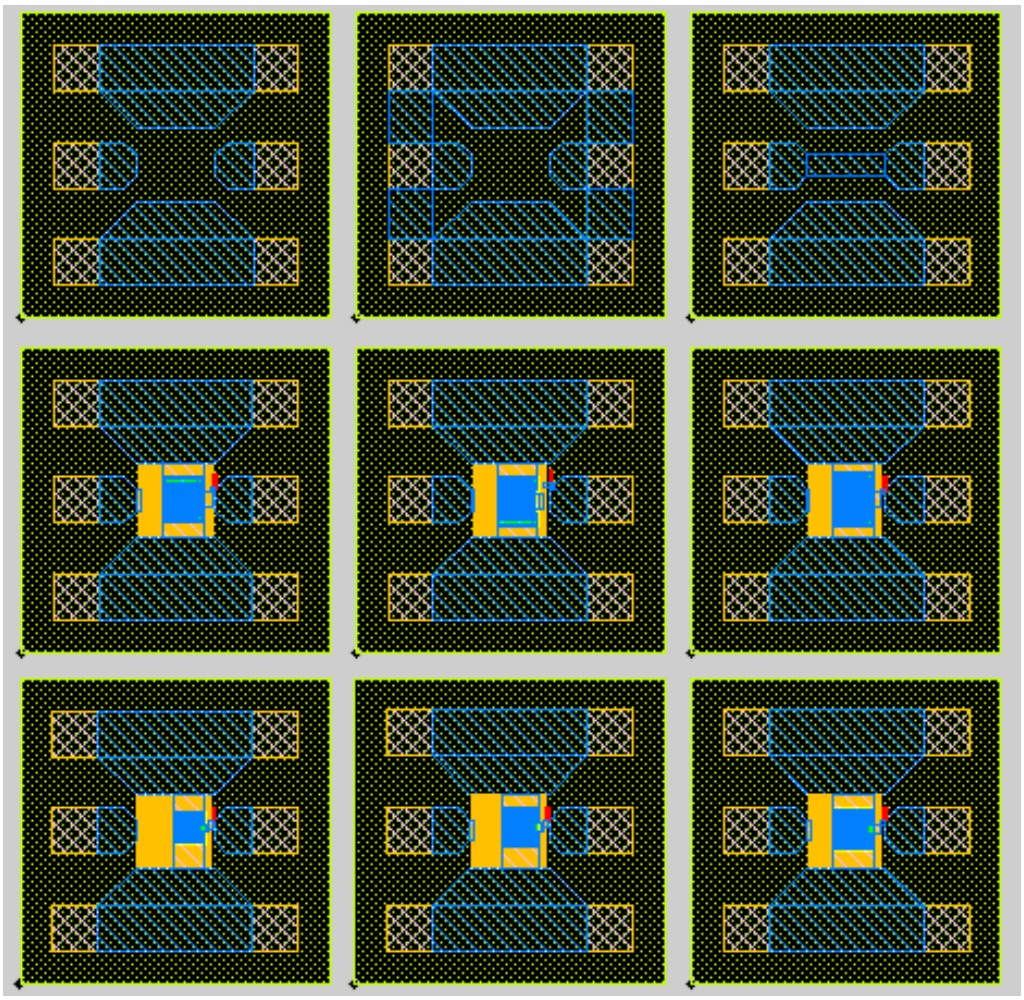

Fig. 4. Complete layout view.

5. Conclusion

The series resistance of the Schottky diode was reduced by interdigitating the fingers of the Schottky and ohmic contacts. To reduce lost charge through the substrate body, the capacitor was laid out in a horizontal, rather than vertical manner, by tying Met2 /Met3 with Via2 and interdigitating the fingers. A resistor was added to the detector topology to average the low-high and high-low switching times. The devices were laid out in a fixture with ground-signal-ground (GSG), and submitted to MOSIS for fabrication in the AMI .5μm process. Results of these design improvements will be documented upon return of the devices from MOSIS.

REFERENCES

[1] A. Simon, C.I. Lin and M. Rodriguez-Girones, "Substrateless Schottky diodes for THz Applications", *8th Int. Symposium on Space Terahertz Technology,* March 1997, Harvard University, Cambridge, Mass., USA.

[2] V. Milanovic, M. Gaitan, E. Bowen and M. E. Zaghloul, "CMOS Foundry Implementation of Schottky Diodes for RF Detection", *IEEE Transactions on Electron Devices,* Vol. 43, No. 12, Dec. 1996.

[3] A. Simon, C. Lin, "Planar Schottky Barrier Diodes for THz Applications",

[4] C. Tomovich, "MOSIS—At gateway to silicon," *IEEE Circuits and Devices Mag*., vol. 4, no.2, 1988.

[5] Baker, R.J., "A Windows based integrated circuit design tool for distance education", *International Conference on Simulation and Multimedia in Engineering Education*, 1999.

[6] Boyce D.E. and Baker R.J., (1997) "A Complete Layout System for the PC," *Midwest Symposium on Circuits and Systems*, 1998 .

[7] G. Neudeck, R. Pierret, "*The PN Junction Diode*," Vol. 2, Addison-Wesley, 1989.