Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices

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***Abstract*—A reliable configuration for triggering a series string of power metal oxide semiconductor (MOS) devices without the use of transformer coupling is presented. A capacitor is inserted between the gate and ground of each metal oxide semiconductor field effect transistor (MOSFET), except for the bottom MOSFET in the stack. Using a single input voltage signal to trigger the bottom MOSFET, a voltage division across the network of device capacitance and inserted capacitances triggers the entire series stack reliably. Design formulas are presented and simple circuit protection is discussed. Simulation shows reliable operation and experimental verification is presented. Application of the method is applied to series insulated gate bipolar transistors (IGBTs).**

***Index Terms*—MOSFET-series connection, power MOS devices, power MOSFET-gating methods.**

I. Introduction

POWER metal oxide semiconductor field effect transistors (MOSFETs) have gained wide acceptance in a number of applications, including power supplies, variable speed motor drives, and a host of other systems. MOSFETs process power at what is often considered to be the lower power ranges. Their speed, turn-off capability, cost, and voltage-based gating have led to their popularity. However, these devices have definite limits on the voltage that they can support. Higher voltage ratings than presently available may not make the resulting devices as attractive as one might anticipate. For example, the on-resistance of the MOSFET is proportional to a factor greater than the square of the breakdown voltage. Current ratings are typically greater for n devices in series than for a single MOSFET rated at n times the breakdown voltage.

If one connects several devices in series and each device supports a share of the applied voltage, then the series string should be able to support more voltage than any single device could support alone. For example, assuming equal sharing of the applied voltage, a series string of N devices could support a voltage up to N times the voltage rating of any individual device in the string. Unfortunately, it is particularly difficult to obtain anything even close to an equal voltage sharing arrangement during switching transitions. Tiny delays in triggering or small variations in rise or fall times among devices can cause large inequities in how the applied voltage is shared.

Even when successful, such series connections require an individual gate-to-source triggering voltage for each MOSFET device. Transformers with multiple secondaries reduce the independent triggering voltage to a single supply, but transformers introduce time delay and economic penalties.

Recently, a reliable method of stacking power MOSFETs, placing them in series, was demonstrated [1], [2]. The operation of this circuit relies on a voltage division among the effective gate-source capacitance of the MOSFETs. This particular method was originally intended for high-speed turn-on switching of single pulses. Its original application was in the design of high-voltage pulse generators, dramatically improving the speed, power dissipation, and lifetime over the specialized vacuum tubes that have been employed in the design of such equipment well into the 1990s.

In this paper, the same method is modified to enable continuous switching of power MOSFET devices, not merely single pulse turn-on. This makes the method applicable to common power MOSFET applications. First, a review of existing methods is presented. Attendant advantages and disadvantages are described. Second, the new method of coupling gate signals is introduced. A description of the circuit topology and an important variation follows. Third, the devices and the whole circuit are modeled in a conventional fashion. These models reveal a capacitive series circuit, on which a voltage division may be performed to gain appropriate triggering voltage levels on each gate. Fourth, design formulae and methods are derived to determine an appropriate gate capacitance for each MOSFET in the series string. Fifth, using simulation program with integrated circuit emphasis (SPICE), the system is simulated and dynamic and static voltage sharing is predicted. Sixth, experimental results verify the switching of the series MOSFET string and show appropriate voltage sharing across the devices. Seventh and finally, applicability of this method to triggering IGBT devices is discussed.

II. Connecting Power Mosfets in Series

Existing methods for series connection of semiconductor devices fall into two categories [3]. A category described as load-side voltage balancing includes methods based on impedance-symmetrization [4], clamp circuits, active/lossless snubber circuits [5], [14], and passive snubber circuits [3]. The other category, described as gate side voltage balancing, includes dV/dt and dI/dt control [6], active overvoltage protection by dynamic clamp circuits [7], high precision gate drive timing [8], cascaded synchronization [9], and time-delay compensation [3]. These methods have been applied to GTO-thyristors, BJTs, and MOSFETs. Gerster gives a bibliography of these methods in [3] and gives examples of

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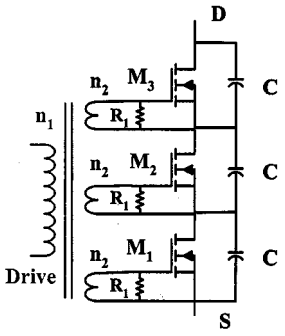

Fig. 1. Capacitor and diode network driving MOSFETs connected in series [10].

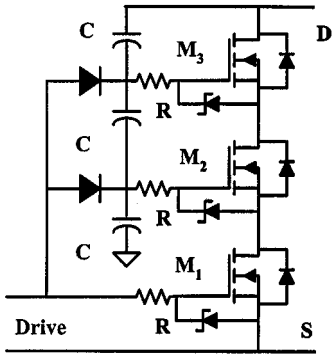

Fig. 2. Capacitor and diode network driving MOSFETs connected in series [10].

each dating from 1979 to 1990. As indicated by the references shown in the preceding paragraph, recent literature extends most of these methods, load-side and gate-side, to IGBTs.

Most load-side methods slow the dynamic voltage to achieve a better voltage sharing behavior. Unfortunately, slowed switching usually brings greater losses. Compactness of the power circuit can also suffer. Capacitive snubbers and resonant techniques applied to the load side can reduce the losses somewhat, but require more power components [5], [14]. Design techniques are the same as those employed to build a diverse range of snubbers [3].

Gate-side methods of driving power devices in series synchronize the pulses and compensate for the difference in switching time, optimize the driving circuit [10], or employ dynamic clamping [7], [8]. Transformer coupling of the gate signal is quite common for series-connected devices [11]. Using a dedicated transformer secondary for each device couples the gate drive signal and achieves the desired isolation. An alternative is to use a single secondary and separate drive circuitry for each device. Because the transformer can introduce unequal delays among secondaries, some form of synchronization, active or passive, often appears in the gate drive circuitry. For low frequency performance, some form of energy storage or memory circuit is often necessary. Gate-side methods may appear in the same circuit with load-side methods, improving the loss behavior and voltage distribution, static and dynamic, above what can be gained from either set of methods alone [10].

Timing circuits can be simple RC networks that are cheap, but have difficulty remaining accurate under normally varying circuit conditions [10]. They can also use sophisticated fast control methods to synchronize and shape the pulse and control or clamp the voltage output. These obtain a good degree of static and dynamic voltage balancing, but can add sensors and computation time [3], [8]. These methods tend to proliferate the parts on the gate side. These are not as expensive as power components, but they often do add up significantly.

A typical transformer coupling circuit for driving series devices is shown in Fig. 1. Its use is not restricted to MOSFETs [10]. An alternative to transformer coupling is capacitive coupling of the gate drive signal. A practical circuit for this purpose has been proposed specifically for MOSFETs and IGBTs, as shown in Fig. 2 [10]. The diodes couple the drive signal into the gates and the RC network is tuned to synchronize the gate signals. This circuit allows optimum voltage balance and claims to use less gate drive energy than the transformer-coupled topology [10]. However, its waveforms are still difficult to optimize and usually require additional circuitry to balance and synchronize the gate signals. For low frequency operation, a memory circuit may be necessary.

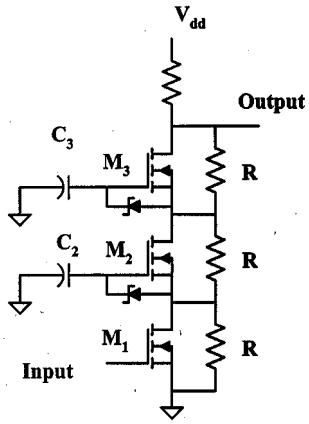

Fig. 3. Proposed topology for reliable operation of stacked power MOSFETs.

This paper introduces a new gate-side technique that takes advantage of the MOS device's internal capacitances to achieve synchronization of gate signals. This method has been shown to achieve extremely fast and balanced turn-on of MOS devices without additional load-side voltage balancing [1]. Its similarly fast turn-off does benefit from load-side techniques. This new method uses less than one additional small capacitor per switching device. A single gate drive source is required, sized to drive less than the sum of the gate currents. The speed keeps losses quite low, even when aided by load-side techniques.

III. New Method to Connect Power Mosfets in Series

A series stack of power MOSFETs may be created as shown in Fig. 3. The drain of a device is connected to the source of its neighbor. The load may be resistive or inductive. In this paper, a resistive load is assumed. Important aspects of this topology fall into three categories.

1) Adding one capacitor to the gate of each MOSFET, with one exception. The exception is the MOSFET nearest

the common ground, the device that has the single triggering source connected between its gate and the common ground.

2) Adding a resistive divider that stabilizes the voltage rise at turn-off. Such a resistive divider is a common fixture when connecting semiconductor devices in series, whether thyristors, MOSFETs, or others.
3) Including simple circuit protection for the MOSFETs. This design process is based on a model for gate charge transfer that is commonly accepted among many device manufacturers.

The switching behavior of power MOSFETs occurs in the cutoff, saturation, and linear regions of operation. In this paper, a common model for device behavior treats gate charge transfer differently in each of these three regions. For the analysis, the following three assumptions are made.

1) The drain current is zero when the MOSFET is in cutoff.
2) The drain current is given by the well-known $gm(V_{GS} - V_{th})$.; gm is transconductance; V_{GS} is the gate-source voltage; V_{th} is the threshold voltage.
3) The drain current in the linear region is $V_{DS}./R_{DS}(\text{on})$. V_{DS} is the drain-source voltage and $R_{DS}(\text{on})$ is the drain-source on-resistance [13].

The time between application of a drive signal and the drain current flowing is called the delay time. During the delay time, the MOSFET is in the cutoff region. When the current is between 10% and 90% of its final value, the MOSFET is in the saturation region. When the current is above 90% of its final value, the MOSFET is in the linear region.

Assuming the gate-source capacitance C_{gs} is much greater than the gate-drain capacitance C_{gd}, the charge Q_{g1} required to change from cutoff to saturation region is given in (1):

$$Q_{g1} = C_{gs}V_{th} \tag{1}$$

where V_{th} is the threshold voltage. In the saturation region, the drain-source voltage V_{ds} and the gate-source voltage V_{gs} influence the input capacitance C_{in}. C_{gd} may be assumed approximately constant. Therefore, when the MOSFET is in the saturation region, C_{in} is given in (2):

$$C_{\text{in}} = C_{gs} + C_{gd}(1 - \Delta V_{ds}/\Delta V_{gs}) \tag{2}$$

where the second term in the Miller capacitance. If V_{g2} is the value of V_{gs} when V_{ds} is 90% of its final value, then the charge Q_{g2} to traverse this region is given in (3):

$$Q_{g2} = C_{\text{in}}(V_{g2} - V_{th}) - Q_{g1} \tag{3}$$

C_{gd} has its maximum value $C_{gd\max}$ when the gate-drain voltage reaches its negative limit. For a driving voltage V_{gg}, the gate charge Q_{g3} necessary to traverse the upper 10% of the drain-source voltage rise is given approximately in (4):

$$Q_{g3} = V_{gg}(C_{gd\max} + C_{gs}) - Q_{g2}. \tag{4}$$

This piecewise model of gate charge transfer leads to new method for triggering MOSFETS for switching applications. The method, presented in the rest of this section of the paper, includes a design procedure for selecting the required components.

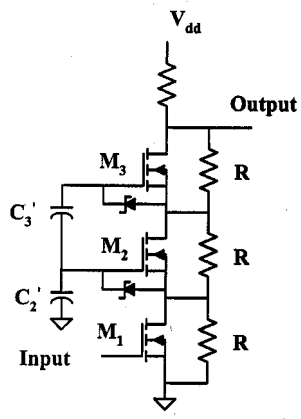

Fig. 4. Alternative topology for reliable operation of stacked power MOSFETs.

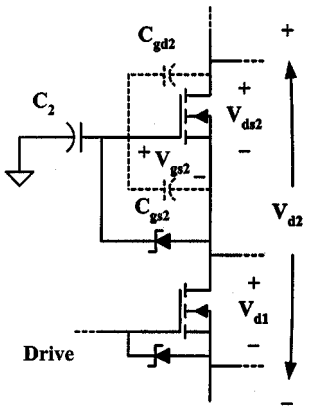

Fig. 5. Detail of series connection of power MOSFETs.

A. Inserting Capacitance into the Gate Circuit

As shown in Fig. 3, a capacitance is inserted between each gate and common ground. An alternative topology is to insert capacitance between adjacent gates, as shown in Fig. 4. Maintaining low equivalent series inductance (ESL) and equivalent series resistance (ESR) can be important to avoid distortion of the triggering voltage waveform.

Triggering the circuit is a matter of voltage division. Consider the proposed topology of Fig. 3, of which the lower portion is shown in more detail in Fig. 5. Let A_{V2} be defined as the ratio of ΔV_{d1}, the change of drain-source voltage across device M_1, to ΔV_{gs2}, the change of gate-source voltage on device M_2, as shown in (5). Let C'_{gs2} be the effective gate-source capacitance of M_2 as shown by (6). The second term in (6) approximates the Miller capacitance, assuming a large value of A_{V2}

$$A_{V2} = \frac{\Delta V_{d1}}{\Delta V_{gs2}} \tag{5}$$

$$C'_{gs2} = C_{gs2} + A_{V2} * C_{gd2}. \tag{6}$$

When device M_1 turns on, the voltage change on its drain, ΔV_{d1}, divides across C'_{gs2} the effective gate-source capacitance

of M_2, and the inserted capacitor C_2. This change in voltage ΔV_{gs2}, is given by (7)

$$\Delta V_{gs2} = \frac{\Delta V_{d1} C_2}{C_2 + C'_{gs2}}. \tag{7}$$

A similar equation may be written for M_3. However, in the latter case, the voltage ratio A_{V3} is the ratio of the voltage at the drain of M_2 to the change of gate-source voltage on device M_3. A reasonable division of the applied voltage V_{dd} among devices is to have an equal share across each device. Because ΔV_{d2} is twice ΔV_{d1} in that case, then $C_3 = 1/2C_2$. For longer strings of devices with equal sharing of V_{dd}, $C_4 = 1/3C_2$, or in general, the design formula is given in (8)

$$C_n = \frac{1}{(n-1)} C_2. \tag{8}$$

For power MOSFETs, $C_{gs} \approx C_{iss}$ and $C_{gd} \approx C_{rss}$, where C_{iss} is the input capacitance and C_{rss} is the reverse transfer capacitance. Most data sheets supply these values.

The alternative topology shown in Fig. 4 is a modification of the basic circuit of Fig. 3. The advantage of this alternative topology is that the gate capacitors may lend themselves to easier layout and assembly than for the basic circuit. The only difference between the topologies of the two circuits is the gate capacitor pattern. The output topology is identical in each case and, as before, equal output voltage sharing is desired. If it were possible to provide an identical gate-source voltage on each respective device in either topology, then the alternative topology would have the same output as the basic circuit.

By inspection, the top device in Fig. 4 must have the same gate capacitor voltage as the bottom device in Fig. 3. Both have the same gate-source voltage, the same gate-drain voltage, and sit atop a lower device with the same gate-drain voltage. Both must also have the same gate current to achieve identical behavior. Therefore, the top capacitor C'_3 in the alternative topology must have the same capacitance value as the bottom capacitor C_2 in the basic circuit. Restating this in (9)

$$C'_3 = C_2. \tag{9}$$

Due to the equal output voltage sharing and the identical gate-source voltage required at each device, each gate capacitor in the alternative topology must have the same terminal voltage. A gate current I should flow in each gate during turn-on. Therefore, I flows in the topmost capacitor, $2I$ in the next,…, and $(n-1)I$ in the bottom capacitor, for a series string of n devices. The topmost capacitor has value $C'_3 = C_2$, as determined already. To obtain an identical voltage across each of the remaining capacitors, the next capacitor must have a value of $2C_2$, $\cdots$, and the bottom capacitor must have a capacitance value of $(n-1)C_2$. In general, therefore, any gate capacitor Ci' may be found from (10)

$$C'_i = (n-i+1)C_2. \tag{10}$$

Because the gate capacitor voltages are identical and are in series, the alternative topology has a more relaxed specification on the working voltage of the capacitors.

B. Resistance

Appropriate resistance in parallel with the drain-source connections of each device maintains static voltage balance. To maintain the desired voltage division under blocking conditions, the current in each shunt resistor must be significantly greater than its respective device's leakage current. A resistance ladder such as this is a common element in most series combinations of semiconductor devices.

Adding a single capacitor across the entire resistance ladder can speed up the response time of the stack while turning off.

C. Circuit Protection

The breakdown voltage of the MOSFETs gate-source oxide is typically 20 V. This is significantly less than the output voltage values expected or intended in a series power MOSFET string. Transient overvoltages in excess of this may appear when switching. Inserting a resistor or a zener diode between gate and source are both common methods of mitigating this problem.

A zener diode sets a ceiling on the gate-source voltage and protects the device against such transient overvoltages between gate and source. This zener diode must be rated below the breakdown voltage of the MOSFET's gate-source oxide, but well above the voltage necessary to sustain conduction outside the MOSFET's active region. When designing capacitor values, the zener's capacitance must be added to the gate-source capacitance of the MOSFET.

A zener diode is also superior to a resistor for circuit protection because the zener diode draws only a negligible leakage current when operating below rated voltage. A resistor draws somewhat more current, more rapidly bleeding off the charge on the capacitor that sustains conduction. The zener diode should be rated to handle a brief inrush current at startup and at device turn-off. A fast diode in parallel with the zener diode can help solve this problem.

IV. System Simulation

Using SPICE, the system was simulated. International Rectifier provided a SPICE model for an IRF630, a common small power MOSFET. These simulations used Version 6.2 of the PSPICE software.

Values for C_{iss} and C_{rss} are 800 pF and 76 pF, respectively, based on data obtained from the data sheets published by International Rectifier. For 12 V gate-source voltage and a 100 V dc input voltage, distributed equally between three devices, A_v is 2.8 and the values of C_2 and C_3 should be 597 pF and 298 pF, respectively. The load is entirely resistive, in this case, a 20 Ω resistance. The resistance ladder has three 10 kΩ resistances to equalize the voltages at turn-off.

Several cycles of the voltage from the drain terminal to ground at each MOSFET is shown in Fig. 6. The upper trace is the M_3 drain voltage, the middle trace is the M_2 drain voltage and the lower trace is the M_1 drain voltage. The voltage is evenly distributed between devices for much of the cycle. At turn-off, there is a greater voltage stress on M_1, but only a few percent greater than on the other devices.

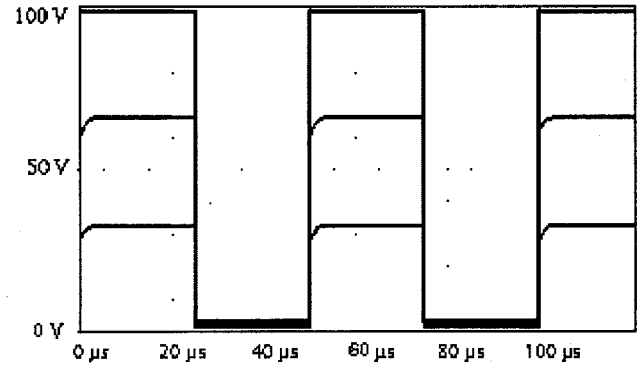

Fig. 6. Drain voltages of three series MOSFETs.

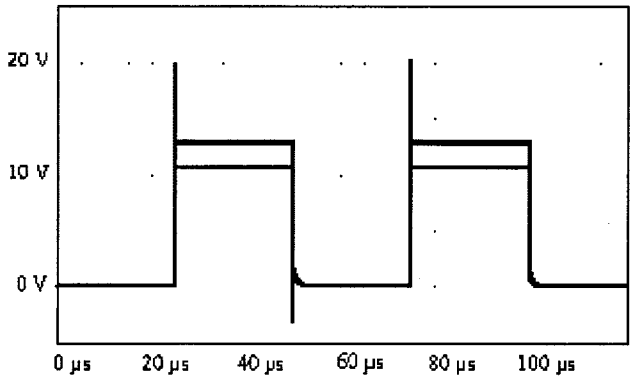

Fig. 7. Gate-source voltages of three series MOSFETs.

The gate-source voltages are shown in Fig. 7. The upper trace is that of device M_2 and the lower trace is that of device $M3$. The voltages are within the 20 V voltage limit. No zener diode was added to this simulation. There is a transient overvoltage at turn-on, indicating that a zener diode for circuit protection may be appropriate. There is also a transient at turn-off, indicating that a zener diode and a fast diode in parallel with it from source to gate may be appropriate as well.

Simulation was also performed for a series set of three IRF840 MOSFETs. Manufacturer's values for C_{iss} and C_{rss} are 1300 pF and 100 pF, respectively. For 20 V gate-source voltage and a 1500 V dc input voltage, distributed equally between three devices, A_v is 25 and the value of C_2 and C_3 should be 160 pF and 80 pF, respectively. The load is again a 20 Ω resistance.

Voltage waveforms were of the same form as those of the IRF630 over several cycles. Turn-on transient voltages are shown in Fig. 8. The five traces are referenced to common and are, from top to bottom: M_3 drain voltage, C_3 voltage, M_2 drain (M_3 source) voltage, C_2 voltage, and M_1 drain (M_2 source) voltage. The voltages fall in a manner that maintains a nearly equal sharing of the applied voltage.

An expansion of the time axis of the gate-source voltages at turn-on is shown in Fig. 9. The voltage that rises more quickly initially, but ends slightly lower, is the gate-source voltage of device M_2. There is a transient overvoltage predicted, giving

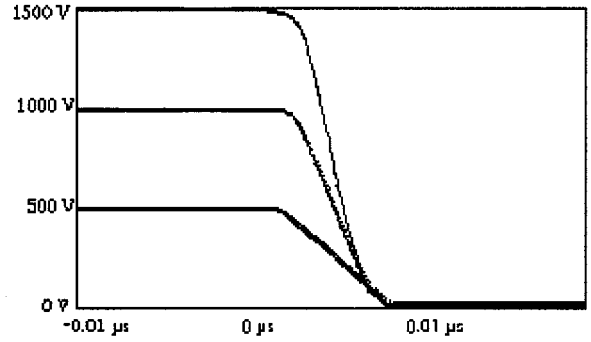

Fig. 8. Turn-on drain voltages of three series IRF840 MOSFETs.

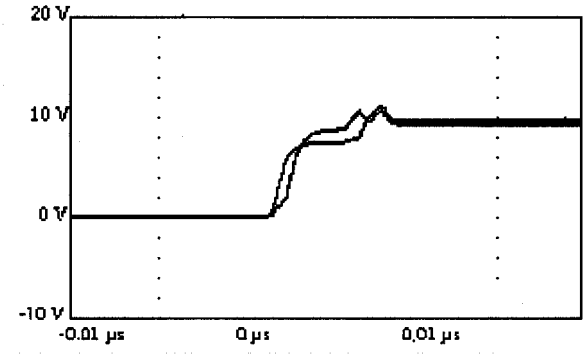

Fig. 9. Turn-on gate-source voltages of three series IRF840 MOSFETs.

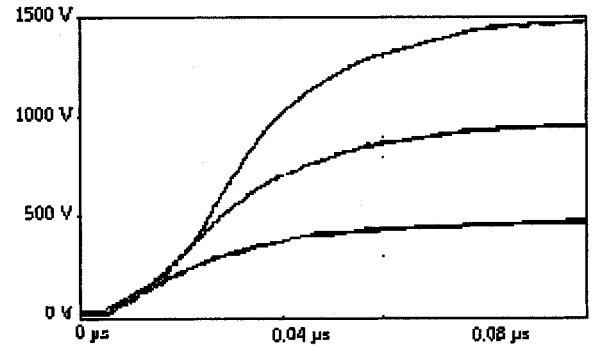

Fig. 10. Turn-off drain voltages of three series IRF840 MOSFETs.

credibility to using a zener diode. When a zener diode was added and the capacitance values were revised to compensate for the zener capacitance, this peak disappeared and the zener diode restricted the gate-source voltage appropriately.

Drain voltages at turn-off are expanded in time in Fig. 10. From top to bottom, voltages at the drains of M_3, M_2, and M_1, respectively. Voltage rise appears to be about equally distributed, keeping the individual device voltage stresses down to a reasonable share of the applied voltage.

Gate-source voltages during turn-on are shown in Fig. 11. The upper and lower traces are gate-source voltages for M_3 and M_2, respectively.

In PSPICE simulation, similar results have been found using manufacturer's models in simulation for the IRF644

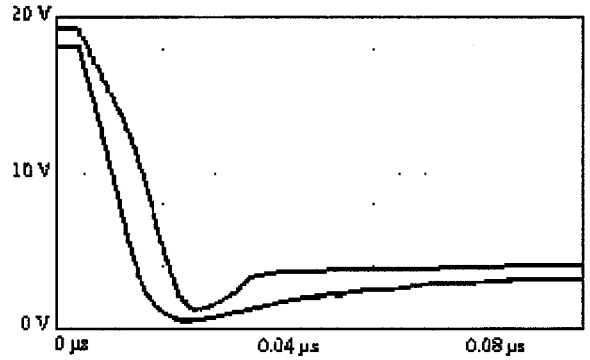

Fig. 11. Turn-off gate-source voltages of three series IRF840 MOSFETs.

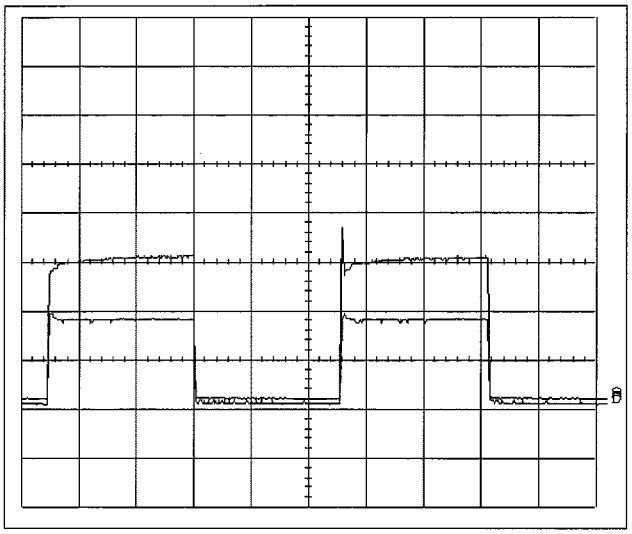

Fig. 12. Experimental results. Voltages at the drain terminals of $M2$ and $M1$. Scale: 20 V/div, 10 μs/div.

and IRFPE50 power MOSFETs. Simulations show reasonable turn-off and turn-on behavior. The devices switch together and in a manner that preserves voltage sharing. The gate-source voltages are of a reasonable magnitude and can sustain ordinary switching speeds for typical hard-switched loads indefinitely.

V. Experimental Results

Experimental verification of these results has been performed. A series stack of three IRF630 MOSFETs was connected as shown in Fig. 3. The capacitance values are $C2 = 600$ pF and $C3 = 290$ pF. Resistances $R = 9.8$ kΩ. Series load resistance is 20 Ω.

The results for repetitive switching are shown in Figs. 12 and 13. In Fig. 12, the voltages shown are the drain voltage at M_2 and the drain voltage at M_1, both referenced to common at the source terminal of M_1. The devices turn on and hold their respective conduction voltages, which are appropriate voltage values. At turn-off, the device voltages return to a reasonable sharing of the voltage. In Fig. 13, the voltages shown are the drain voltage at M_3 and the drain voltage at M_1. Comparison with Fig. 12 shows a reasonable sharing of the applied voltage.

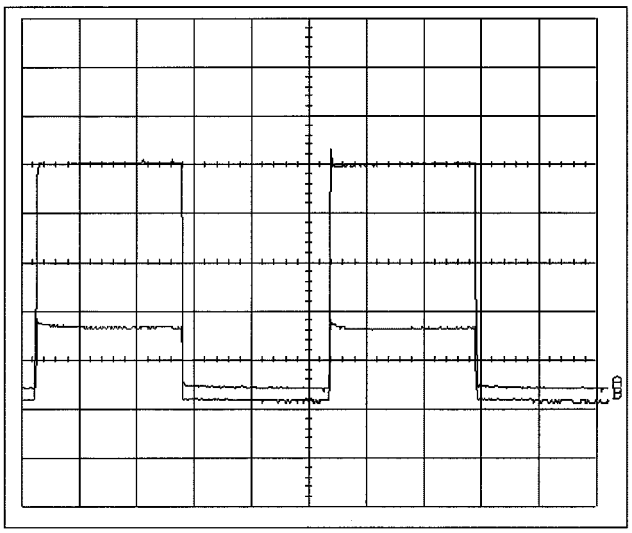

Fig. 13. Experimental results. Voltages at the drain terminals of $M3$ and $M1$. Scale: 20 V/div, 10 μs/div.

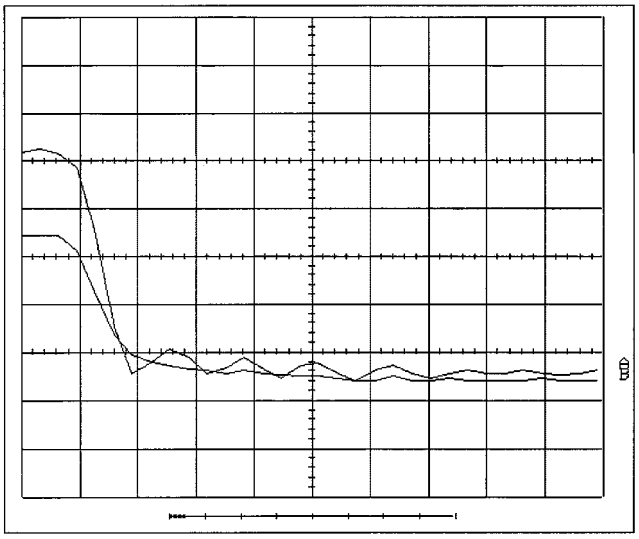

Fig. 14. Drain voltage waveform at turn-on at 100 V for IRF630 power MOSFET scale: 20 V/div, 31.25 ns/div.

Two turn-on transients are shown in Figs. 14 and 15. In Fig. 14, the turn-on transients for the drain voltage on M_2 and M_3 of the IRF630 circuit are shown. The devices turn on with a reasonable sharing of the voltage. In Fig. 15, the turn on transient for the drain voltage at M_3 of a series stack of IRF840 devices is shown. The IRF840 is a 500 V device. When the devices are off, the applied voltage across the stack of three devices is 1500 V. The devices performed without failure or damage, indicating a good sharing of the voltage during turn-on.

As simulated and then verified experimentally, the fall time is quite rapid, somewhat less than the nominal fall time for the devices at hand. As mentioned previously, a turn-off snubbing capacitor further decreases rise time.

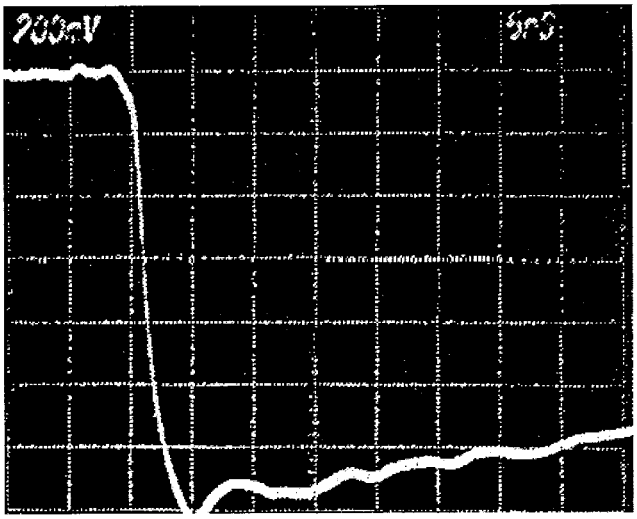

Fig. 15. Drain voltage waveform at turn-on at 1500 V for IRF840 power MOSFET scale: 200 V/div, 5 ns/div

Similar experimental results have been observed for the IRFPE50 power MOSFET.

From experimental and simulation results, it appears that voltage balancing behavior, static and dynamic, is as good as or, in most cases, superior to other methods as documented in the literature. This method appears to be faster than other methods without expensive control hardware or software. As a result, both experiment and simulation show switching losses at turn-on that are quite attractive and, due to aiding by a fast load-side method, are at least as attractive as those found in other load-side methods. Additional parts count is lower than other methods, particularly on the gate side, being less than a single small capacitor per switching device. A gate drive selected for this method must be capable of driving more than a single device, but all gate-side methods require that capability in some way. Charge on the capacitors does tend to bleed off, so care must be taken when planning to operate at low frequencies. Investigation continues into it behavior under load fault conditions.

VI. Application to IGBT Devices

An insulated gate bipolar transistor (IGBT) is also a MOS gated device. The method of transformerless gating presented in this paper applies to the IGBT as well. However, results are not quite as encouraging as those found for power MOSFETs.

Using the manufacturer's data sheets, appropriate capacitance values can be identified. Capacitor values for insertion at the appropriate gate terminals precedes in the same fashion as proposed in Section II-A of this paper. Simulation using simple SPICE models shows similar results at turn-on. However, the IGBT is a minority carrier device, requiring evacuation of the stored charge before turn-off, a mechanism unlike the majority carrier behavior of a MOSFET. Hence, each IGBT tends to turn off in sequence, rather than nearly simultaneously, as MOSFETs have been shown to do.

The practical effect of this is to restrict the turn-off behavior of the series-connected IGBT triggered by this method. Soft switching remains a valid option for turning off a series stack of IGBT devices, having been demonstrated by Wesenbeeck, *et al.* in 1995 [5], [14] and by Botto, *et al.*, in 1997 [12].

Low-voltage turn-off to any voltage is reasonable if that voltage is always less than the combined recovery time and voltage rating of the IGBTs in a series stack as they turn off in sequence from bottom to top. This is a slight improvement on the behavior of the silicon controlled rectifier (SCR), which requires zero current switching and a fairly long recovery time. Therefore, if a series string of IGBTs is connected and triggered as this paper recommends for MOSFETs, then the aggregate switching behavior is similar to an SCR, but having a somewhat greater overall peak voltage rating and much faster speed than an SCR.

A disadvantage of this method of triggering devices is the fact that the capacitor charge does bleed off, so the series stack cannot be kept in a conducting state indefinitely. For typical switching speeds and devices encountered in practice, this may not be a significant difficulty. Simulation and experimental results for a series stack of IGBTs will be presented in a future paper.

VII. Conclusions

A method to trigger MOSFETs and IGBTs without transformer coupling has been presented. The method is based on a voltage division across a series of capacitances, most of which are internal device capacitances. Design equations for the added capacitors have been derived. Simulation reveals that both static and dynamic voltage balancing for MOSFETs is achieved. Device stresses are within ratings. Simple circuit protection can be accommodated. Experimental results verify this method.

This method may be classed as a gate-side technique for voltage balancing. Voltage balancing behavior, static and dynamic, as good as or, in most cases, superior to other methods as documented in the literature. This method appears to be faster than other methods. As a result, switching losses at turn-on are quite attractive and, due to aiding by a fast load-side method, are at least as attractive as those found in other load-side methods. There is no additional expensive control hardware or software. On the gate side, additional parts count is lower than other methods, being less than a single small capacitor per switching device. There is no expensive isolation transformer and, hence, no additional balancing regulators to compensate for delay caused by transformer coupling. This method does require a gate drive capable of driving more than a single device, but that is common to all gate-side methods. Charge on the capacitors does tend to bleed off, so operation at low frequencies may be limited. Investigation continues into it behavior under load fault conditions.

The method applies to IGBTs, showing the same capabilities under turn-on conditions. However, the turn-off behavior is restricted, making a series string of IGBTs exhibit a switching behavior similar to an SCR, but with greater peak voltage capability and faster speed.

REFERENCES

[1] R. J. Baker and B. P. Johnson, "Stacking power MOSFETs for use in high speed instrumentation," *Rev. Sci. Instrum.*, vol. 63, pp. 5799–5801, Dec. 1992.

[2] ——, "Series operation of power MOSFETs for high speed high voltage switching applications," *Rev. Sci. Instrum.*, vol. 64, pp. 1655–1656, June 1993.

[3] C. Gerster, "Fast high-power/high-voltage switch using series-connected IGBTs with active gate-controlled voltage-balancing," in *Proc. 1994 Appl. Power Electron. Conf.*, Feb. 1994, pp. 469–472.

[4] R. Guidini, D. Chatroux, Y. Guyon, and D. Lafore, "Semiconductor power MOSFETs devices in series," in *Proc. 5th Euro. Conf. Power Electron. Applicat.*, Sept. 1993, pp. 425–430.

[5] M. P. N. van Wesenbeeck, J. B. Klaassens, U. von Stockhousen, A. M. de Morales Anciola, and S. S. Valtchev, "A multiple-switch high-voltage DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 44, no. 6, pp. 780–787, Dec. 1997.

[6] P. R. Palmer and A. N. Githiari, "The series connection of IGBTs with optimized voltage sharing in the switching transient," in *Proc. 1995 Power Electron. Specialists Conf. (PESC95)*, June 1995, pp. 44–49.

[7] S. Hong, V. Chitta, and D. A. Torrey, "Series connection of IGBTs (sic) with active voltage balancing," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 917–923, July/Aug. 1999.

[8] A. Consoli, S. Musumeci, G. Oriti, and A. Testa, "Active voltage balancement of series-connected IGBTs," in *Proc. 30th Ind. Applicat. Soc. Annu. Meeting*, Oct. 1995, pp. 2752–2758.

[9] J. Richardson and J. A. Nebert, "MOSFET-GTO cascode-connected power switch for high efficiency," in *Proc. 4th Int. Conf. Power Electron. Variable Speed Drives*, July 1990, pp. 411–416.

[10] R. Letor, "Series connection of MOSFET, bipolar and IGBT devices," in *SGS-Thomson Designers' Guide to Power Products*. New York: SGS-Thomson, 1994, pp. 759–769.

[11] J. M. Bourgeois, "An isolated gate drive for power MOSFETs and IGBTs," in *SGS-Thomson Discrete Devices Transistors Applications Notes*. New York: SGS-Thomson, Mar. 17, 2000.

[12] G. Botto, M. Carpita, E. Gilardi, and S. Tenconi, "Series connected soft switched IGBTs for high power, high voltage drives applications: Experimental results," in *Proc. Rec. 28th Annu. IEEE Power Electron. Specialists Conf.*, June 1997, pp. 3–7.

[13] R. J. Baker, "Applying power MOSFETs to the design of electronic and electro-optic instrumentation," Ph.D. dissertation, Univ. of Nevada, Reno, NV, 1993.

[14] M. P. N. van Wesenbeeck, J. B. Klaassens, U. von Stockhousen, A. M. de Morales Anciola, and S. S. Valtchev, "A multiple-switch high-voltage DC–DC converter," in *Proc. 17th Int. Telecommunications Energy Conf. (INTELEC)*, Oct. 1995, pp. 322–329.

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