

Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices

Herbert L. Hess
University of Idaho
Moscow, Idaho

R. Jacob Baker
University of Idaho
Boise, Idaho

Abstract—A reliable configuration for triggering a series string of power MOS devices without the use of transformer coupling is presented. A capacitor is inserted between the gate and ground of each MOSFET, except for the bottom MOSFET in the stack. Using a single input voltage signal to trigger the bottom MOSFET, a voltage division across the network of device capacitance and inserted capacitances triggers the entire series stack reliably. Design formulas are presented and simple circuit protection is discussed. Simulation shows reliable operation and experimental verification is presented. Application of the method is applied to series IGBTs.

ground. Second, the devices and the circuit are modeled in a conventional fashion. These models reveal a capacitive series circuit, on which a voltage division may be performed to gain appropriate triggering voltage levels on each gate. Design formulae are found for the gate capacitance. Third, using SPICE, the system is simulated and dynamic and static voltage sharing is predicted. Fourth, the method is applied to IGBTs, with desirable turn-on behavior, but significant limits on turn-off behavior. The final paper will contain experimental results for series connection of both MOSFETs and IGBTs.

I. INTRODUCTION

Power MOSFETs have gained wide acceptance in a number of applications, including power supplies, variable speed motor drives, and a host of other systems that process power at what is considered to be the lower power ranges. Their speed, turn-off capability, cost, and voltage-based gating have led to their popularity. However, these devices have definite limits on the voltage that they can support. Attempts to increase that voltage limit by series connection of devices is rare because it is difficult to trigger the devices close enough to simultaneously so that each supports its share of the applied voltage.

Recently, a reliable method of stacking power MOSFETs, placing them in series, was demonstrated.[1,2] The operation of this circuit relies on a voltage division among the effective gate-source capacitance of the MOSFETs. This particular method originally applied only to high-speed turn-on switching of single pulses. Its application was in the design of high-voltage pulse generators, dramatically improving the speed, power dissipation, and lifetime over the specialized vacuum tubes that have been employed in the design of such equipment well into the mid-1990s.

In this paper, the same method is modified to enable continuous switching of power MOSFET devices, not merely single pulse turn-on. This makes the method applicable to common power MOSFET applications. First, a description of the circuit is presented, with capacitors connected from common ground to the gate of each MOSFET device, except the one nearest the common

II. SERIES CONNECTION OF POWER MOSFET DEVICES

A series stack of power MOSFETs may be created as shown in Figure 1. The drain of a device is connected to the source of its neighbor. The load may be resistive or inductive. Appropriate resistance in parallel with the drain-source connections of each device maintains static voltage balance: under blocking conditions, the current in each shunt resistor must be significantly greater than its respective device's leakage current.

Capacitance is placed between each gate and common. These need not be single capacitors, but may be series-parallel combinations to achieve capacitance and voltage levels not available in any single device. The next section of this digest proposes design methods to determine these capacitance values.

A zener diode sets the gate-source voltage and protects the device against overvoltages between gate and source. This zener diode need be rated below the breakdown voltage of the MOSFET's gate-source oxide, typically 20V. It should also be able to handle a brief inrush current at startup and at device turn-off. A fast diode in parallel with the zener diode can solve this problem. Simulation presented later in this digest shows that this dynamic overvoltage protection is necessary. Also, the depletion capacitance of the zener diode is in parallel with its respective MOSFET's gate-source capacitance and, as such, adds to the latter, a fact important in the capacitor design.

III. DESIGN OF THE ADDED CAPACITANCE VALUES

When device M_1 , as shown in Figure 1, turns on, the voltage variation on its drain divides across the effective gate-source capacitance of M_2 , C'_{gs2} , and the capacitor C_2 . This change in voltage ΔV_{gs2} , is given by equation (1)

$$\Delta V_{gs2} = \frac{\Delta V_{d1} C_2}{C_2 + C'_{gs2}}$$

where C'_{gs2} is given by equation (2). The ratio A_{V2} is the ratio of the change of gate-source voltage to the change of drain-source voltage.

$$C'_{gs2} = C_{gs2} + A_{V2} * C_{gs2}$$

The design process is similar for M_3 , except that ΔV_{d2} is twice the value of ΔV_{d1} . In general, this gives a value for the nth capacitance C_n as $1/(n-1)*C_2$.

IV. SYSTEM SIMULATION USING SPICE

Using SPICE, the system was simulated. A model for an IRFPE500, a common small power MOSFET is selected. Values for C_2 and C_3 are 1300pF and 676pF, respectively, based on data readily obtained from the manufacturer's data sheets. These values are slightly different from those required for exactly equal gating voltages to show the effect of capacitance values on gate voltage. DC voltage is 150V. The load is resistive.

Several cycles of the voltage from the drain terminal to ground at each MOSFET is shown in Figure 2. Voltage sharing is quite good in the simulation. Interaction between the balancing resistors and the added capacitors does have an effect on the rise time.

Gate to source voltages are shown in Figure 3. As expected, they are not equal by design. Each device does share the voltage. The zener diodes proposed earlier in this digest are definitely needed to prevent the gate to source voltages from exceeding the maximum allowable level of 20V.

Similar results in simulation and experimentally have been found at a load voltage of 1500V for the IRF840 rated at 500V.[1]

V. EXPERIMENTAL VERIFICATION

Experimental verification of these results has been performed on an IRF630 MOSFET. Ratings are 200V and

8A. Drain voltages at two devices in a three-device stack are shown in Figure 4. Expanded views of the turn-off transient are shown in Figure 5. Further experimental verification will be presented in the paper.

V. APPLICATION TO IGBTs

This method applies to IGBTs because they are a MOS gated device. Using the model proposed by Hefner, a gate to emitter capacitance can be identified. Adding capacitances in the same manner yields similar simulation results. However, the IGBT is a minority carrier device, requiring evacuation of the stored charge before turn-off, a mechanism unlike that observed in a MOSFET. Hence, each IGBT turns off in sequence, rather than nearly simultaneously, as MOSFETs do. Simulation verifies this, making the IGBT less desirable for series connection. However, the practical effect is to restrict application of the series-connected IGBT triggered by this method to zero-current switching. This, in effect, makes a series string of IGBTs behave as an SCR, but having somewhat greater peak voltage rating and being somewhat faster than even inverter grade SCRs. (Botto et. al. recently proposed zero voltage switching of series-connected IGBTs.[3]). Simulation and experimental results of series IGBT switching will be presented in the paper.

VI. CONCLUSIONS

In the proposed paper, a method to trigger MOSFETs and IGBTs without transformer coupling will be presented. The method is based on a voltage division across a series of capacitances, most of which are inherent device capacitances. Design equations for the added capacitors are simple. Simulation reveals that both static and dynamic voltage balancing for MOSFETs is achieved. The method is less effective for IGBTs, but still applies to turn-on conditions, making a series string of IGBTs behave in switching in a manner similar to an SCR, but with greater peak voltage capability and faster speed than an SCR. Experimental results will be presented in the paper.

REFERENCES

- [1] R.J. Baker and B.P. Johnson, "Stacking Power MOSFETs for use in High Speed Instrumentation," Review of Scientific Instruments, 63, December 1992, pp. 5799-5801.
- [2] R.J. Baker and B.P. Johnson, "Series Operation of Power MOSFETs for High Speed High Voltage Switching Applications," Review of Scientific Instruments, 64, June, 1993, pp. 1655-1656.
- [3] G. Botto, M. Carpita, E. Gilardi, and S. Tenconi, "Series Connected Soft Switched IGBTs for High Power, High Voltage Drives Applications: Experimental Results," Record of the 28th Annual IEEE Power Electronics Specialists Conference, June 1997, pp. 3-7.

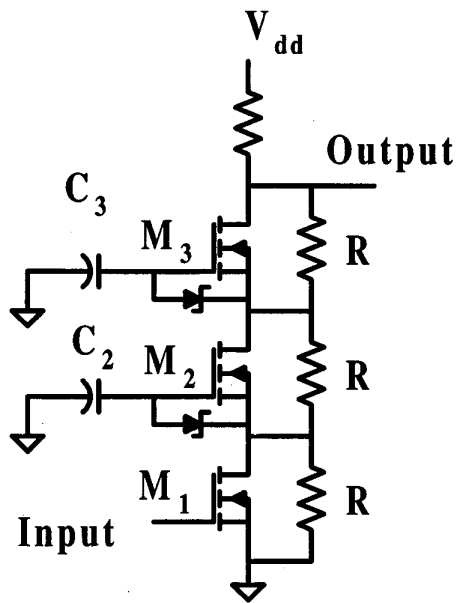


Fig 1. Series Connection of MOSFETs

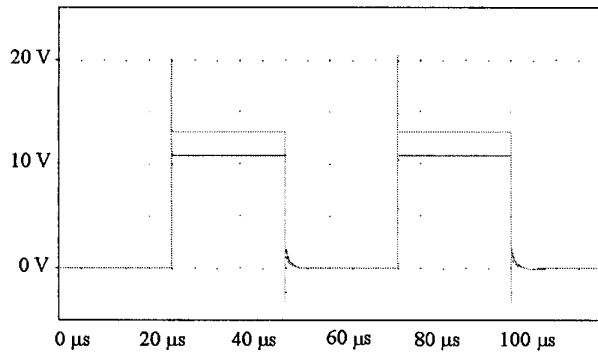


Fig 2. Simulation Results: Drain to Ground Voltages

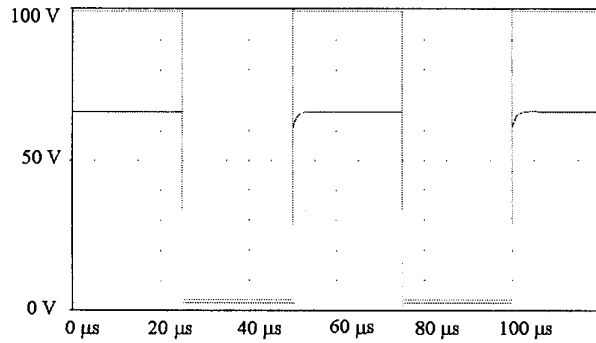


Fig 3. Simulation Results: Gate-Source Voltages

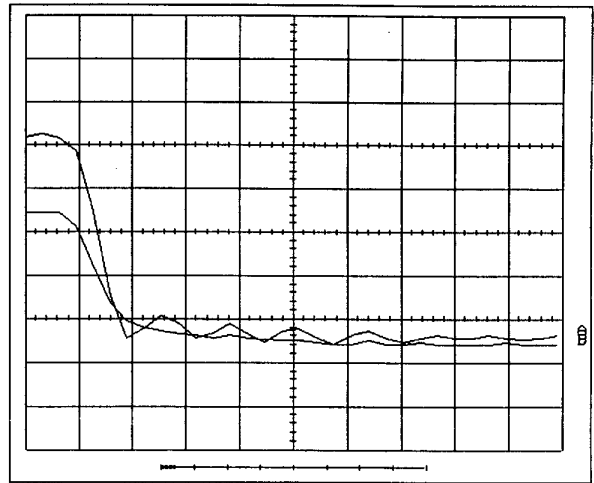


Figure 4. Experimental Results. Voltages at the Drain Terminals of M_3 and M_1 . Scale: 20V/div, 10 μ sec/div

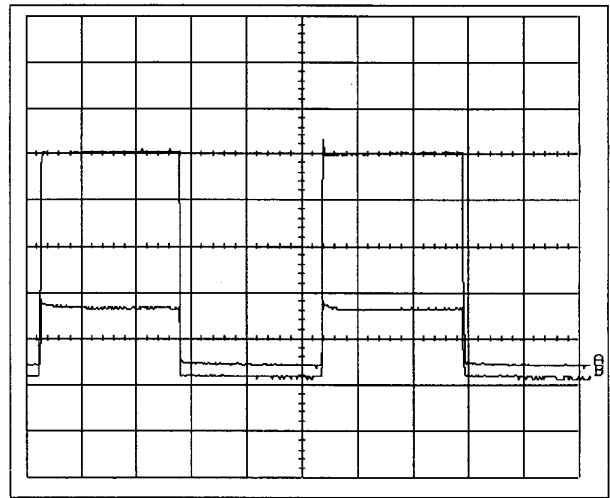


Figure 5. Drain Voltage Waveform at Turn-On at 100V for IRF630 power MOSFET Scale: 20V/div, 31.25ns/div