Midwest 98

Process and Temperature Performance of a CMOS Beta-Multiplier Voltage Reference

Song Liu and R. Jacob Baker
Microelectronics Research Center
The University of Idaho Center in Boise *
800 Park Blvd., Boise, Idaho, 83712
lsong@uiboise.engboi.uidaho.edu or jbaker@uidaho.edu

Abstract – The beta multiplier voltage reference (BMVR) is discussed as a direct replacement for the bandgap voltage reference in a CMOS process especially when substrate current is a concern. Performance of the BMVR with regard to temperature and process variations is covered. Experimental results from a 2-micron MOSIS test chip indicate that the BMVR can be tuned to within 10 mV of a desired value while maintaining a temperature coefficient below 1000 ppm/C and a supply sensitivity under 50mV/V.

I. Introduction

The beta-multiplier voltage reference (BMVR) can offer some important improvements over traditional bandgap circuits when implemented in a CMOS process. In an n-well CMOS process the bandgap voltage reference relies on the parasitic PNP transistor formed between a p+ implant in the n-well and the p-type substrate. Using this parasitic PNP transistor results in substrate current injection. In some applications, for example, DRAM, the substrate is pumped to a negative voltage. Using a bandgap voltage reference, with the resulting substrate current, causes the on-chip charge pump (the circuit pumping the substrate to a negative voltage value, e.g., VBB) to continuously run. The result is unwanted power dissipation. Another concern, when the substrate is pumped negative, is that the regulated value of VBB can affect the value of the voltage reference. In addition, parasitic PNP bipolars may not be characterized in a CMOS process. This adds to the difficulty of designing and fabricating a precision bandgap voltage reference. The beta-multiplier reference is an alternative approach which eliminates the use of bi-polar transistors, and therefore eliminates the substrate current injection.

II. Operation

The schematic of the beta multiplier in simplified form is shown in Fig.1. MOSFETs M3 and M4 are used to force the same current through each leg of the circuit. The size of MOSFET M2 is made larger than that of M1 (its transconductance parameter, beta, is larger than M1's) so that the difference in the gate to source voltage of M1 and M2 is dropped across R. When temperature increases, the voltage drop across R also increases because of the positive temperature coefficient of the resistor R and compensates the decrease of the gate-source voltage of M2 due to the negative temperature coefficient of its threshold voltage. A constant reference voltage can thus be maintained.

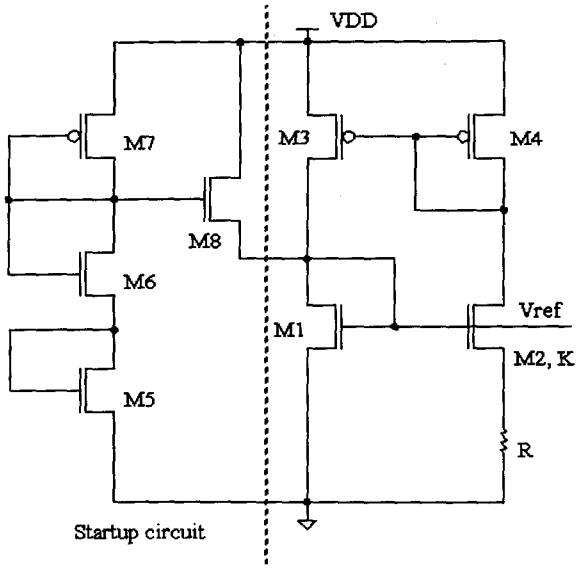

Figure 1 A beta-multiplier reference

Assuming $\beta_2 = K \cdot \beta_1$, we have the following equations (neglecting the output resistance of MOSFETs and the body effect of M2):

$$V_{GS1} = V_{GS2} + I \cdot R \quad (1)$$

$$V_{GS1} = \sqrt{\frac{2I}{\beta_1}} + V_{THN} \quad (2)$$

$$V_{GS2} = \sqrt{\frac{2I}{K \cdot \beta_1}} + V_{THN} \quad (3)$$

* *This work was supported by Micron Technology*

Solving for I and V_{REF} using the three equations yields

$$I = \frac{2}{R^2 \cdot \beta_1} \cdot \left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (4)$$

and

$$Vref = V_{GS1} = \frac{2}{R \cdot \beta_1} \cdot \left(1 - \frac{1}{\sqrt{K}}\right) + V_{THN} \quad (5)$$

The temperature coefficient of the voltage reference is given by:

$$\frac{dVref}{dT} = \frac{dV_{THN}}{dT} - \frac{2}{R\beta_1} \cdot \left(1 - \frac{1}{\sqrt{K}}\right) \cdot \left(\frac{1}{R} \cdot \frac{dR}{dT} + \frac{1}{KP(T)} \cdot \frac{dKP(T)}{dT}\right) \quad (6)$$

Equation (5) and (6) illustrate some important properties of the BMVR. First, according to equation 5, the reference voltage is independent of the power supply, VDD. In practice, the power supply dependence comes from the finite output resistance of the MOSFETs. Second, since with increasing temperature the resistance value increases while the threshold voltages and the transconductance parameter of the MOSFETs decrease, a temperature insensitive voltage reference can be designed. In a standard CMOS process, for example, the typical temperature coefficient of the threshold voltage, transconductance parameter and resistance of n+ resistor is –3000ppm/C, -1.5/T (T is in Kelvin) and 2000ppm/C, respectively. Plugging these process parameters into equation (6), we have the following equation (assuming $V_{THN} = 0.8V$):

$$\frac{dVref}{dT} = -\frac{2.4mV}{C} + \frac{2}{R\beta_1} \cdot \left(1 - \frac{1}{\sqrt{K}}\right) \cdot \left(-\frac{2000ppm}{C} + \frac{1.5}{T}\right) \quad (7)$$

At room temperature (300K) Equation (7) is equal to zero when:

$$\frac{2}{R\beta_1} \cdot \left(1 - \frac{1}{\sqrt{K}}\right) = 0.8 \quad (8)$$

If K = 4, we require that

$$R = \frac{1}{0.8 \cdot \beta_1} \quad (9)$$

In fact, equation (7) indicates that the temperature coefficient can also be set to positive or negative values by selecting the value of K, β_1 and R.

III. Stability

The beta-multiplier reference is an example of a circuit that uses positive feedback, and thus an analysis of the conditions of stability becomes necessary. Let's begin by supposing that the loop is broken at the gates of M1 and M2 (refer to Fig. 1). An input test voltage is applied to the gate of M2 and the returned voltage is taken at the drain/gate of M1. The feedback loop gain, A_{loop}, is the gain from gate of M2 to drain of M2 multiplied by the gain from gate of M3 to drain of M3:

$$A_{loop} = \left[-\frac{\frac{1}{g_{m4}}}{\left(\frac{1}{g_{m2}} + R\right)}\right] \cdot \left(-\frac{g_{m3}}{g_{m1}}\right) \quad (10)$$

where g_m is the forward transconductance of the MOSFETs ($g_m = \sqrt{2 \cdot \beta \cdot I_D}$, I_D is the drain current of MOSFETs).

Plugging equation (4) into equation (10), assuming the forward transconductances of M3 and M4, g_{m3} and g_{m4}, are equal and noticing $g_{m2} = \sqrt{K} \cdot g_{m1}$, yields,

$$A_{loop} = \frac{1}{2 - \sqrt{\frac{1}{K}}} \quad (11)$$

For stable operation of the circuit the feedback gain must be less than 1. This suggests that the size ratio of M2 and M1, K, should be greater than 1 to ensure the stability of the BMVR. Since this is always the case for BMVR (when K < =1, all the MOSFETs are turned off, and therefore BMVRs with K equal or less than 1 are not useful), the BMVR is guaranteed stable from its structure (One concern, however, is the stray capacitance across R).

Another issue that deserves mention is that like all other self-biased circuits, the BMVR needs startup circuitry (MOSFET M5 –M8 in Fig. 1) to avoid working at the undesired operating point (zero current).

IV. Sensitivity to temperature, power supply and process variations

It is desirable to determine how the reference voltage of the BMVR is affected by changes in sheet resistance, power supply voltages, and MOSFET threshold voltages. Simulation results of an ideal BMVR using Orbit's CN20 process SPICE models with a reference voltage of 1.8 V at room temperature are shown below.

Figure 2 shows the simulated temperature behavior of the beta multiplier reference. The simulation results indicated that the temperature coefficient of the BMVR could be made well below 500 ppm/C.

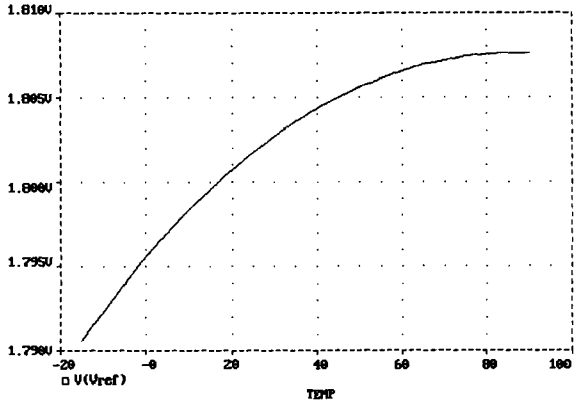

Figure 2 Simulated temperature behavior of the BMVR

Figure 3, as another simulation example, shows how the output voltage changes with the n+ resistor value and temperature. Here one of the problems of using beta-multiplier reference, namely a high reference voltage dependence on the sheet resistance (for the resistor used), is revealed. The V_{REF} dropped nearly 0.6V with R changing from 15K to 29K, which is within the possible sheet resistance variation range of a nominally 20K n+ resistors of CN20 process.

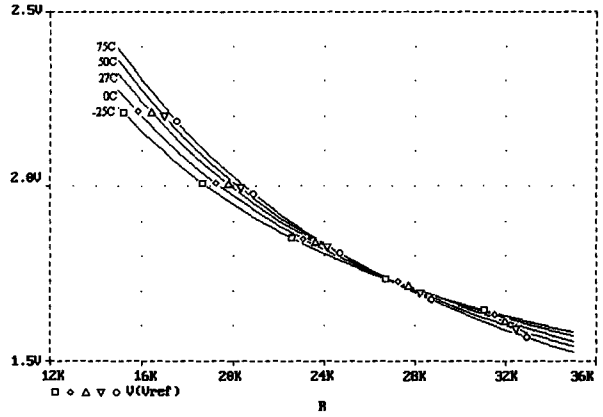

Figure 3 Simulated reference voltage dependence on R

Figure 4 shows how the reference voltage, in this self-biased configuration, is varied with changes in the power supply, VDD. The simulation results gave a power supply dependence of approximately 55mV/V.

The biggest drawback to using the beta multiplier reference, according to the simulation results, is the dependence of the output reference voltage on sheet resistance. The variation in MOSFET threshold voltage (and the MOSFET transconductance parameter, KP, although to a lesser degree) affect the voltage as well. Thus, precision voltages are more difficult to achieve than the bandgap reference. In any practical manufacturing environment the reference voltage must be adjusted on-chip. A precision voltage can be achieved by trimming the resistor value. The simulation results (see Fig. 3) indicate that a large variation in the sheet resistance and, indirectly, the MOSFETs' transconductance can be compensated for by proper design of a trimming circuit. While it is true that a bandgap reference cannot be fabricated to within 10 mV at room temperature without some on die adjustments, it is interesting to know how much on-chip adjusting can be expected if a beta multiplier is used. A summary of the experimental results from a test chip follows.

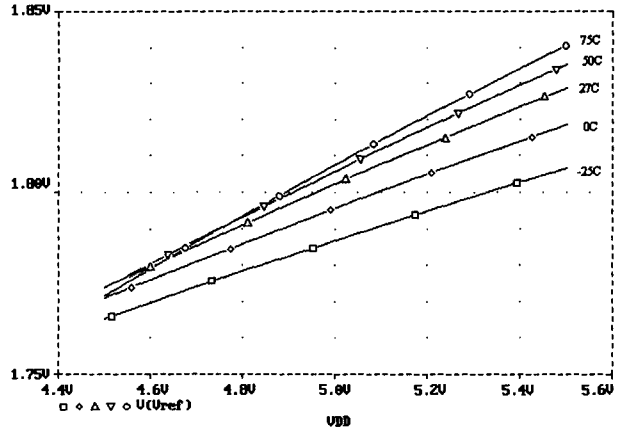

Figure 4 Simulated reference dependence on VDD

V. Experimental results

A test chip has been fabricated in a 2-micron n-well process with several test structures for investigating the tunability and manufacturability of the beta multiplier reference (Fig. 5).

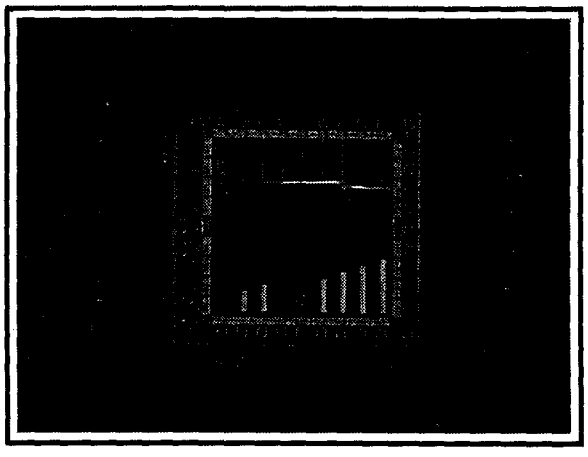

Figure 5 Photomicrograph of the test chip

Table 1 shows the measured reference voltage dependence on R at room temperature. The reference voltage has been tuned to all values from 1.75V to 1.85V, with a 10mV increment, by varying the value of

the resistor R. The experiment results indicated that the BMVR can be tuned to within 10mV of a desired value by selecting a proper value of resistance via an on-chip trimming circuit.

R (K)	Vref (V)
20.532	1.8503
20.762	1.8404
21.007	1.8301
21.231	1.8203
21.470	1.8103
21.727	1.8004
21.984	1.7902
22.235	1.7803
22.493	1.7701
22.753	1.7601
22.015	1.7503

Table 1 Tuning the reference voltage by varying the value of R

The temperature characteristics of the test BMVR were also measured and are shown in Figure 6. The measured temperature coefficient was 865 ppm/C, which was higher than the SPICE simulation showed (below 500ppm/C). However, this is still within a satisfactory level. The difference between the results of the SPICE simulation and the experiment was probably due to MOSFET and resistor temperature model limitations. The reference voltage is set to 1.81V at room temperature in the experiment.

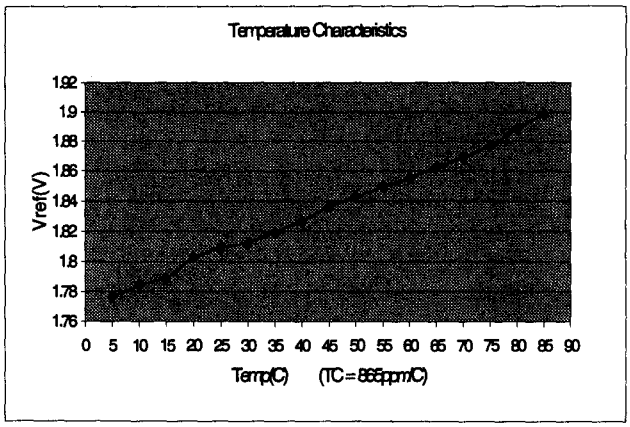

Figure 6 Measured temperature characteristics

Figure 7 shows the experimental results of the reference voltage dependence on VDD. The measured power supply dependence was 48.5mV/V.

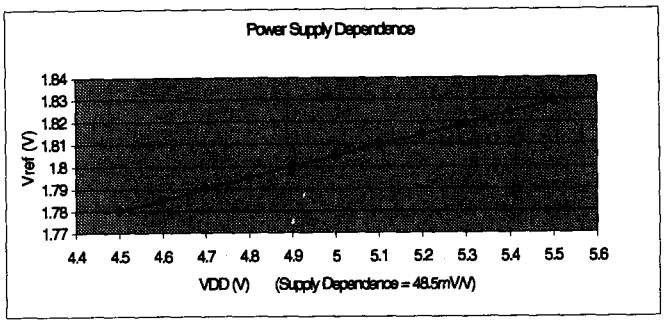

Figure 7 Measured power supply dependence

VI. Conclusions

It is suggested from both simulation and experiment results that beta-multiplier voltage reference can serve as a direct replacement for the bandgap voltage reference in a CMOS process in some less demanding applications such as needed sometimes in a PLL or data converters. Without substrate current injection, the biggest disadvantage of the bandgap references, the BMVR can be tuned to within 10mV of a designed value with a temperature coefficient below 1000ppm/C. The bandgap reference also needs trimming to achieve a precision voltage with a temperature coefficient around 500ppm/C. Furthermore, the high power supply dependence of BMVR can be improved by using more sophisticated structures (for example, cascoding the MOSFETs in Fig.1).

References

[1] R.Jacob Baker, Harry W. Li and Davis E. Boyce: *"CMOS Circuit Design, Layout, and Simulation"*, IEEE Press 1998.

[2] Hoi-Jun Yoo, Seung-Jun Lee, Jeong-Tae Kwon, Wi-Sik Min and Kye-Hwan Oh, *"A Precision CMOS Voltage Reference with Enhanced Stability for the Application to Advanced VLSI's"*, ISCAS 1993

[3] E.Vittoz and J. Fellrah, *"CMOS Analog Integrated Circuits Based on Weak Inversion Operation"*, IEEE Journal of Solid State Circuits, Vol. SC-12, No.3, June 1977, pp.224-231