Designing nanosecond high voltage pulse generators using power MOSFETs

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Power MOSFETs in series are used for generating high voltage, >1kV, pulses with nanosecond rise and fall times. The design procedures for series operation and driving power MOSFETs to attain nanosecond switching times are given. A −1500V pulse generator is designed with a 3ns falltime and a 15ns risetime into a 50Ω load.

Introduction: Traditionally, vacuum tubes such as the krytron, thyratron, or planar triode, have been used to create high voltage pulses with nanosecond rise and fall times. Modern power MOSFETs, with their unlimited lifetime, small physical size, and low on-resistance, offer an alternative method of designing high voltage pulse generation circuits. By operating power MOSFETs in series, their low breakdown limitation (1kV for commercially available MOSFETs) can be overcome. With proper driving circuitry, the troubling effects of the source lead inductance can be lessened. This Letter describes circuit design techniques to circumvent these problems.

Series operation of power MOSFETs: Fig. 1 shows schematically how power MOSFETs can be operated in series. The DC biasing resistors, not shown, have been neglected. Prior to being triggered the DC drain-source voltages of the MOSFETs are equal, i.e. $V_{DS3} = V_{DS2} = V_{DS1}$. The gate-source voltage of each MOSFET is 0V.

When switching takes place the effective capacitance between the gate and source of each MOSFET is

$$C_{gseff} = C_{gs} + \frac{dV_d}{dV_g} \cdot C_{gd}$$

The drain-source capacitance has been neglected. Capacitors C_2 and C_3, shown in Fig. 1, are used to charge *the* C_{gseff} of MOSFETs $M2$ and $M3$, respectively, during switching. Initially the charge on C_2 is

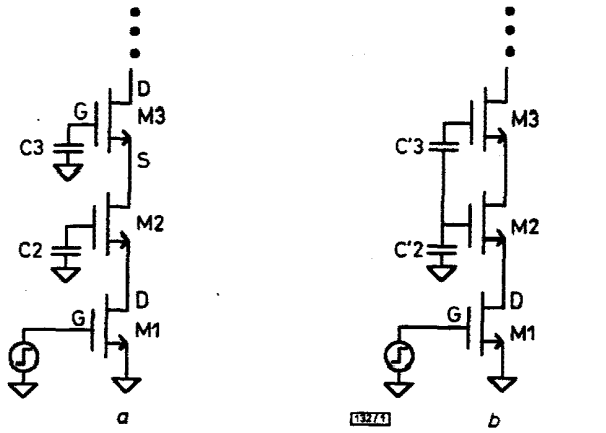

Fig. 1 *Simplified schematic diagram for series operation of power MOSFETs and alternative method for series operation of power MOSFETs*

a Series operation of power MOSFETs
b Alternative method

$$Q = C_2 \cdot V_{DS} \quad (1)$$

This assumes that all drain source voltages are the same prior to switching. After switching takes place, assuming 20V across the gate-source terminals; this charge is distributed between C_{gseff} and C_2, i.e.

$$Q = C_2 \cdot 20 + C_{gseff} \cdot 20 \quad (2)$$

Eqns. 1 and 2 may be combined and rewritten as

$$C_2 = \frac{C_{gseff} \cdot 20}{V_{DS} - 20} \quad (3)$$

Calculation of C_3 proceeds in a similar manner except that a charge $2 \cdot V_{DS} \cdot C_3$ is stored on C_3. C_3 is given by $C_3 = (C_{gseff} \cdot 20)/(2V_{DS} - 20) \simeq \frac{1}{2}C_2$ for $V_{DS} >> 20$V. If another MOSFET, $M4$, is

added in series then $C_4 \simeq \frac{1}{3} \cdot C_2$ or in general $C_n \simeq 1/(n-1) \cdot C_2$ for $n \geq 2$. These gate capacitors can be combined as shown in Fig. 1*b*, where C'_2 supplies charge to the gates of $M2$ and $M3$. This gives $C'_2 = 2 \cdot C_2$ and $C'_3 = C_2$ or in general $C'_n = (m-n+1) \cdot C_2$ where m is the total number of MOSFETs in series and n is the number of the MOSFET.

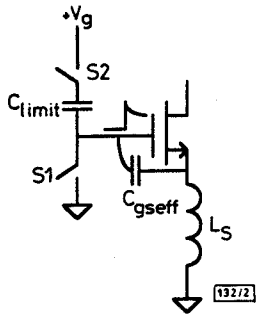

Fig. 2 *Simplified schematic diagram of gate driver circuitry*

Driving power MOSFETs: Fig. 2 shows the basic scheme for driving power MOSFETs. The unwanted source lead inductance is also shown. To prevent gate oxide damage, the gate-source potential should be limited to 20V. To illustrate the switching speed problem, consider a ideal 20V step voltage applied directly to the gate of $M1$. Initially all of this voltage is dropped across the source inductance. The rate of current rise is dV/dt = 20V/5nH or 4 A/ns for a 5 nH source inductance. Clearly this is a limitation if switching 30A in 3ns is desired. Use of the scheme shown in Fig. 2 will overcome the source inductance limitation while protecting the gate-source oxide. When the string of FETs are off, $S1$ is closed and $S2$ is open. When pulsed, $S1$ is opened and $S2$ is closed allowing V_G to be applied across C_{limit}, C_{gseff} and L_s. Initially all of V_G will be dropped across L_s. The current in the source lead inductance will be increasing at a rate of $di/dt = V_G/L_s$. The capacitance C_{limit} is selected to satisfy $20 = (V_G \cdot C_{limit})/(C_{limit} + C_{gseff})$. This is simply a capacitive voltage divider between C_{limit} and C_{gseff} which limits the gate source voltages after the effects of the source inductance die out. The gate voltage will rise substantially above 20V but the gate-source voltage will operate within the maufacturer's specifications.

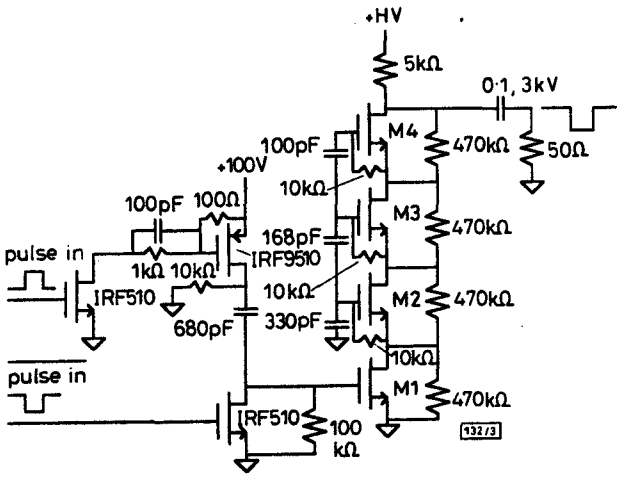

Fig. 3 *Schematic diagram of 1500 V pulse generator designed using the techniques presented*

$M1$–$M4$ are IRF740

Experimental results: A 1500V pulse generator was designed with the techniques given above to drive a 50Ω load with nanosecond risetimes and falltimes. Owing to their 400V drain-source voltage rating, four IRF740 MOSFETs were used. The schematic diagram of the pulse generator is shown in Fig. 3. The resulting output pulses are shown in Fig. 4. The falltime is ~3ns and the risetime is

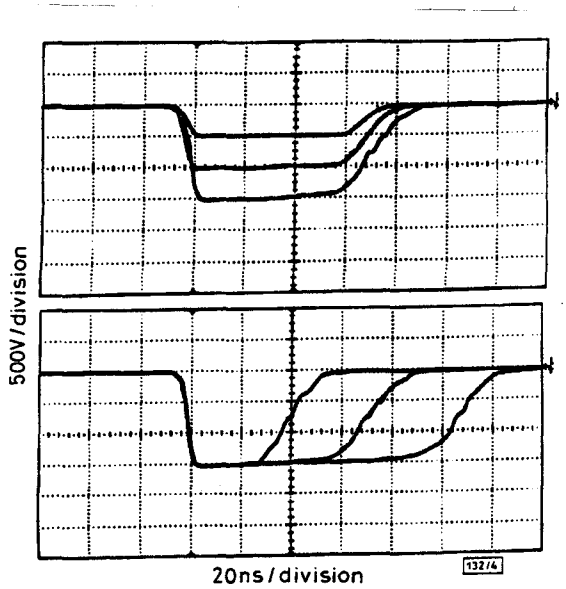

Fig. 4 *Output of pulse generator with varying amplitudes and pulse widths*

Conclusion: Design techniques were presented which allowed power MOSFETs to be used in series for higher voltage applications. Also presented was a power MOSFET driver circuit which overcame the switching speed problems associated with the source lead inductance. Pulses of this type should find uses in high energy physics, ultrafast optics such as gating microchannel plates and generating sweeps for streak cameras and in drivers for pulsed power applications.

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MCM layer assignment using genetic search

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A genetic algorithm for the MCM (multichip module) layer assignment problem is presented. A problem-specific genetic encoding scheme is used. Experimental results show that the proposed genetic algorithm consistently produced the same or better results than the simulated annealing algorithm and the best deterministic layer assignment algorithm known.

Introduction: A multichip module (MCM) is a multilayer electronic package. The top layer in a typical MCM is the chip layer on which bare dies are mounted. Below the chip layer are several pin redistribution layers whose purpose is to rearrange the signals from the pins of the dies into a uniform two dimensional grid pattern. Below the pin redistribution layer are several signal layers which are used for interchip signal routing. Each signal layer consists of two planes: x-plane and y-plane (Fig. 1*a*). Horizontal segments (x-segments) of a wire are routed on the x-plane and vertical segments (y-segments) are routed on the y-plane. x- and y-segments are connected by a via between the two planes. The objective of layer assignment is to assign each interconnection net to a signal layer such that no two net segments on a plane intersect each other. As the cost of fabricating an MCM and the cost