Stacking power MOSFETs for use in high speed instrumentation

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A reliable circuit configuration is described for stacking power metal–oxide semiconductor field effect transistors (MOSFETs). The resulting circuit has a hold off voltage N times larger than a single power MOSFET, where N is the number of power MOSFETs used. The capability to switch higher voltages and thus greater amounts of power, into a 50 Ω load, in approximately the same time as a single device is realized. Design considerations are presented for selecting a power MOSFET. Using the design method presented, a 1.4 kV pulse generator, into 50 Ω, with a 2 ns rise time and negligible jitter is designed.

I. INTRODUCTION

Power metal–oxide semiconductor field effect transistors (MOSFETs) have the potential to solve many problems in high speed, nanosecond and subnanosecond, instrumentation design.[1–4] The intrinsic speed of the commercial devices is limited mainly by packaging (lead inductances) and the combination of the drain, source and gate resistances, and the device junction capacitances. These factors limit device switching speed to approximately 500 ps depending to a large extent on packaging, device type, and circuit configuration.

To date, the main limitation of power MOSFETs in the design of instrumentation has been their hold off voltage (the maximum voltage which can safely be applied between the drain and source). This has resulted in examining power MOSFETs in stacks to acquire the cumulative voltage ratings required. Stacking power MOSFETs has been reported[1–3] for use in high speed instrumentation. These reported methods rely on driving each MOSFET individually whereas the method reported herein drives only the bottom MOSFET in the stack. Circuit part count is lower and board layout is simpler.

Currently 1 kV devices are available from several manufacturers with peak pulsed current ratings in the range of 20 A. If a 50 Ω load must be driven with greater than 1 kV, a lower voltage MOSFET with a higher peak current capability must be used in a stack configuration. This limitation in hold off voltage has forced applications requiring high voltage signals varying in the nanosecond region (such as sweep circuits for streak cameras[5,6] and gating of pockels cells[7] and microchannel plate image intensifers) to rely on avalanche transistor strings.[8]

To further understand the desirability of using power MOSFETs, consider the design of a streak camera ramp circuit. This circuit must provide a constant current to the streak tube deflection capacitance (typically 10 pF) over a range of 1.5 kV. A constant current charging a capacitance produces a linearly increasing voltage or in other words a ramp. Varying the current, and thus the ramp or sweep rate, is easily done with power MOSFETs by varying the gate-source voltage. On the other hand varying the ramp rate using Avalanche transistors requires major circuit modifications or else tolerating a highly nonlinear sweep. This is because the MOSFET can operate as a linear device while the avalanche transistor is inherently a nonlinear device.

II. STACKING POWER MOSFETs

Figure 1 shows a reliable method of stacking power MOSFETs. The resistor values are not critical and are used to set the dc operating voltages. The main cause of failure when stacking power MOSFETs is exceeding the maximum gate-source voltage specification of typically ±20 V resulting in a puncturing of the SiO_2 interface. The circuit shown in Fig. 1 relies on a voltage division between the effective gate source capacitances of M2 and M3 with C2 and C3 to stay below 20 V. A properly designed circuit will force all of the MOSFETs to turn on at the same rate.

When M1 turns ON the voltage change on its drain divides across the effective gate source capacitance of M2, C'_{gs2}, and the capacitor C2. The change in voltage between the gate and source of M2, ΔV_{gs2}, is given by

$$\Delta V_{gs2}=\Delta V_{d1}\cdot\frac{C2}{C2+C'_{gs2}}, \tag{1}$$

where C'_{gs2} is given by

$$C'_{gs2}\cong C_{gs2}+A_{V2}\cdot C_{gd2}. \tag{2}$$

The gain A_{V2} is determined by the ratio of the change in drain-source voltage to the gate-source voltage change. Similar equations may be written for M3 with the main difference being $V_{d2}=2V_{d1}$. This results in $C3\cong\frac{1}{2}C2$. If four MOSFETs are used then $C4\cong\frac{1}{3}C2$, or in general $Cn=[1/(n-1)]C2$. Most data sheets supply values for C_{iss}, C_{rss}, and C_{oss} and for power MOSFETs $C_{iss}\cong C_{gs}$ and $C_{rss}=C_{gd}$.

A zener diode or switching diode between the gate and source[4] of M2 and M3 can be used in place of a resistor. The cathode of the diode should be connected to the gate of the MOSFET. Also when calculating C'_{gs2} the diode capacitance will be added in Eq. (2). A diode between the gate and source has two advantages over the resistor. First, for wide pulses the resistor acts to shut the MOSFETs off by drawing a conduction current while the diode leakage cur-

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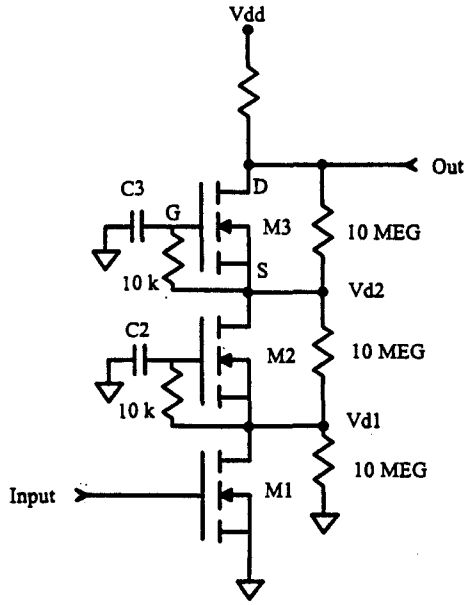

FIG. 1. Reliable method of stacking power MOSFETs.

rent is negligible. Second, a zener diode will protect the gate-source oxide from overvoltages.

III. AN EXAMPLE

Figure 2 shows a pulse generator designed around the method given above. The IRF840 has $C_{iss}=1300$ pF and $C_{rss}=50$ pF. Since the drain-source voltage of each MOSFET will change by 500 V while at the same time the gate-source voltage must not exceed 20 V, the voltage gain, Av, is approximately 25. The equivalent gate-source capacitance of M1, M2, or M3 is 2500 pF (1300 pF+25×50 pF). For amplifier or ramp design where swing linearity is important, 10 V is a better choice for the maximum V_{gs}. For V_{gs} larger than 10 V, the MOSFET will be in its linear region, or in other words the MOSFET will be ON.

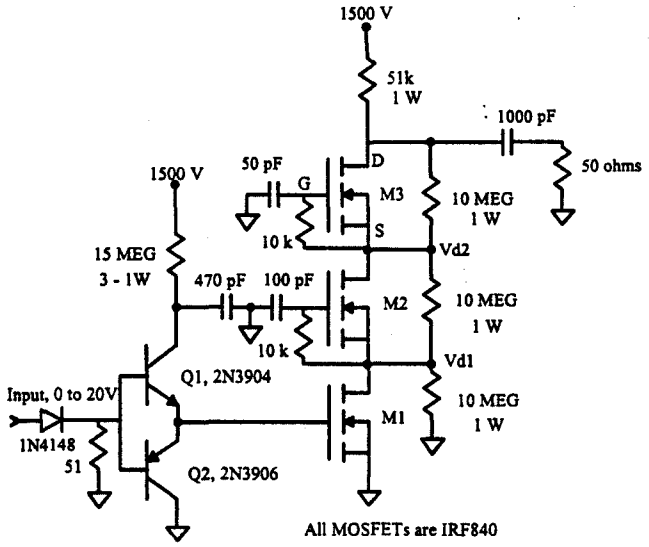

FIG. 2. Pulse generator using stacked MOSFETs.

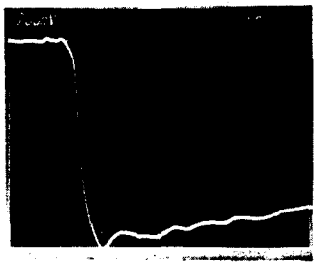

FIG. 3. Output of MOSFET pulser. 200 V/div and 5 ns/div.

Transistor Q1 is operated as an avalanche transistor[4,8] with breakdown voltage of 120 V. When Q1 is triggered by the input signal, 0 to 20 V, it dumps the charge on the 470 pF capacitor into the input capacitance of M1. If the input of M1 looks like a capacitor only, no lead inductances, a capacitive voltage divider exists between the 470 pF avalanche transistor capacitor and the 2500 pF input capacitance of M1. This voltage division limits the applied gate drive to 20 V. Adding the effects of the lead inductance can cause the gate potential to rise above 20 V. The driver compensates for the voltage induced by the lead inductances by increasing the voltage applied to the gate of M1. When the gate potential rises above 20 V Q2 turns on, after a delay long enough to charge M1's input capacitance, and pulls the gate back to 20 V.

The gate capacitors of M2 and M3 are 100 and 50 pF or $\frac{1}{25}$ 2500 and $\frac{1}{50}$ 2500 pF. The output of this pulse generator is shown in Fig. 3. The amplitude is 1400 V with a rise time of approximately 2 ns. There was no noticeable jitter. Several of these circuits were built with no MOSFET failures. The switching time of a single device was 2 ns approximately the same as the stack.

Another concern when stacking MOSFETs is maintaining the manufacturers specification on peak pulsed current. When selecting a power MOSFET, the peak current needed will determine the type of MOSFET used while the peak voltage needed will determine the number of devices. In the example given above, three IRF840s, with 500 V and 32 A ratings, provide the maximum number that may be used for a 50 Ω load.

IV. DISCUSSION

One of the benefits of using the circuit presented in this paper is the ease in which variable width pulses of several thousand volts may be generated. At the present time pulses of this nature use tubes such as the krytron or planar triode with a pulse forming line. A practical limitation in amplitude of 4 kV (80 A) exists with power MOSFETs currently available. Another benefit of the power MOSFET is its virtually unlimited lifetime when operated properly. This is very attractive when considering the limited lifetime of tubes that perform comparable functions.

Future work will involve developing sweep camera ramp circuits adjustable from subnanoseconds to hundreds of nanoseconds and a more universal MOSFET driver. The

MOSFET driver will combine commercially available MOSFET drivers, such as the MIC4420 18 V/6 A, with avalanche transistors.

ACKNOWLEDGMENT

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