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DESIGN NOTE

A 500 V nanosecond pulse generator using cascode-connected power MOSFETS

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Abstract. Cascode connection of power MOSFETs is described and used to generate variable width 500 V (10 A) pulses with 2 ns rise times and 8 ns fall times. The advantage this configuration has over a simple grounded source configuration is discussed. It is shown that, due to the large voltage swings over nanosecond time intervals and the large junction capacitances, care must be taken to protect the gate source SiO_2 interface from the resulting displacement currents. This protection is accomplished with the use of a diode clamp.

1. Introduction

Generating high-current (>5 A) and/or high-voltage (>200 V) pulses with nanosecond rise and fall times can be difficult. Instrumentation which uses these types of pulse can be found in electro-optics, radar, semiconductor testing and nuclear diagnostics to name a few. Power MOSFETs have mainly found use in power supply design [1] where nanosecond switching times are not needed. Recently their use in instrumentation for time-of-flight, coincidence and beam modulation experiments has been described [2, 3] and as a low repetition rate nanosecond switch [4]. Silicon controlled rectifiers and avalanche transistors have been used to generate these types of pulse [5, 6], but in general their performance falls short in one way or another of that obtainable with a properly designed power MOSFET circuit.

The main problem that is encountered when using a power MOSFET as a nanosecond switch, is charging and discharging the input capacitance. The IRF840, a typical commercially available power MOSFET, has an input capacitance of approximately 1200 pF. This capacitance, combined with the effective added capacitance due to the Miller effect, makes switching times of less than 10 ns difficult to achieve. Also, the high-voltage swings combined with the nanosecond switching intervals displace large currents through these capacitances which can destroy a poorly designed gate drive circuit.

2. Cascode connected power MOSFETs

Figure 1 shows a schematic diagram of a pulse generator using cascode-connected power MOSFETs M1 and M2.

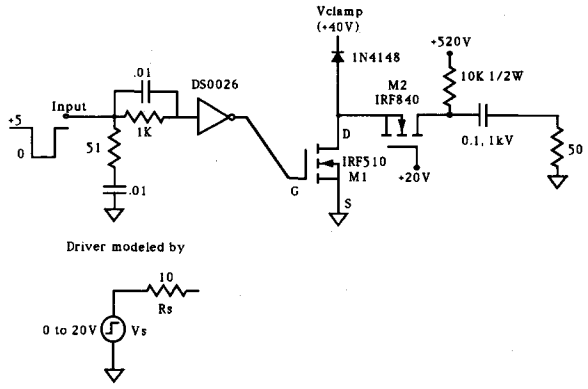

Figure 1. Pulse generator using cascode connection of power MOSFETs.

The output of this pulse generator into a 50 Ω load is shown in figures 2(*a*,*b*). The leading edge transition duration is 2 ns, while the trailing edge transition duration is 8 ns. A grounded source configuration using the IRF840 (alone), and the same driving circuit shown in figure 1, produced switching times of 18 ns and 65 ns for the leading and trailing edges respectively. The basic idea behind this cascode connection is to reduce the input capacitance which must be driven. This is accomplished by (1) using and driving a lower breakdown voltage FET, and thus lower input capacitance, and (2) eliminating the Miller effect.

The operation of the circuit is as follows. The driving source voltage, which is modelled by the 0–20 V step generator with 10 Ω source resistance, switches ON and starts charging the input capacitance of M1, approximately 200 pF, through R_s (=10 Ω). This causes the

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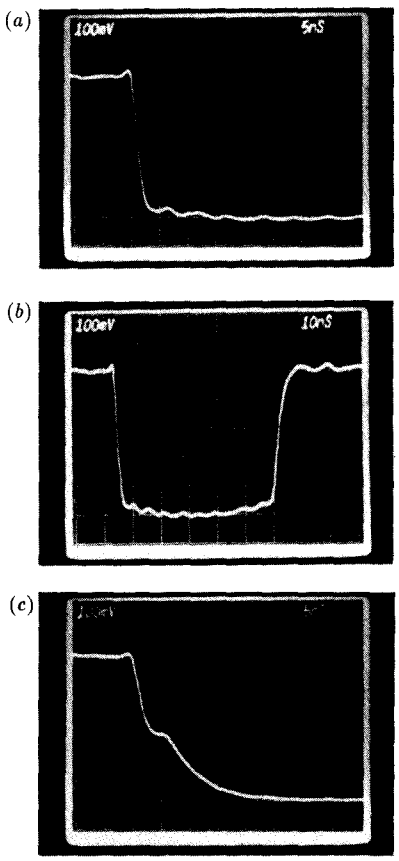

Figure 2. 100 V/div (2A/div). (a) Output of circuit in figure 1 showing leading edge, 5 ns/div. (b) Trailing edge, 10 ns/div. (c) Output with diode clamp tied to +20 V.

drain current of M1 to increase. If the drain potential of M1 is 40 V, M2 will start to turn ON a finite time after the drain current in M1 increases. Establishing a large drain current in M1 before M2 switches ON can be used to cause M2 to switch ON in a time limited approximately by the device's lead inductance. The cost for faster switching time is longer delay. The delay between M1 turning ON and M2 turning ON can be adjusted using V_{clamp}. Connecting the diode clamp to +20 V, that is to the gate of M2, gives an output as shown in figure 2(*c*).

The main cause of failure in power MOSFETs is perforation of the gate source silicon dioxide layer. This failure occurs when the gate source potential exceeds the manufacturer's specification (typically ±20 V). For the circuit shown in figure 1 the drain of M1 should always be at a potential of less than or equal to 40 V.

3. Switching analysis

Figure 3 shows an approximate circuit model for the circuit shown in figure 1. The transconductance is assumed linear for each MOSFET past its threshold voltage. The capacitances are nonlinear functions of applied voltage, but for this analysis will be assumed constant. The voltage on the drain of M2 after power is applied

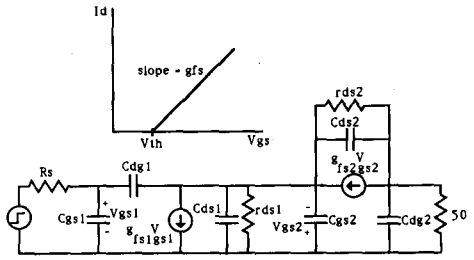

Figure 3. Model used to describe switching behaviour of the pulse generator shown in figure 1.

will be given, to first order, by the voltage division of r_{DS1} and r_{DS2}. If these two resistances are approximately the same, this voltage is limited by the breakdown voltage of M1, or approximately 100 V. In either case, the diode clamp is needed to protect the gate-source SiO_2 interface.

3.1. Switching from OFF to ON

The current flowing in the pair after switching takes place is 10 A (500 V/50 Ω). Establishing a drain current of 15 A, 1.5 times the final current value, in M1 before M2 switches ON will cause M2 to switch ON limited by it's lead inductance. This figure of 1.5 times the final drain current was determined through experimentation and simulation. MOSFET M2 starts to switch ON when it's gate-source voltage becomes greater than V_{th}, assumed in the following to be equal to 4 V, i.e. when the drain of M1 becomes less than 16 V.

To calculate the minimum value of clamping voltage, and thus delay needed to establish this 15 A of current, an expression for the drain-source voltage of M1, V_{d1}, is needed. First the gate-source voltage of M1 is given simply by

$$V_{gs1} = V_s\left[1 - \exp\left(\frac{-t}{R_s(C_{gs1} + 2C_{gd1})}\right)\right] V. \qquad (1)$$

For the IRF510, $C_{gs} + 2C_{gd}$ is approximately $C_{iss} =$ 200 pF, $R_S = 10\ \Omega$ and $V_s = 20$ V. The time it takes for V_{gs1} to get to V_{th} (4V) is approximately 0.5 ns. At a time 0.5 ns after the source driving voltage has switched on, I_{d1} starts to increase. Assuming $g_{fs1} = 2\ \Omega$ when $V_{gs} = I_D/g_{fs1} + V_{th} = 11.5$ V, the current flowing in M1 will be 15 A and the overall time that has passed will be 1.75 ns. At a time of 1.75 ns, V_{d1} should be greater than 16 V. The voltage on the drain of M1 at 1.75 ns is given by (assuming $C_{gs1} \gg C_{gd1}$ and $C_{gs2} \gg C_{ds1} + C_{ds2}$),

$$V_{d1} = V_{clamp} - \frac{1}{C_{gs2} + C_{gd1}} \int_{0.5n}^{1.75n} g_{fs1}(V_{gs1} - V_T)\,dt \qquad (2)$$

$$= V_{clamp} - 21.2\ \text{V} \qquad (3)$$

assuming $C_{gs2} + C_{gd1} = 1200$ pf. If $V_{clamp} > 37.2$ V, M2 will turn on when $I_{d1} > 15$ A.

3.2. Switching from ON to OFF

The rate at which current ceases to flow in the load is controlled by the load-output capacitance time constant, or $(50\ \Omega)(C_{dg2}+C_{ds2})$. The voltage change will be quick enough for the impedance of C_{ds2} and C_{gs2} to be small compared with r_{ds1} and r_{ds2}. In this case V_{d1} is given by

$$\frac{C_{ds2}}{C_{ds2}+C_{gs2}}500\ \text{V}.$$

Again the need for a diode clamp is apparent, for if C_{ds2} is one-tenth of C_{gs2}, V_{d1} will be greater than 40 V.

4. Conclusion

It was shown that a cascode connection of power MOSFETS could be used as a high-speed, high-power pulse generator as long as a protection diode was included to protect the SiO_2 gate-source interface. Nearly an order of magnitude improvement in transition times was observed when comparing the cascode and grounded source configurations. What were not discussed were the effects of lowering source driving impedance and shortening lead lengths to reduce series inductance, which can produce even better results.

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