Conf. paper

Step Response Considerations and the Design of a Suitable Step Generator for High Speed Digitizer Testing

R.J. Baker, E.G.&G. Energy Measurements, P.O. Box 1912, Mail Stop N-31, Las Vegas, Nevada 89125. (702) 295-2422.

J.J. Blair, E.G.&G. Energy Measurements, P.O. Box 1912, Mail Stop N-33, Las Vegas, Nevada 89125. (702) 295-2647.

Abstract - Step response testing is discussed and the design of a variable amplitude step generator is presented. A review of basic systems theory as applied to step response testing is given. This review is intended to set a basis for understanding the results of this type of testing. Transition duration, reconstruction, sampling frequency and aliasing are discussed as related to step response testing of digitizers.

The step generator performs the function of changing a sinusoidal input centered around ground into a rectangle waveform output with a first transition duration of 225 ps. The maximum repetition rate of this generator is >10MHz, while keeping leading edge jitter to <50ps. A discussion is given on integrating this step generator into a system for the characterization of digitizers with analog bandwidths in the range of 500 MHz.

I. Introduction

There are two types of tests which can be performed on digitizers; tests which determine the errors due to the quantization process, and tests which determine errors due to the finite bandwidth of the digitizer. If care is taken to avoid aliasing the digitizer may be thought of as a Linear Time Invariant(LTI), causal system. The purpose of this paper is to discuss step response testing[1] and in particular the design of a suitable step generator, while assuming the digitizer is an LTI, causal system. From the the step response of the digitizer the frequency response, amplitude and phase spectra, may be determined. An equivalent transfer function is determined by taking the derivative of the step response, which is the impulse response in the time domain, and taking the Fourier transform.

II. Step Response Testing

A valid question which may be asked is why use step response testing? Why not use a sine wave to determine the transfer function of the digitizer? The answer to this question is that using a sinewave will allow the determination of the amplitude response of the digitizer but not the phase response. This is due to not having the trigger signal and the signal generator tied in time to the digitizers internal clock. Without knowing the phase response the distortion introduced by the digitizer cannot be determined.

A. Distortionless transmission

Figure 1 shows an LTI, causal system with impulse response h(t) being excited by a signal x(t) and the corresponding response y(t). For distortionless transmission we require,

$$y(t) = K\,x(t - t_d). \qquad [1]$$

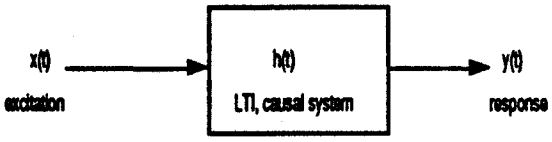

Figure 1 - Block diagram used for discussing distortionless transmission.

The constant K accounts for the change in amplitude and t_d for the time delay through the system, h(t). Taking the Fourier transform of both sides of equation [1] we get ,

$$Y(f) = K\,X(f)\,e^{-j2\pi f t_d}, \qquad [2]$$

where the time delay corresponds to a shift in phase in the frequency domain. The transfer function H(f), which is simply the Fourier transform of h(t), of this distortionless system is given by,

$$H(f) = \frac{Y(f)}{X(f)} = K\,e^{-j2\pi f t_d}. \qquad [3]$$

If we use Euler's identity, $e^{jx} = \cos x + j\sin x$, equation [3] may be written as,

$$H(f) = K\cos(-2\pi f t_d) + jK\sin(-2\pi f t_d). \qquad [4]$$

Equation [4] is in the form x + jy which has a magnitude and phase response given by:

$$\sqrt{x^2+y^2} \quad \text{and} \qquad [5]$$

$$\tan^{-1}\frac{y}{x} \qquad [6]$$

respectively. Knowing $\sqrt{\cos^2 x + \sin^2 x} = 1$ and $\tan^{-1}(\tan x) = x$, the magnitude and phase of equation [3] are given by

$$|H(f)| = K \qquad [7]$$

$$\Theta(f) = -2\pi t_d f \qquad [8]$$

The meanings of equations [7] and [8] are that in order for a system with transfer function H(f) to introduce no distortion into the signal of concern the amplitude response, $|H(f)|$, must be a constant for all frequencies of interest and the phase response, $\Theta(f)$, must be linearly decreasing with with increasing frequency. These relationships are shown in figure 2. Notice how the slope of the phase response is proportional to the time delay through the system. Often the phase response is drawn as a sawtooth waveform. This results from subtracting 2π from the phase whenever the phase becomes greater than 2π.

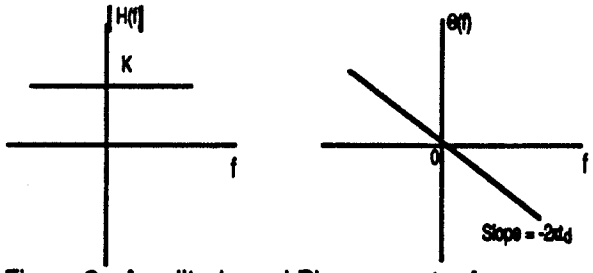

Figure 2 - Amplitude and Phase spectra for distortionless transmission.

B. Sampling and Aliasing

Sampling is the process of converting a continuous signal into a sequence of samples. These samples are a sequence of numbers which correspond to the value of the signal, say a voltage, at even intervals in time. The time between samples is called the sampling interval, T_s, while the frequency at which the samples are taken is called the sampling frequency, f_s. The sampling interval is related to the sampling frequency by,

$$T_s = \frac{1}{f_s}. \qquad [9]$$

Consider the unit step waveform, called u(t) with finite transition duration(risetime), shown in figure 3a. The Fourier transform of u(t), called U(f), is shown in figure 3b.

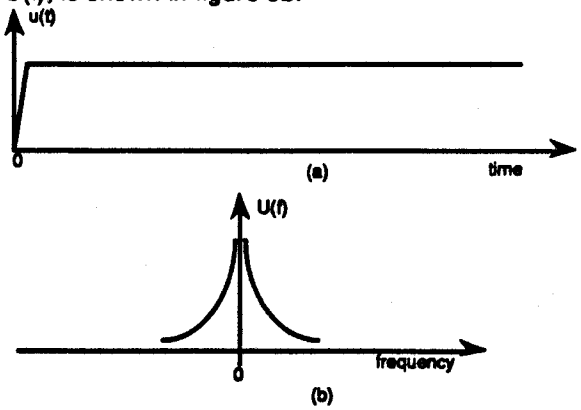

Figure 3 - (a) step waveform with finite transition duration and (b) the corresponding spectrum.

If u(t) is sampled at a frequency, f_s, then we can write the sampled result, $u_s(t)$, as a product of $u(nT_s)$, n an integer greater than or equal to zero, and the dirac delta function or;

$$u_s(t) = \sum_{n=0}^{\infty} u(nT_s)\delta(t - nT_s). \qquad [10]$$

The dirac delta function takes on a nonzero value only when its argument is zero. Therefore $u_s(t)$ is nonzero only at times which are integer multiples of the sampling interval.

It is interesting to note that equation [10] has a mathematical form similar to the Fourier transform of a periodic signal. In particular if $g_p(t)$ is periodic with period T_o, given by

$$g_p(t) = \sum_{m=-\infty}^{\infty} g(t - mT_o), \qquad [11]$$

then its Fourier transform is

$$G_p(f) = \frac{1}{T_o}\sum_{n=-\infty}^{\infty} G\left(\frac{n}{T_o}\right)\ \delta\left(f - \frac{n}{T_o}\right). \qquad [12]$$

The function g(t) is a truncated version of $g_p(t)$, that is g(t) equals $g_p(t)$ between zero and T_o and is zero elsewhere. This correspondence suggests

that we may determine the Fourier transform of $u_s(t)$ by using the duality property of the Fourier transform. The frequency spectrum of the sampled step is given by,

$$U_S(f) = f_S \sum_{m=-\infty}^{\infty} U(f - mf_S). \qquad [13]$$

Uniformly sampling this step signal results in a periodic spectrum with the period equal to the sampling rate. The spectrum of our sampled step waveform is shown in figure 4. The sampled spectrum is the sum of the original spectrums separated by the sampling frequency.

At this point we have neglected the effects of the finite bandwidth of the digitizer. To include these effects one would simply modify the original spectrum. The new spectrum of the overall response is given by,

$$U_r(f) = U_d(f)\, U(f), \qquad [14]$$

where $U_d(f)$ is the transfer function of the digitizer. The sampled spectrum taking into account the finite bandwidth of the digitizer is

$$U_{rS}(f) = f_S \sum_{m=-\infty}^{\infty} U_d(f - mf_S)U(f-mf_S). \quad [15]$$

This spectrum will be similar in shape to that shown in figure 4.

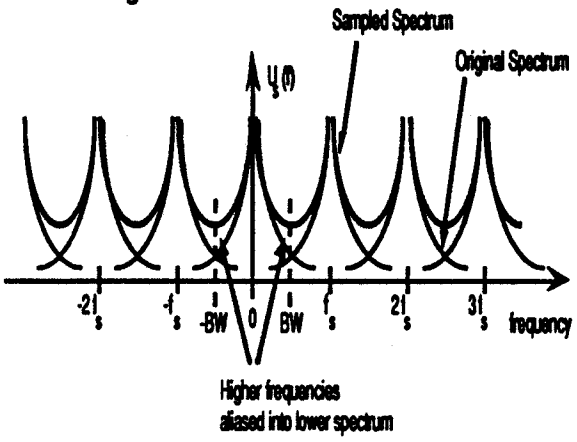

Figure 4 - Spectrum of the sampled step waveform

To reconstruct the signal we see that passing the sampled spectrum, figure 4, through a low pass filter, with bandwidth BW as shown in the figure, will remove the unwanted higher frequency components. Leaving approximately the original spectrum. There exists two problems with the reconstructing; 1) it is difficult to build a low pass filter with a sharp cutoff frequency while still maintaining linear phase, 2)if the Fourier transform of the signal is not negliigible at frequencies above the Nyquist frequency (one-half the sampling frequency), the periodic spectra will overlap resulting in aliasing.

The problem of low pass filtering can be solved by using a digital filter, that is filtering the data with the computer. The restriction of causality does not exist due to the data being stored in memory. This allows the design of an almost perfect filter to remove the unwanted frequency components in the stored data. What is more commonly done though, is to just assume a straight line between adjacent points. This is the simplest type of filter which can be applied to the data to eliminate the higher frequency components.

The problem of aliasing is not as easily solved. The frequency spectrum of the step waveform falls off as 1/f, so there is bound to be aliasing. The question is how much is acceptable?

Aliasing can be reduced by increasing the sampling frequency or limiting the frequency content of the sampled signal. Following the procedure given in [1] the sampling frequency may be increased by using a periodic rectangle waveform. The frequency of the waveform is selected to allow overlapping in time of the individual steps, see figure 1 in [1]. This results in multiplying the digitizers sampling frequency by the number of cycles in the waveform, this equivalent time sampling is similar to that used with sampling scopes.

Limiting the frequency content of the applied signal may be accomplished by limiting the transition duration of the applied step. The step must rise in less time than the equivalent rise of the digitizer, .35/3dB frequency, so as to allow determination of the digitizers frequency response beyond its 3 dB frequency. But, at the same time the transition duration must not be so short that a large amount of aliasing occurs in the resulting sampled signal.

III. Step Generator Design

Figure 5 shows a block diagram of the step generator used for step response testing. The input sinewave is applied to the comparator circuit which changes the signal into a square wave at ECL logic levels. This square wave is applied to the level shifting and MOSFET drive ciruit. The output of this circuit is a zero to fifteen volt square wave. This square wave is applied to the amplitude adjust and MOSFET switch circuit. When the MOSFET is turned "ON" the amplitude

selected is applied to the step-recovery diode circuit. The step-recovery diode circuit speeds up the leading edge, transition duration, of the step. A more detailed discussion follows.

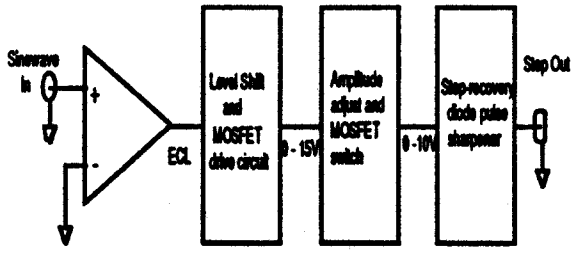

Figure 5 - Block diagram of step generator

A. Input comparator

When triggering on a sinewave in the frequency range of 100khz to 10Mhz it is very difficult to maintain low trigger jitter. If a 1V peak amplitude sine wave at 100 kHz is applied to the comparator, the slope of the signal as it is passing through zero is approximately 0.6 mV/ns. In order to obtain jitter less than 100 ps would require discriminating on a signal level of less than 60 μV. What makes the problem more difficult is the inability to observe the jitter with an oscilloscope. The oscilloscope triggering circuit has the same problem discriminating on such low level signals. Phase noise of the sinewave source and noise in and around the circuit make matters worse.

The circuit used as a comparator is shown in figure 6. The comparator, SP9685, is an ECL logic level output type which responds to a step overdrive in 2.2 ns typical. The gain of this comparator is 60 dB, or 1000. Because 60 μV will produce an output 60 mV, the gain must be increased. This is done by using positive feedback.

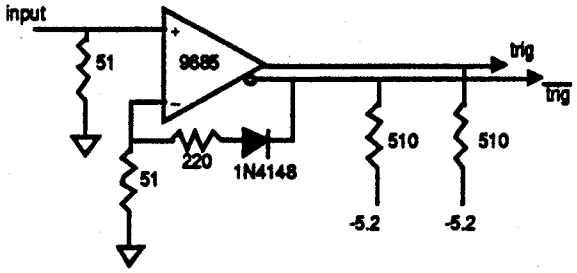

Figure 6 - Input comparator

Initially when $\overline{trig}$ is at -0.8 volts, corresponding to an ECL high, the voltage on the inverting input of the 9685 is (-0.8 + 0.7)51/(51 + 220) or -19 mV. If the input signal rises 10 μV above the voltage on the inverting input the $\overline{trig}$ output will fall by 10 mV. A portion of this change in voltage will appear at the inverting input causing the output to change again. This continues until $\overline{trig}$ reaches its low state, that is -1.6V, and is limited by the speed of the comparator. The voltage required to bring the comparator back into its original state is (-1.6 + 0.7)51/(51+220) or -170 mV. This circuit can also be called a Schmidt trigger because of the hysteresis required to change the state of the outputs. It should be mentioned that this analysis is somewhat ideal in that the finite propagation delay of the comparator has not been considered.

B. Level Shifting and MOSFET Drive Circuit

The next problem that one must solve is that of changing the ECL levels into a level that is suitable for turning a MOSFET "ON" and "OFF". This is accomplished with the circuit of figure 7.

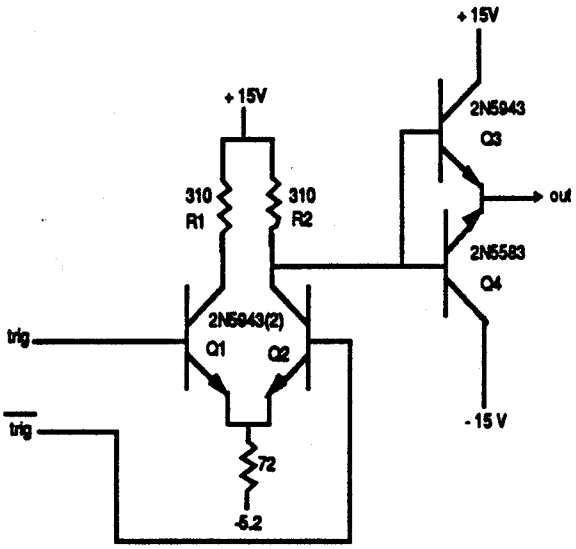

Figure 7 - Level shifting and MOSFET drive circuit

Transistors Q1 and Q2 form a differential pair which performs the function of changing the ECL waveform into a 0v to 15V waveform. The voltage at the emitters is -1.6V and the current flowing through the 72 ohm resistor is 50 mA. If the trig input is an ECL high, -0.8V, Transistor Q1 sources the 50 mA current while Q2 is off. The voltage on the collector of Q2 is approximately 15V and the output of the circuit is 14.3V, Q3 and Q4 form a push-pull amplifier effectively lowering the source impedance seen by the load. When trig is an ECL low, -1.6V, Q1 is off and Q2 is providing the 50 mA current. The voltage on the collector of Q2 is now 15 - 310(50 mA) or -0.5V. The output voltage is approximately zero. It should be noted that Q1 and Q2 never go into saturation. This avoids the problem of removing the excess stored charge in a saturated transistor. Also R1 has the effect of

lowering the 3dB frequency of the pair. It was included to lower the power dissipated by Q1.

C. Amplitude Adjust and MOSFET switch

The output of the level shifting and MOSFET drive circuit is connected to the circuit shown in figure 8.

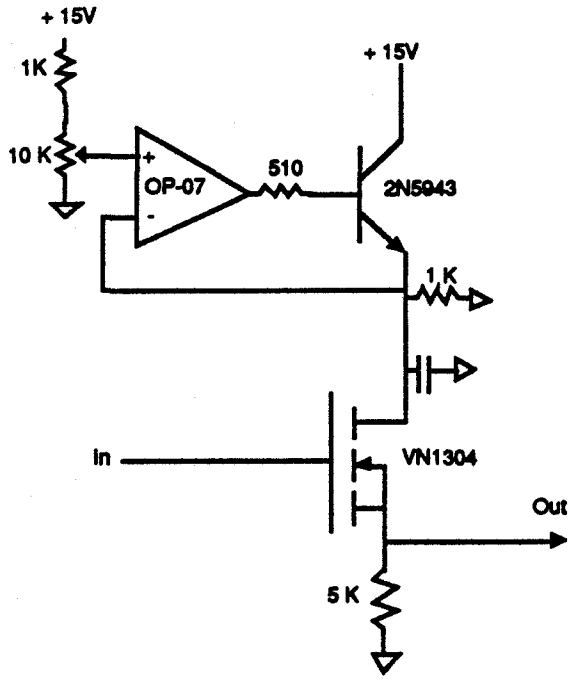

Figure 8 - Amplitude adjust and MOSFET switch

The op-amp is set up in a voltage follower configuration, setting the voltage on the drain of the MOSFET to whatever the voltage is on the non-inverting input of the op-amp. The amplitude of the output pulse is changed by adjusting the potentiometer and thus adjusting the voltage at the drain of the MOSFET. When the input voltage is 14V the MOSFET is fully conducting making the output voltage equal to the voltage at the drain minus the voltage dropped across the MOSFET. Because the input capacitance of the MOSFET is approximately 30 pF the source driving impedance must be on the order of a few ohms in order to attain nanosecond switching times. The purpose of the bipolar transistor is to provide current gain insuring that the output of the op-amp is always driving a relatively large impedance.

D. Step Recovery Diode Pulse Sharpener

Step Recovery Diodes(SRD) are commonly used for harmonic generation in microwave circuits. However, another use for these diodes is that of a pulse sharpener[2]. The SRD is basically a PIN diode with a low, <0.2 pF, reverse bias capacitance. All diodes exhibit a reverse recovery time made up of removing the stored junction charge and charging the junction capacitance. While the stored minority carriers are being removed the impedance of the diode is low, typically less than an ohm[2]. If a voltage greater than the forward drop of the SRD and of opposite polarity is applied to a forward biased SRD the reverse current in the diode will increase limited by the source impedance. The diode is basically shorting the output of the source until the stored junction charge is removed. When this charge is remove the voltage across the diode will change at a rate controlled by the source impedance SRD junction capacitance time constant. The SRD is said to have snapped when it changes from its low impedance state to its reverse biased high impedance state.

A schematic diagram of the SRD circuit is shown in figure 9.

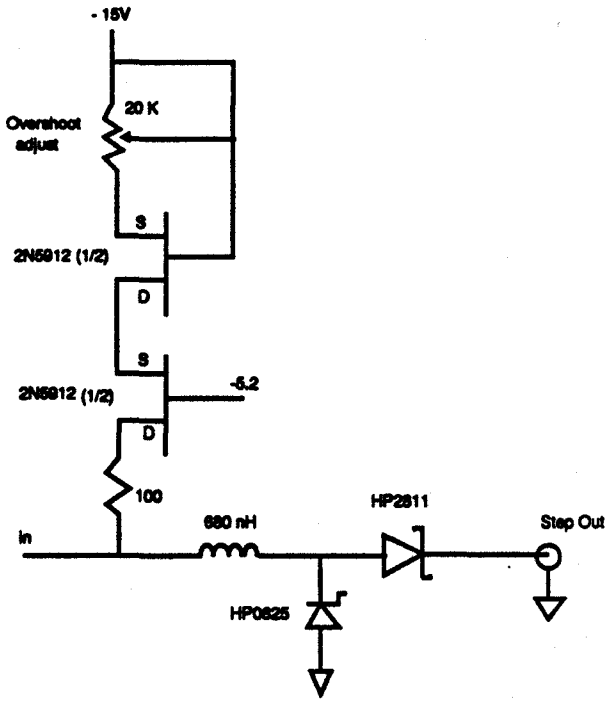

Figure 9 - Step Recovery Diode Pulse Sharpener

The JFETs form a high frequency current source which forward biases the SRD, HP0825, when there is no applied input voltage. The schottky diode is used to keep the -0.7 V offset of the SRD from appearing at the output of the generator. It also helps to eliminate the ramping voltage associated with removing the charge in the SRD junction while reverse biasing the diode. Using the

simplified schematic of Figure 10 the operation of the circuit can more readily be explained.

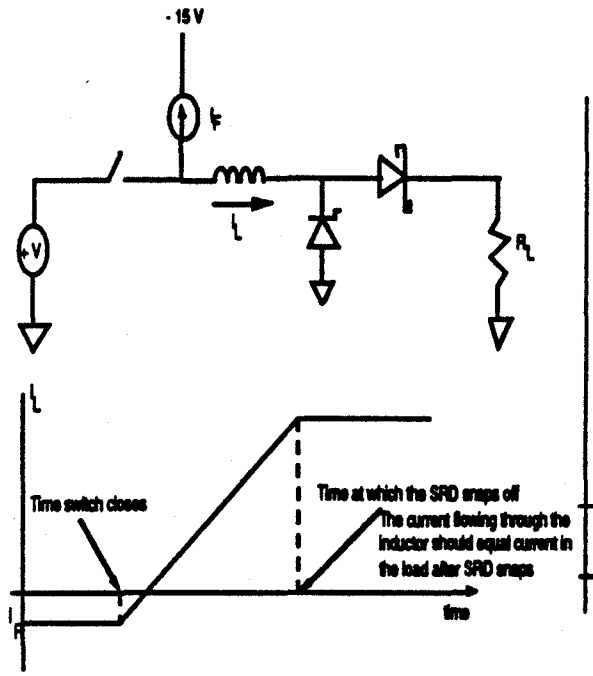

Figure 10 - Simplified schematic of SRD pulse sharpener.

Initially the SRD is forward biased and the switch is open. The current flowing through the diode and the inductor is I_F. The value of I_F determines the stored junction charge and thus when the SRD will snap to its high impedance state. When the switch closes the voltage V is applied to the inductor causing the current to increase linearly according to $V = Ldi/dt$. The current I_F is set so that the SRD will snap to its high impedance state when the current flowing through the inductor is V/R_L. This provides the flat top desired for step response testing. This method can also be thought of as changing a source impedance of Rs, Ls and Cs into a source impedance of inductance only. The inductor is large enough to swamp out the effects of the other components. The output of this step generator is shown in figure 11 displayed on a 20 GHz sampling system. The first transition duration is approximately 225 ps. The pulse settles to within 2% of its final value in less than 1 ns. The jitter is less than 50 ps with a 1 MHz input sinusoid. This was measured by triggering the sampling scope and delaying this triggered signal for display on this same scope. The first displayed edge will show the jitter of the sampling system while the second edge shows the jitter of the step.

The output of the step generator is adjustable from approximately 2V to 6V. To maintain an approximately 50 ohms output impedance a 10:1 attenuator was used on the output. When using the attenuator the output voltage is adjustable between 200 and 600 mV.

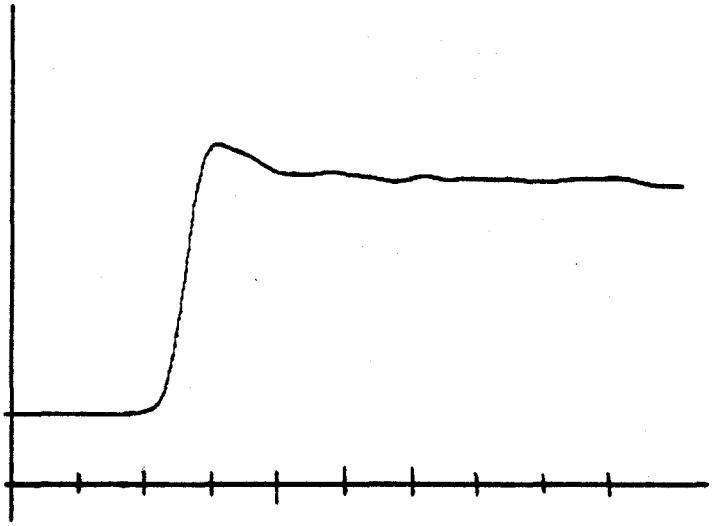

Figure 11 - Output of step generator,500 ps/div

IV. Experimental Results

The digitizer to be tested has a manufacturers bandwitdh specification of 500 Mhz and a sampling rate of 500 Msamples/s. The input step's transition duration was slowed to 350 ps using a risetime shaper. This was necessary to decrease the amount of aliasing, as was discussed in section II. Following the method used in [1], L=400 ns, D=8, frequency of the sinusoid is 1.2503907 MHz and at least 3500 sample points. The data shown in figure 12 was determined. These data were arrived at by deconvolving the input step from the recorded data and then taking the Fourier transform of the derivative of this step response. This part of our system is still in the developement stages so the data shown in figure 12 is not refined enough to be used for corrections. A time shift is applied to the recorded signal so that zero time corresponds to the 50% amplitude point on the step response. This subtracted time delay causes the slight negative delay shown by thephase shift curve. This time delay has no physical significance. We our concerned more with the linearity of the phase response rather than the time delay.

V. Conclusions

This paper has discussed the step response testing of high speed digitizers as well as the design of a step generator for use in a testing

system. One of the main points where step response testing of digitizers varies from oscilloscopes is transition duration. When testing an oscilloscope the shortest transition duration that one can get is desirable. But, because of the aliasing effect in digitizers, the transition duration of the step must be limited depending on equivalent sampling rate and the bandwidth of the digitizer under test.

VI. References

[1] T.M. Sounders, D.R. Flach, and J.J. Blair, "Step and Frequency Response Testing of Waveform Recorders," Proceedings of the IEEE IMTC/90, San Jose, California, Feb., 1990.

[2] "Pulse and Waveform Generation with Step Recovery Diodes," Hewlett Packard Application Note 918.

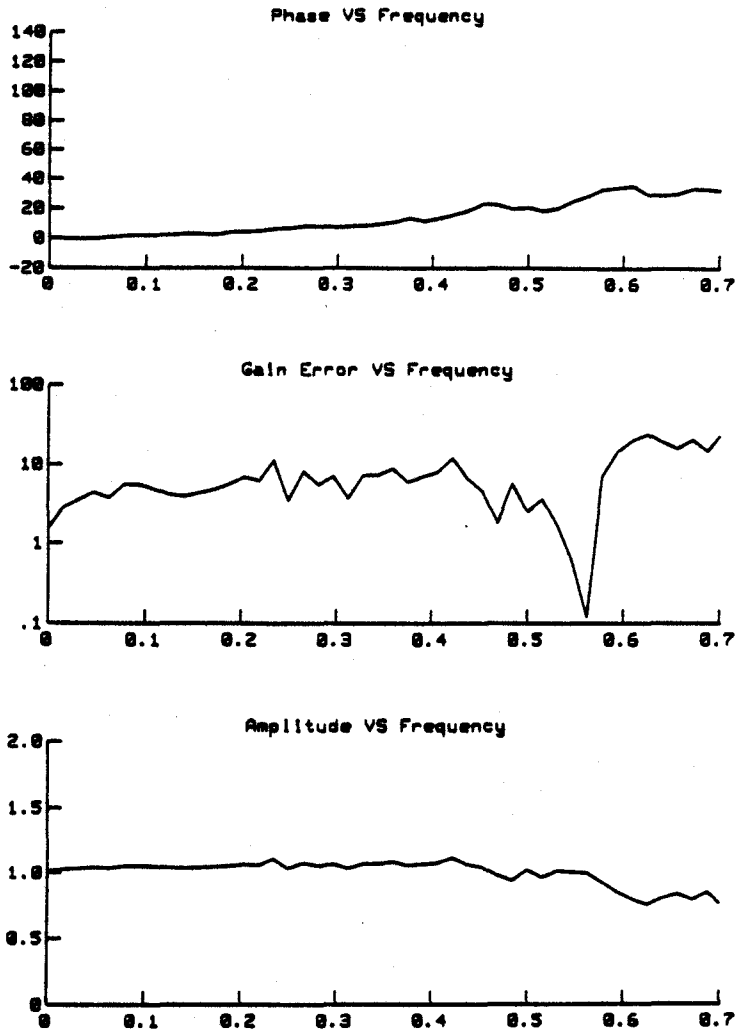

Figure 12 - Amplitude and Phase Plots of a 500 MHz commercially available Digitizer calculate using step response testing. Horizontal scale is in GHZ and the vertical scale is normalized and linear.