UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PICTOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 7,800,145

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,800,145

TABLE OF CONTENTS

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 7,800,145
Ex. 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex. 1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex. 1004	Prosecution History of U.S. Patent No. 7,800,145
Ex. 1005	U.S. Patent No. 7,259,413 to Rhodes ("*Rhodes-413*")
Ex. 1006	U.S. Patent Publication No. 2003/0228736 to Kimura ("*Kimura*")
Ex. 1007	U.S. Patent No. 7,335,958 to Mouli ("*Mouli*")
Ex. 1008	U.S. Patent No. 7,250,647 to Rhodes("*Rhodes-647*")
Ex. 1009	U.S. Patent No. 7,155,689 to Pierrat ("*Pierrat*")
Ex. 1010	D. Neamen, *Semiconductor Physics and Devices – Basic Principles*, 3rd Ed. (2003) ("*Neamen*")
Ex. 1011	S. Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1 (2000) ("*Wolf-V1*")
Ex. 1012	S. Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 3 (1995) ("*Wolf-V3*")
Ex. 1013	U.S. Patent No. 7,535,042 to Rhodes ("*Rhodes-042*")
Ex. 1014	U.S. Patent No. 7,602,438 to McGarvey et al. ("*McGarvey*")
Ex. 1015	Memorandum Adopting Report and Recommendation of United States Magistrate Judge on Claim Construction (Dkt. #401), *Imperium (IP) Holdings, Inc. v. Apple, Inc.*, No. 4:11-cv-00163-RC-ALM (E.D. Tex. Jan. 28, 2013).
Ex. 1016	Report and Recommendation of United States Magistrate Judge (Dkt. #209), *Imperium (IP) Holdings, Inc. v. Apple, Inc.*, No. 4:11-cv-00163-RC-ALM (E.D. Tex. Jul. 2, 2012).

Ex. 1017	Amended Complaint (Oct. 22, 2020) in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission
Ex. 1018	Notice of Institution of Investigation (Nov. 25, 2020) in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission (published at 85 Fed. Reg. 77,238-39 (Dec. 1, 2020)
Ex. 1019	(RESERVED)
Ex. 1020	(RESERVED)
Ex. 1021	Order #4 Setting Target Date at Sixteen Months in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission (Dec. 18, 2020)
Ex. 1022	Order #5 Regarding Procedural Schedule in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission (Dec. 18, 2020)
Ex. 1023	Order #6 Setting Procedural Schedule in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission (Jan. 6, 2021)
Ex. 1024	LG Energy Solution Responds to ITC Delay in Trade Secret Dispute (Dec. 9, 2020)

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner" or "Samsung") requests *inter partes* review of claims 1-3, 5, 6, 9, 10, and 12 ("the challenged claims") of U.S. Patent No. 7,800,145 ("the '145 patent") (Ex. 1001), which, according to PTO records, is assigned to Pictos Technologies Inc. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: The '145 patent is at issue in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission ("the ITC Investigation").

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), (3) Phillip Citroën (Reg. No. 66,541), (4) Howard Herr (*pro hac vice* admission to be requested). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20036, Tel.: 202.551.1700, Fax: 202.551.1705,

email: PH-Samsung-Pictos-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '145 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-3, 5, 6, 9, 10, and 12 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1-3, 5, 6, 9, 10, and 12 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Rhodes-647* (Ex. 1008) in view of *Kimura* (Ex. 1006); and

Ground 2: Claims 1-3, 5, 6, 9, 10, and 12 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Rhodes-413* (Ex. 1005) in view of *Kimura* and *Rhodes-042* (Ex. 1013).

The '145 patent issued September 21, 2010, from U.S. App. No. 11/026,582 filed Dec. 30, 2004. *Rhodes-413* was issued on Aug. 21, 2007, from U.S. App. No. 10/950,927 filed September 28, 2004, *Rhodes-647* was issued on July 31, 2007, from

U.S. App. No. 10/611,892 filed Jul. 3, 2003, and *Rhodes-042* was issued on May 19, 2009, from U.S. App. No. 10/881,525 filed July 1, 2004. Thus, *Rhodes-413*, *Rhodes-647*, and *Rhodes-042* qualify as prior art to the '145 patent at least under pre-AIA 35 U.S.C. § 102(e). *Kimura* published December 11, 2003, from U.S. App. No. 10/335,912 filed Jan. 3, 2003. Thus, *Kimura* qualifies as prior art to the '145 patent at least under pre-AIA 35 U.S.C. § 102(b). None of these references were considered during prosecution. (*See generally* Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '145 patent ("POSITA") would have had a bachelor's degree in a field relating to semiconductor design and manufacturing like physics, electrical engineering, or other related subjects, and two to three years of experience in the design and fabrication of semiconductor devices such as image sensors. More education can supplement practical experience and vice versa. (Ex. 1002, ¶¶20-21.)[1]

VII. CLAIM CONSTRUCTION

During IPR, claims are construed according to the "*Phillips* standard." *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*); 83 Fed. Reg.

[1] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '145 patent. (Ex. 1002, ¶¶1-15, 20-37; Ex. 1003.)

51341 (Oct. 11, 2018). The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[2] (Ex. 1002, ¶38.)

VIII. PROSECUTION HISTORY OF THE '145 PATENT

Following Office Actions rejecting all pending claims (Ex. 1004, 146-156, 164-169, 187-197), Applicant filed a Pre-Appeal Brief Request for Review, asserting the Examiner failed to address a claim limitation, namely "in an absence of the control voltage the control terminal creates an electric field tending to repel the electrons from a portion of the body by the control terminal." (*Id.*, 201-202.) In response, the PTO reopened prosecution of the application (*id.*, 209), and then the Examiner simply allowed the claims (*id.*, 210-216). Based on the search history, the Examiner does not appear to have specifically searched for the allegedly ignored limitation (*Id.*, 219; Ex. 1002, ¶¶44-45; *see also id.*, 39-43), which, as demonstrated below is disclosed in the prior art.

[2] Petitioner reserves all rights to raise claim construction and other arguments in this and other proceedings as appropriate.

IX. DETAILED EXPLANATION OF GROUNDS[3]

As discussed below, claims 1-3, 5, 6, 9, 10, and 12 are unpatentable in view of the prior art. (Ex. 1002, ¶¶16-172.)

A. Ground 1: *Rhodes-647* in view of *Kimura* Renders Obvious Claims 1-3, 5, 6, 9, 10, and 12

1. Claim 1

a) An image sensor integrated circuit, comprising:

To the extent the preamble of claim 1 is limiting, *Rhodes-647* discloses the limitations therein. (Ex. 1002, ¶¶58-61.) As shown in figure 12 below, *Rhodes-647* discloses an integrated CMOS imager 800 having a pixel array 200 on a chip. (Ex. 1008, FIG. 12, 3:12-13, 9:36-39, 13:16-14:21; *see also id.*, FIG. 11, 9:29-35, 3:39-40; Ex. 1002, ¶58.)

[3] Section IX references exhibits other than the identified prior art for each ground. Such exhibits reflect the state of the art known to a POSITA at the time of the alleged invention consistent with the testimony of Dr. Baker.

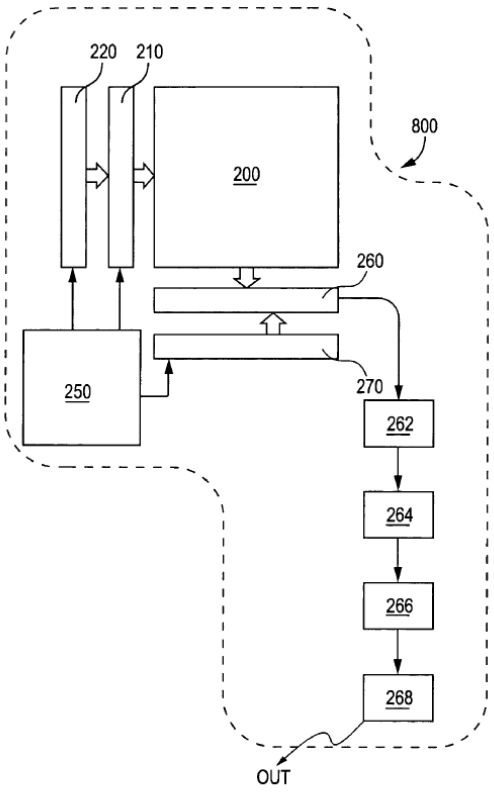
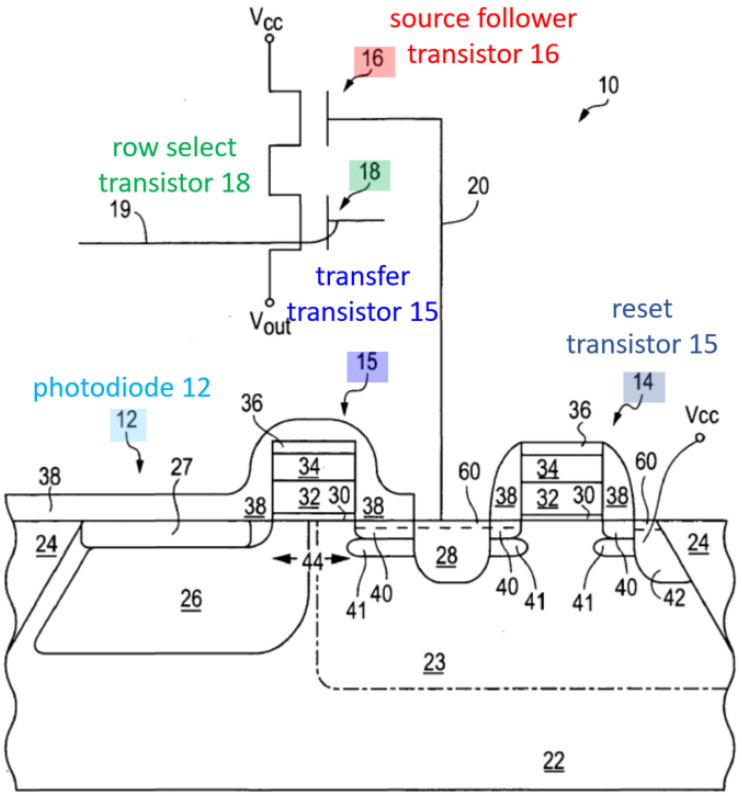


FIG. 12

(Ex. 1008, FIG. 12.) *Rhodes-647* discloses that pixel array 200 includes multiple pixels 10 arranged in columns and rows. (*Id.*, 9:36-41; *see also id.*, FIG. 11, 4:48-53, 9:29-35.) *Rhodes-647* explains that pixels 10 may be selectively output by row and column select lines using a combination of row and column circuitry, including, e.g., row driver 210, row address decoder 220, control circuit 250, column driver 260, and column address decoder 270. (*Id.*, 9:41-60; Ex. 1002, ¶58.)

Rhodes-647 discloses that, as shown in figure 1(a) below, each pixel 10 of array 200 shown in figure 12 may be a four-transistor (4T) CMOS pixel, including a photodiode 12, a transfer transistor 15, a reset transistor 14, a source follower

transistor 16, and a row select transistor 18. (Ex. 1008, 4:27-33, 4:54-57; *see also id.*, 4:16-26, 9:29-35 ("FIG. 11 shows part of an array 200 of 4T CMOS imager pixel 10 circuits."), FIG. 11.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶¶59-60.)

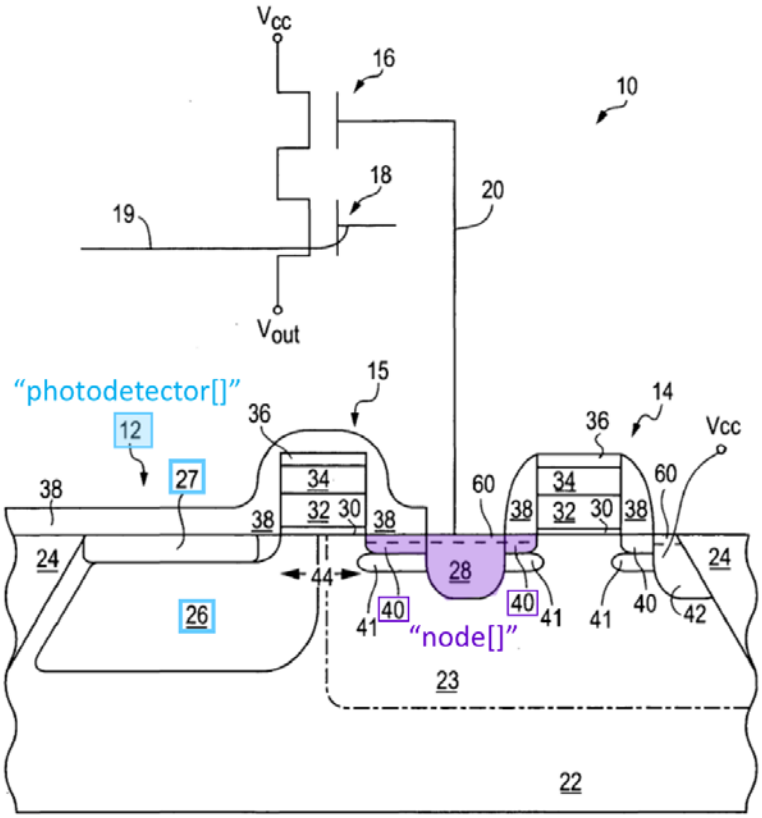
The CMOS imager 800 chip, which includes a pixel array where each pixel includes a photodiode, is an "image sensor integrated circuit," as claimed. (Ex. 1002, ¶61; *infra* Sections IX.A.1(b)-(h).)

b) a plurality of photodetectors generating electrons excited by incident photons;

Rhodes-647 discloses this limitation. (Ex. 1002, ¶62.) *Rhodes-647* discloses that the pixel array 200 includes a plurality of pixels 10, where each pixel includes a photodiode 12 ("plurality of photodetectors"). (Ex. 1008, 4:30-33, 4:54-60 ("The 4T CMOS pixel 10…includes a photodiode 12").) Photodiode 12 generates charges ("electrons") that are excited by incident light ("photons"). (Ex. 1008, 1:11-15, 3:24-26, 4:16-20, Abstract; Ex. 1001, claim 10 ("the plurality of photodetectors is a plurality of photodiodes").) Thus, *Rhodes-647* discloses "a plurality of photodetectors generating electrons excited by incident photons." (Ex. 1002, ¶62.)

c) a plurality of nodes, wherein each of the plurality of photo detectors has a corresponding node of the plurality of nodes;

Rhodes-647 discloses this limitation. (Ex. 1002, ¶¶63-65.) As shown in figure 1(a) below, each pixel 10 includes a "floating diffusion region 28" that is "electrically link[ed]" to photodiode 12. (Ex. 1008, 4:58-60.) As discussed in more detail below, a POSITA would have understood that the combination of floating diffusion region 28 and active area extension region 40 (highlighted in figure 1(a) below) corresponds to the claimed "node." (Ex. 1002, ¶63.)

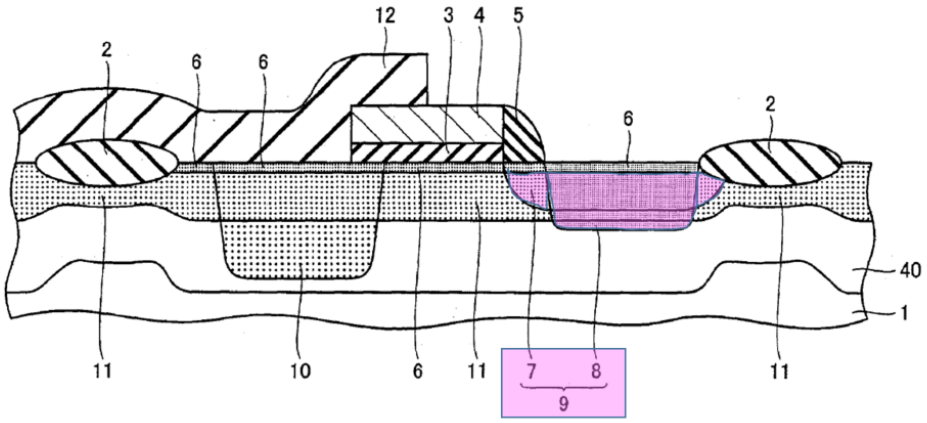


(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶63.) Both region 40 and floating diffusion region 28 are n-type regions that function together as the drain terminal of the transfer transistor 15. (Ex. 1008, 4:60-65, 3:31-39, 3:41-42, 4:60-65; *see also id.*, 2:15-20, 3:40-41, 5:10-11; Ex. 1002, ¶63.) Given that regions 28 and 40 act together as the drain terminal of transistor 15, a POSITA would have understood that regions 28 and 40 together form a "node" for the pixel. (Ex. 1002, ¶63.) Such an understanding is consistent with the state of the art, including *Kimura*,[4] which

[4] *Kimura* demonstrates the knowledge of a POSITA at the relevant time.

discloses, as shown in figure 13 below, that floating diffusion region 9 includes low-concentration impurity region 7 and high-concentration region 8 of the same n-type doping. (Ex. 1006, ¶¶[0018]-[0019], FIGs. 1-16; *see also id.*, ¶¶[0004], [0010].)

FIG.13 PRIOR ART



(Ex. 1006, FIG. 13 (annotated); Ex. 1002, ¶63.)

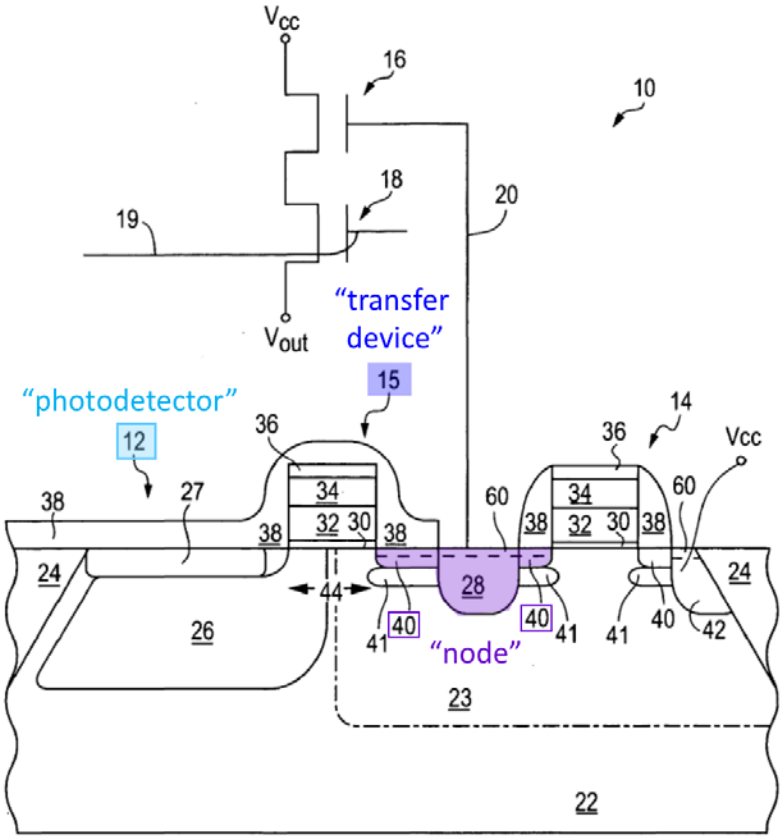
Indeed, a POSITA would have understood that region 40 in *Rhodes-647* is a lightly-doped extension of region 28. (Ex. 1002, ¶64.) *Rhodes-647* discloses that region 28 is an "active area," and that region 40 is an "extension" of the active area. (Ex. 1008, 5:30-32 ("active area extension region 40…extends the active area to the edge of the transfer transistor 15 gate."), 8:48-50 ("floating diffusion region 28 also is an active area and acts as a type of source/drain region."); *see also id.*, 1:15-18.)

The understanding that regions 28 and 40 together constitute a "node" is also supported by *Rhodes-647*'s disclosure of "floating diffusion region [e.g., region 28] comprising an active area extension region [e.g., region 40] at…[one] side of" a

transfer gate. (Ex. 1008, 12:8-9; Ex. 1002, ¶65.) Moreover, the combination of regions 28 and 40 corresponding to the claimed "node" is consistent with the '145 patent's disclosure, which uses the terms "n-type lightly-doped drain (nLDD)" and "floating diffusion" interchangeably. (*See* Ex. 1001, 13:37-45.) Therefore, the combination of regions 28/40 in *Rhodes-647* constitutes a "node" for each pixel. (Ex. 1002, ¶65.)

d) a plurality of transfer devices controlling a transfer of the electrons from said each of the plurality of photodetectors to the corresponding node, each of the plurality of transfer devices including:

Rhodes-647 discloses this limitation. (Ex. 1002, ¶66.) As shown in figure 1(a), each pixel 10 in the array includes a transfer transistor 15 ("a plurality of transfer devices") that controls the transfer of charges ("electrons") from photodiode 12 ("photodetector") to regions 28/40 ("node") for each pixel.



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶66.) *Rhodes-647* discloses that transistor 15, coupled between photodiode 12 and regions 28/40, "provides a gate for electrically linking the photodiode 12 to the other transistors 14, 16, 18 via a floating diffusion region 28." (Ex. 1008, 4:58-60; *see also id.*, 2:15-23.) Indeed, given that transistor 15 is a CMOS transistor, a POSITA would have understood that it is activated and deactivated to control the charge transfer from one terminal to the other, e.g., from photodiode 12 to regions 28/40. (Ex. 1002, ¶¶22-27, 66; Ex. 1008,

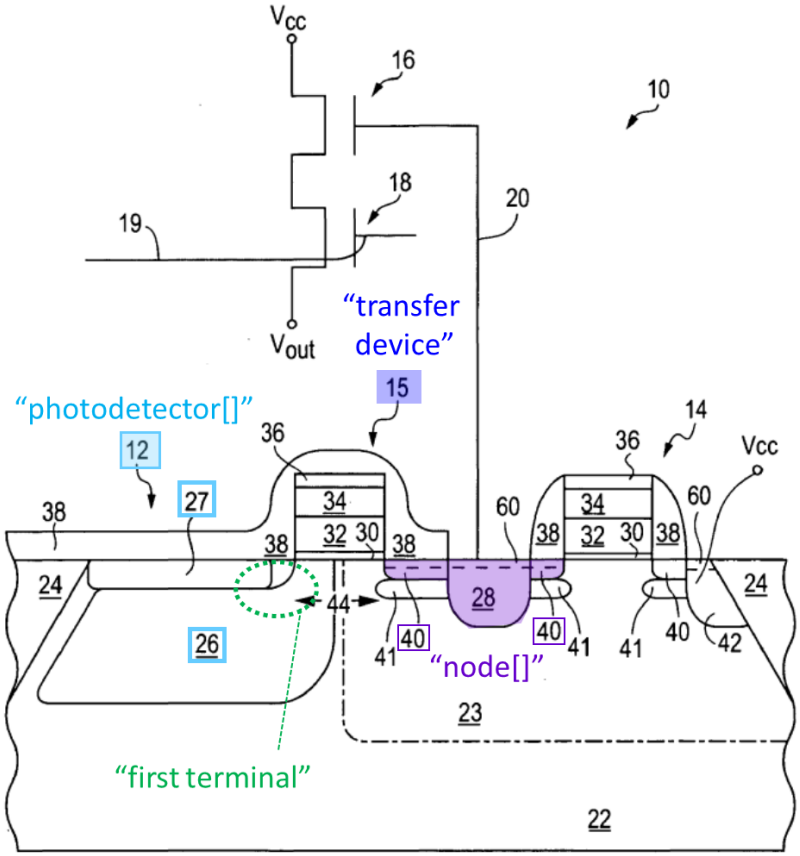
1:20-22, 1:34-36; Ex. 1010, 465-468[5].) Thus, *Rhodes-647* discloses this limitation. (Ex. 1002, ¶66; *infra* Sections IX.A.1(d)(1)-(4).)

(1) a first terminal coupled to one of the plurality of photodetectors;

Rhodes-647 discloses this limitation. (Ex. 1002, ¶¶67-69.) *Rhodes-647* discloses that transfer transistor 15 is an n-channel MOSFET. (Ex. 1008, 4:54-57, 11:41-42 ("n-channel devices").) Thus, a POSITA would have understood that transfer transistor 15 includes source, drain, and gate terminals, and a channel, where charge carriers flow from the source to the drain through the channel when a sufficient bias is applied to the gate. (Ex. 1002, ¶¶ 23-27, 67; Ex. 1010, FIG. 11.35, 484-485.)

As shown in figure 1(a) below, *Rhodes-647* discloses that one of the terminals of transistor 15 ("transfer device") for each pixel is coupled to the corresponding photodiode for the pixel ("a first terminal coupled to one of the plurality of photodetectors"). (Ex. 1008, 4:58-60; FIG. 1(a); Ex. 1002, ¶¶68-69.)

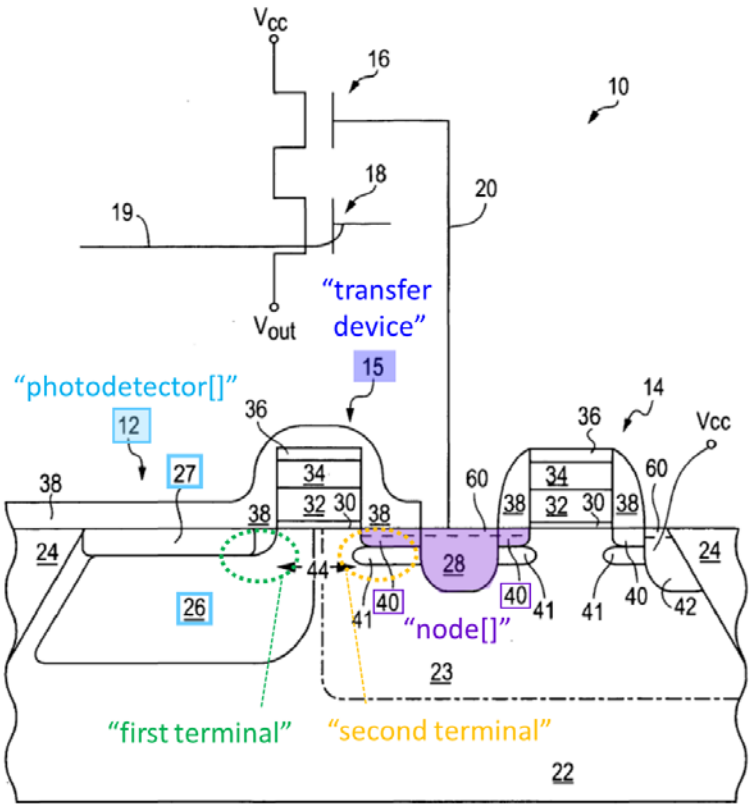
[5] *Neamen* demonstrates the knowledge of a POSITA at the relevant time.



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶68.)

(2) a second terminal coupled to one of the plurality of nodes; and

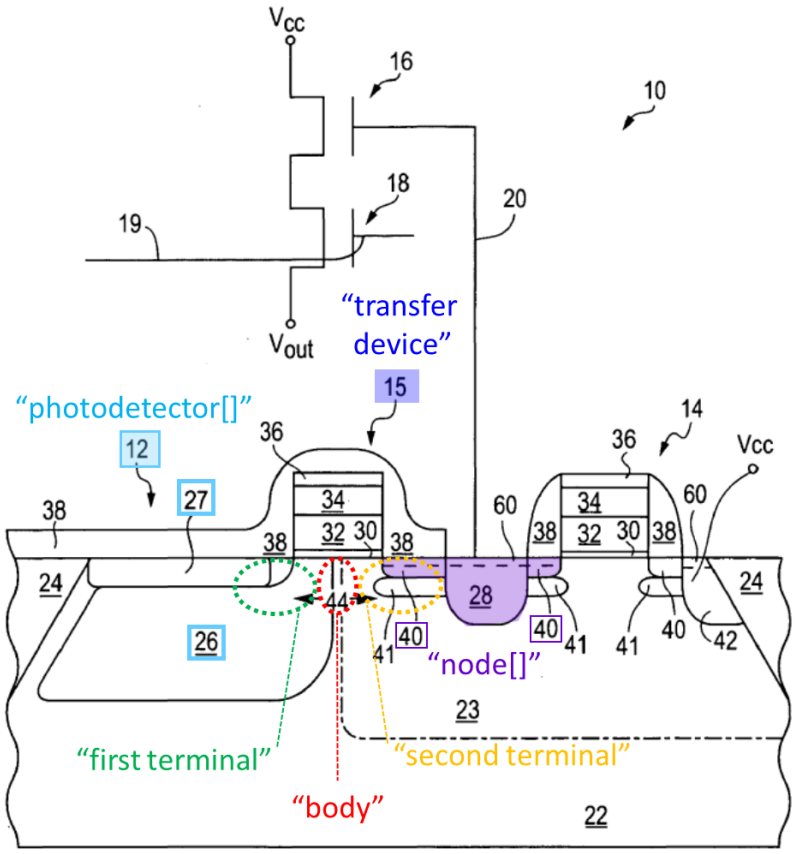
Rhodes-647 discloses this limitation. (Ex. 1002, ¶70.) As shown in figure 1(a) below, the transistor 15 ("transfer device") for each pixel 10 in array 200 also has a terminal ("second terminal") coupled to the "node" formed by the combination of regions 28 and 40. (Ex. 1008, Ex. 1008, 4:54-66, FIG. 1(a); *see also id.*, 3:31-39, 8:48-50; Ex. 1002, ¶70.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶70.)

(3) a body between the first terminal and the second terminal; and

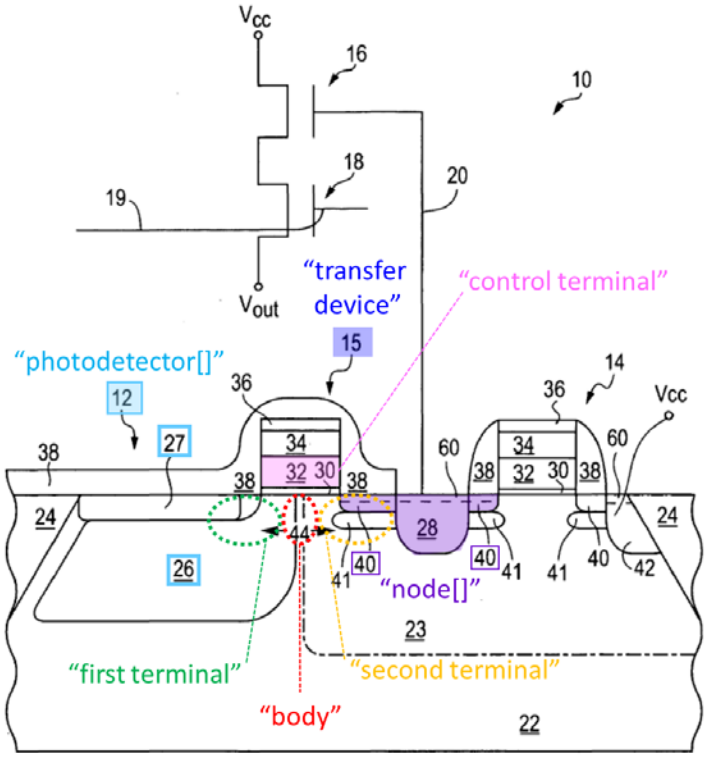
Rhodes-647 discloses this limitation. (Ex. 1002, ¶71.) As shown in figure 1(a) below, each transistor 15 ("transfer device") includes a channel ("body") between the source ("first terminal") and the drain ("second terminal"). (Ex. 1008, 4:58-60, 7:30-40, 11:41 ("n-channel devices"), 12:14-16 ("transfer transistor has an underlying channel region"), FIG. 1(a); Ex. 1002, ¶¶ 23-27, 71.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶71.)

(4) a control terminal electrically coupled to the body, wherein the transfer of the electrons occurs through the body between the first terminal and the second terminal in response to a control voltage of sufficient value applied to the control terminal, and in an absence of the control voltage the control terminal creates an electric field tending to repel the electrons from a portion of the body by the control terminal;

Rhodes-647 in view of *Kimura* discloses or suggests this limitation. (Ex. 1002, ¶¶72-85.) As shown in annotated figure 1a, transistor 15 includes a gate electrode 32 ("control terminal") made of doped polysilicon. (Ex. 1008, 6:34-35, FIG. 1(a); *see also id.*, 6:16-41.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶72.) Transistor 15 is a CMOS transistor (Ex. 1008, 2:45-47), and a POSITA would have understood that gate electrode 32 is electrically "coupled to" the channel ("body") of transistor 15 in a manner consistent with '145 patent's limited disclosure. For example, just like other CMOS transistors, the applied gate bias controls the conductivity of the channel underlying the gate. (Ex. 1002, ¶¶23-27, 72; *see also* Ex. 1010, 450-455, 484-489.) Notably, the '145 patent does not provide any disclosure of a "control terminal coupled to the body" in any manner different from the simple, well-known relationship between the gate electrode and underlying transistor channel that exists for other CMOS transistors. Thus, *Rhodes-647* discloses "control terminal electrically coupled to the body." (Ex. 1002, ¶72.)

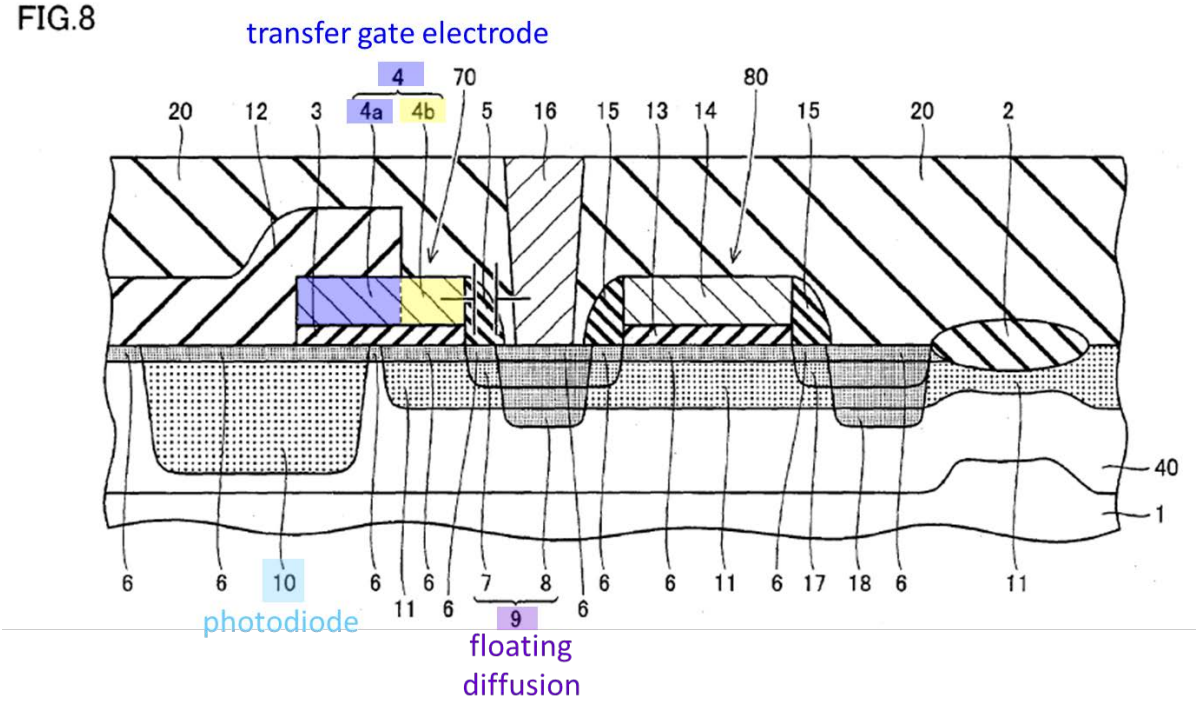
Furthermore, as a POSITA would have understood, by applying a voltage exceeding the threshold voltage of transistor 15 to gate electrode 32 ("control voltage of sufficient value applied to the control terminal") the transfer transistor 15 is activated or turned "on," thereby allowing charges ("electrons") to flow through the transistor's channel ("body") between the terminals of the transistor ("transfer of the electrons occurs through the body between the first terminal and the second terminal"). (Ex. 1002, ¶¶23-27, 73; Ex. 1008, 6:57-60, 12:14-16, 12:63-64, 13:22-23; Ex. 1010, 450-455, 484-489.)

If the voltage on gate electrode 32 is less than the threshold voltage, transistor 15 is not activated, and charges ("electrons") are not able to flow through the channel ("body") between the two terminals. (Ex. 1002, ¶¶23-27, 74; *see also* Ex. 1008, 1:46-56; Ex. 1010, 487 ("When $V_{GS} < V_T$, the drain current is zero.").) Therefore, *Rhodes-647* discloses that "in an absence of the control voltage" (e.g., when not applying a voltage equal to or greater than the threshold voltage to gate electrode 32), transistor 15 is not activated and is in the "off-state." (Ex. 1002, ¶74.)

Rhodes-647 does not expressly disclose that in an absence of the control voltage "the control terminal creates an electric field tending to repel the electrons from a portion of the body by the control terminal." Nevertheless, a POSITA would have found it obvious to implement such a feature for each pixel of *Rhodes-647* in view of *Kimura*. (Ex. 1002, ¶75.)

As shown in figure 8 below, *Kimura*, like *Rhodes-647*, discloses an imaging device that includes a photodiode, a floating diffusion region, and a transfer transistor controlling the charge transfer. (Ex. 1006, ¶¶[0128]-[0137]; FIG. 8.) Therefore, a POSITA would have had reason to look to *Kimura* when implementing an imager system of *Rhodes-647*. (Ex. 1002, ¶76.)

FIG.8



(Ex. 1006, FIG. 8 (annotated); Ex. 1002, ¶76.)

Kimura discloses that transfer gate electrode 4, similar to the gate electrode 32 in *Rhodes-647*, is "a polycrystalline silicon film" that has a low p-type concentration region (4b) and a high p-type concentration region (4a). (Ex. 1006, ¶[0131] (disclosing that "[g]ate electrode 4 [has] high concentration impurity region 4a and low concentration impurity region 4b," which are achieved by a two-step doping process), ¶[0132] (disclosing an alternative method to achieve a low-doped p-type region and a high-doped p-type region); Ex. 1002, ¶77.)

While *Rhodes-647* discloses that the gate electrode of its transfer device is doped polysilicon, *Rhodes-647* does not expressly disclose the type of impurity used

for doping the gate electrode or how that doping is performed. As such, a POSITA would have looked to other references, like *Kimura*, that disclose such information. (Ex. 1002, ¶78; *see generally* Ex. 1008.) Having looked to *Kimura*, a POSITA would have found it obvious to include a graded p-type polysilicon gate structure, like that disclosed by *Kimura*, when implementing transfer transistors for an imaging device like that disclosed in *Rhodes-647*. (Ex. 1002, ¶78.)

Such a POSITA would have been motivated to do so because *Kimura* teaches that such a graded p-type polysilicon gate structure "is highly needed" as it "suppress[es] the trapping of the charges in the potential barrier or the potential drop by the electric field of charge transfer gate electrode 4." (Ex. 1006, ¶[0135].) Furthermore, using such a graded p-type polysilicon gate reduces the "parasitic capacitance between contact plug 16 and gate electrode 4" (*id.*, ¶[0134]) without substantially "decreasing the charge transfer speed" (*id.*, ¶[0136]), and also enhances the signal-to-noise ratio of the photoelectrically-converted signals (*id.*, ¶[0137]). Accordingly, a POSITA would have found it beneficial to implement a graded p-type polysilicon gate structure, like that disclosed in *Kimura*, in an imaging device as disclosed by *Rhodes-647*. (Ex. 1002, ¶78.)

A POSITA would have had a reasonable expectation of success in implementing a graded p-type polysilicon gate structure since such polysilicon gate structures were well-known for semiconductor devices. (Ex. 1002, ¶79; Ex. 1007,

8:1-13 (disclosing that forming a p-type poly-silicon transfer gate is "known in the art") [6].)

Moreover, *Rhodes-647* already discloses forming a doped polysilicon gate structure (albeit without specifying the doping type), thereby demonstrating that a POSITA knew how to implement a doped polysilicon gate and that such a gate is functional in the imaging device of *Rhodes-647*. (Ex. 1002, ¶80; Ex. 1008, 6:16-23.)

Accordingly, including a graded p-type polysilicon gate structure like that disclosed in *Kimura* in the image sensor integrated circuit of *Rhodes-647* would have been nothing more than the combination of known prior art elements (graded p-type polysilicon gate structures for transfer transistors as disclosed by *Kimura* with the transfer transistor in pixels of image sensors as disclosed in *Rhodes-647*) using known transistor fabrication techniques, where each element performs the same function described in *Rhodes-647* and *Kimura*, to achieve the predictable result of a transfer transistor that is improved to provide reduced charge trapping and reduced parasitic capacitance. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). As discussed above, both *Rhodes-647* and *Kimura* describe transfer transistors used in pixel arrays, but *Kimura* describes additional details regarding the gate electrode of

[6] *Mouli* demonstrates the knowledge of a POSITA at the relevant time.

those transistors not found in *Rhodes-647* that beneficially reduces charge trapping and parasitic capacitance. Therefore, a POSITA would have recognized that *Kimura's* teachings relating to a graded p-type polysilicon gate structures could be applied to *Rhodes-647's* transfer transistor in a similar way. *Id.* at 417. As also discussed above, a POSITA would have been encouraged to implement such a graded p-type polysilicon gate in *Rhodes-647's* transfer transistor to provide similar reduced charge trapping and reduced parasitic capacitance to improve overall system performance. (Ex. 1002, ¶80.)

Additionally, including such a graded p-type polysilicon gate in *Rhodes-647's* transfer transistor would have been straightforward for a POSITA given such a person's knowledge and the disclosure in *Kimura*. (Ex. 1002, ¶81.) For example, the combination would have required nothing more than using well-known, rudimentary, and widely available techniques for transistor gate formation and doping to *Rhodes-647's* transistor, where those techniques were commonly used for forming doped polysilicon gates at the time. (*Id*.) Such a combination would not have detracted from the overall functionality of *Rhodes-647's* system, which would have continued to operate as described in *Rhodes-647*. (*Id*.)

Having combined *Rhodes-647* and *Kimura*, a POSITA would have understood that the resulting graded p-type poly-silicon gate would disclose the features ascribed to the control terminal in claim 1. For example, such a gate

implemented in the *Rhodes-647-Kimura* combination would "create an electric field tending to repel the electrons from a portion of the body by the control terminal," as claimed, when not applying the threshold voltage to such a p-type poly-silicon gate electrode ("in an absence of the control voltage the control terminal"). (Ex. 1002, ¶¶28-34, 82.) As a POSITA would have understood, a p-type poly-silicon gate has a relatively high "work function," where work function is a material property that quantifies the amount of energy required to remove an electron from the Fermi level of the material. (Ex. 1002, ¶¶28-34, 82; Ex. 1007, 5:1-4, 8:6-13 (disclosing that a p-type gate electrode has a "higher work-function" than the conventional n-type electrode).)

A POSITA would have also understood that the p-type gate electrode and the channel would have had different work functions (i.e., electron potentials) because the graded p-type gate electrode and the channel are of different materials (polysilicon v. silicon) and are of different doping concentrations (graded doping concentration for forming a conductive gate electrode in comparison to a doping concentration suitable for forming a non-leaky channel). (Ex. 1002, ¶¶28-34, 83; Ex. 1008, 4:3-5, 6:57-60, 6:42-44, 7:41-44; Ex. 1006, ¶[0132]; Ex. 1010, 460-461 (disclosing the "metal-semiconductor work function difference" between a p-type polysilicon gate and a p-type silicon substrate), FIG. 11.13(b).) Indeed, it was well known at the time of the alleged invention that such a work-function difference

between the gate electrode and the channel impacts the threshold voltage of the transistor. (Ex. 1002, ¶¶28-34, 83; Ex. 1007, 4:49-5:8; Ex. 1010, 467 (disclosing that the threshold voltage is a function of the work function difference).)

Furthermore, a POSITA would have understood that the work function difference creates a potential drop across the gate dielectric, where the potential drop creates an electric field to exert force on charges in the body/channel of the semiconductor—even when no bias is applied to the gate electrode. (Ex. 1002, ¶¶28-34, 84; Ex. 1010, 451, 458 ("The voltage V_{ox0} is the potential drop across the oxide **for zero applied gate voltage** and [V_{ox0}] is not necessarily zero"), 460-461, FIG. 11.13(b).) A POSITA would have understood that such an electric field would attract positive charges, which are known as "holes," to the channel region and repel negative charges, i.e., electrons, from the channel region. (Ex. 1002, ¶¶28-34, 84; Ex. 1010, 460-461, FIG. 11.13(b).)

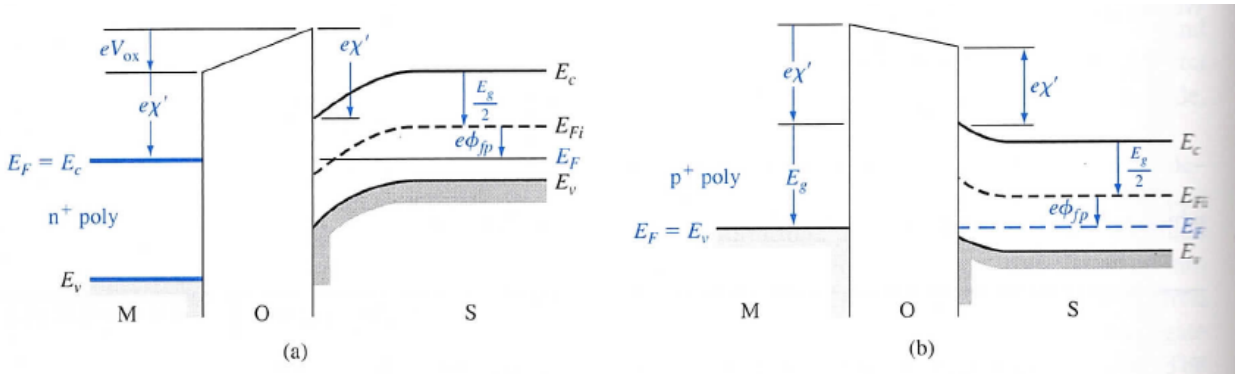


Figure 11.13 | Energy-band diagram through the MOS structure with a p-type substrate at zero gate bias for (a) an n^+ polysilicon gate and (b) a p^+ polysilicon gate.

(Ex. 1010, 11.13(b) (right figure).) Indeed, as shown above in FIG. 11.13(b) of *Neamen*, which describes the band diagram of a MOS structure similar to that of the *Rhodes-647-Kimura* combination (i.e., a stack of p-type polysilicon gate, oxide, and p-type silicon), in the region of the semiconductor (denoted as "S" in the figure) close to the oxide ("O") the Fermi level (E_F) near the O-S interface is further away from the conduction band (E_C) than in the rest of the semiconductor, indicating that the portion of the semiconductor near the interface has a lower electron concentration than the rest of the semiconductor, i.e., the electrons are repelled away from the interface region. (Ex. 1002, ¶¶28-34, 84; Ex. 1010, FIG. 11.13(b).)[7]

Given that the electric field is created by the work function difference of the materials alone, such an electric field exists even when no gate bias is applied to the gate electrode. (Ex. 1002, ¶¶28-34, 85; Ex. 1010, 458.) Such an understanding is consistent with the '145 patent, disclosing that using p-type poly gate attracts holes, i.e., repels electrons. (Ex. 1001, 14:8-11.) Accordingly, because, in the absence applying a gate bias, the p-type polysilicon gate electrode creates an electric field that repels electrons from the channel, the *Rhodes-647-Kimura* combination

[7] FIG. 11.13(a) of *Neamen* shows that when an **n-type** polysilicon gate electrode is used, the semiconductor near the O-S interface has a higher electron concentration than the rest of the semiconductor. (Ex. 1002, ¶¶28-34, 84; Ex. 1010, 11.13(a).)

discloses or suggests "in an absence of the control voltage the control terminal creates an electric field tending to repel the electrons from a portion of the body by the control terminal" as claimed. (Ex. 1002, ¶85.)

e) a plurality of p-type regions . . .

The *Rhodes-647-Kimura* combination discloses or suggests this limitation. For clarity, this is discussed below in two parts. (Ex. 1002, ¶¶86-92.)

(1) a plurality of p-type regions having a concentration stronger than a background p-type concentration of the plurality of transfer devices, wherein…the plurality of p-type regions controlling the transfer of electrons from a photodetector of the plurality of photodetectors to the corresponding node of the photodetector…;

Rhodes-647 discloses forming a p-type halo implant 41 in p-type well 23 for each pixel 10 in array 200. *Rhodes-647* discloses, with reference to figure 4(a), first forming p-type well 23 in substrate 22. (Ex. 1008, 6:42-44, FIG. 4(a); Ex. 1002, ¶87.)

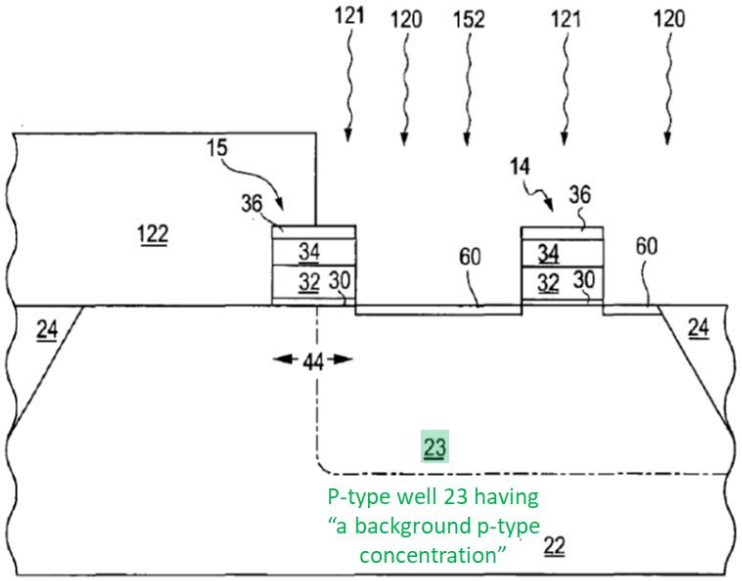


FIG. 4(a)

(Ex. 1008, FIG. 4(a) (annotated); Ex. 1002, ¶87.) Then, after forming p-well, and as shown in figure 6(a) below, additional p-type dopants are added to form halo implant 41 below region 40 in p-type well 23. (Ex. 1008, 7:41-50; *see also id.*, 7:15-40.)

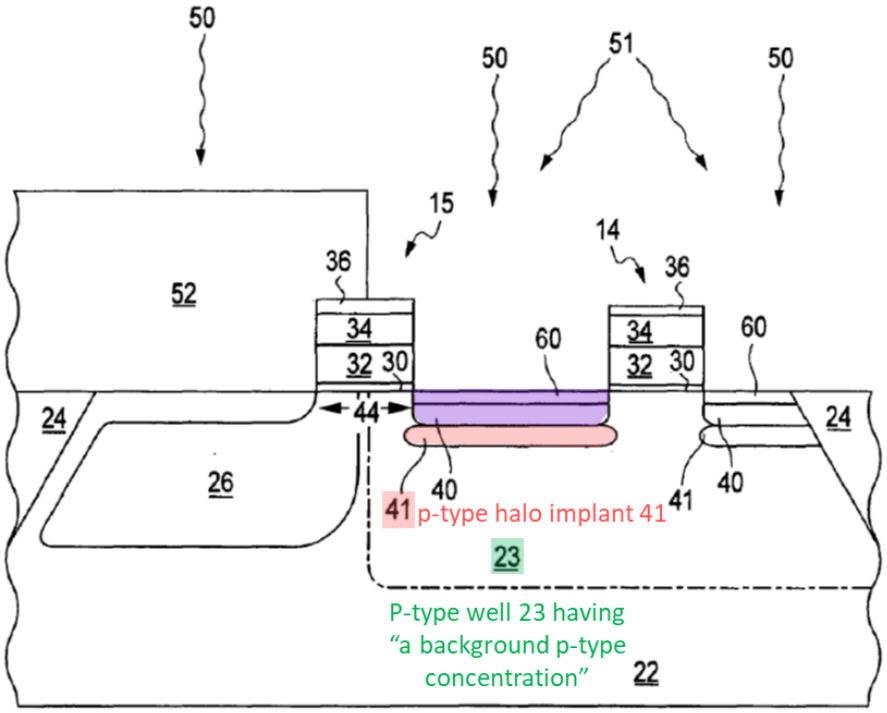
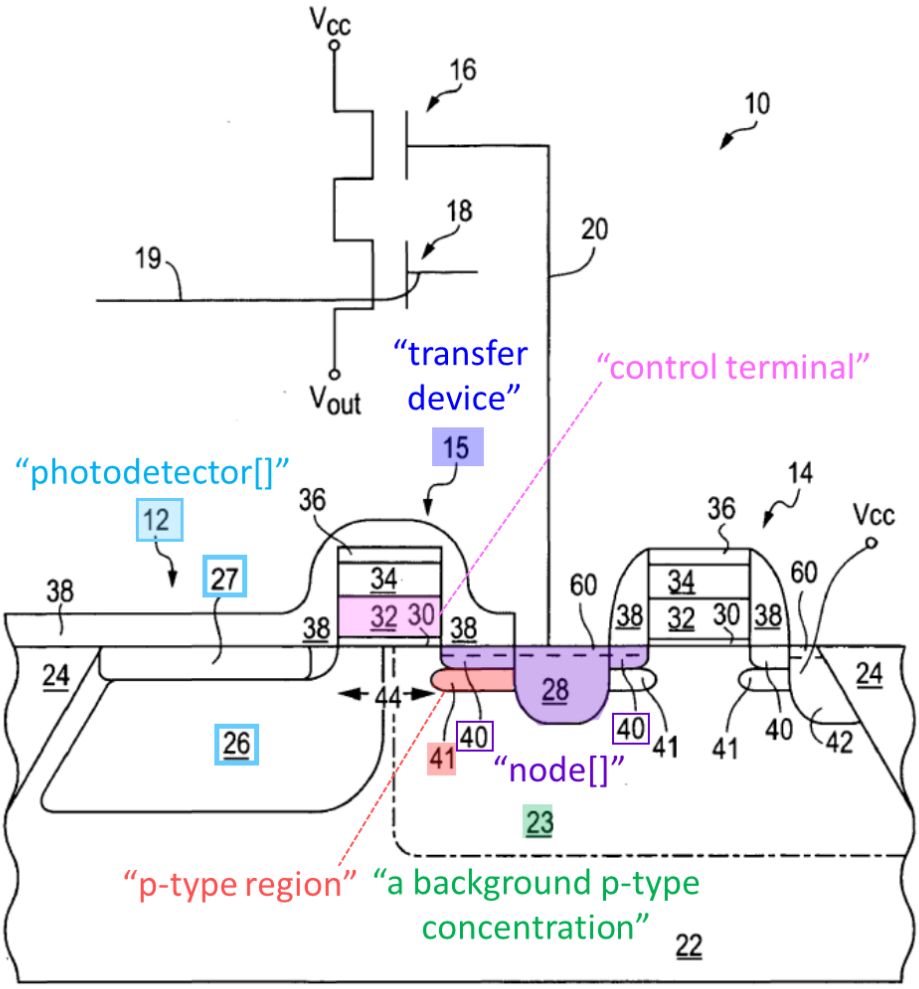


FIG. 6(a)

(Ex. 1008, FIG. 6(a) (annotated); Ex. 1002, ¶87.) The formation of floating diffusion region 28 (Ex. 1008, 8:16-30) for each pixel results in a halo implant 41 for each transistor 15 (the claimed "p-type region"). (Ex. 1002, ¶87.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶87.)

Because the p-type halo implant 41 is added to p-type well 23, a POSITA would have understood that the halo implant 41 has a stronger p-type concentration than that of the rest of the well. (Ex. 1002, ¶88; Ex. 1011, 423, 834-835; Ex. 1012,

238-240 (halo implantation "raises the doping concentration…").)[8] Accordingly, *Rhodes-647* discloses "a plurality of p-type regions having a concentration stronger than a background p-type concentration of the plurality of transfer devices." (Ex. 1002, ¶88.)

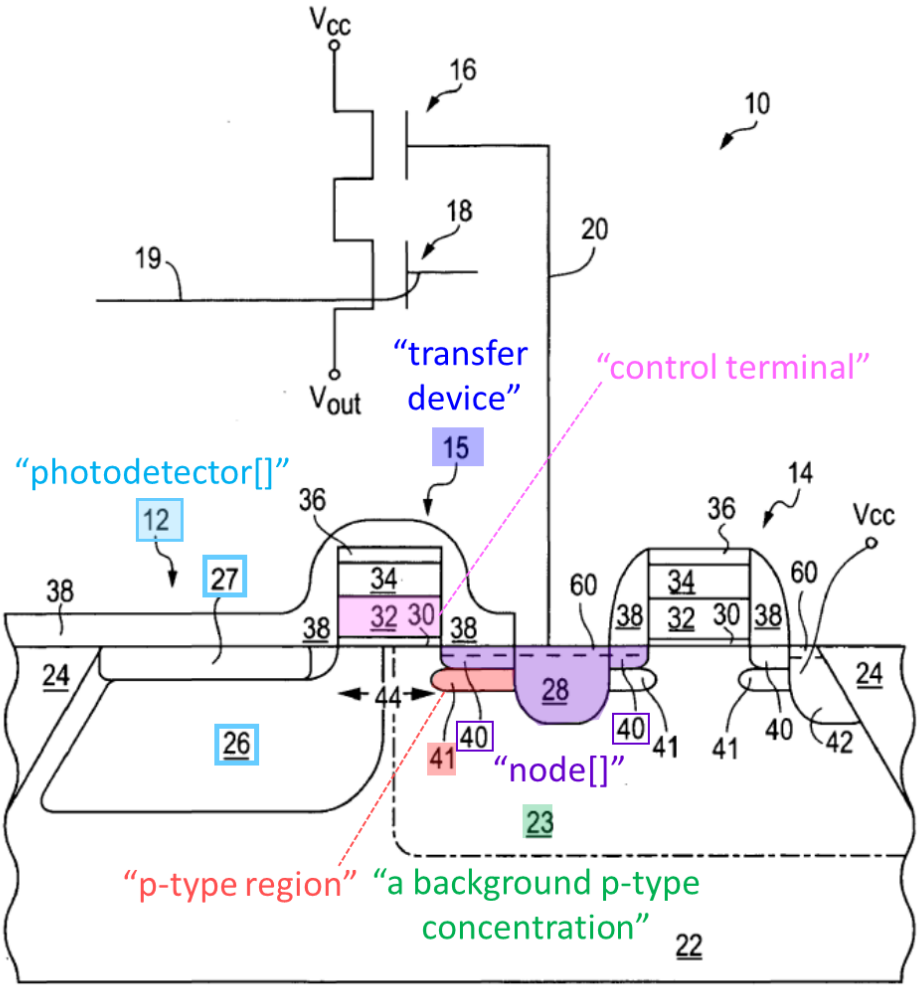
Furthermore, *Rhodes-647* discloses "the plurality of p-type regions controlling the transfer of electrons from a photodetector of the plurality of photodetectors to the corresponding node of the photodetector" in a manner consistent with the disclosure of the '145 patent. (Ex. 1002, ¶89.) For example, *Rhodes-647* discloses that halo implant 41 facilitates the operation of the transfer transistor 15 and is "to provide added punch-through protection" and reduce leakage current in transfer transistor 15. (Ex. 1008, 4:66-5:2). Thus, a POSITA would have understood that *Rhodes-647* discloses "p-type regions controlling the transfer of electrons" through the channel of transfer transistor 15. (Ex. 1002, ¶89; Ex. 1011, 423, 834-835; Ex. 1012, 232 (gate electrode has "less control" of the current when punchthrough occurs), 238-240.) Furthermore, as discussed above in Sections IX.A.1(d),(d)(3), *Rhodes-647* discloses that transistor 15 controls the electron

[8] *Wolf-V1 and Wolf-V2* demonstrate the knowledge of a POSITA at the relevant time.

transfer from photodiode 12 to the node (i.e., regions 28/40). (*Supra* Sections IX.A.1(d), (d)(3); Ex. 1008, 1:34-36, 4:58-60, 11:41, 12:14-16; Ex. 1002, ¶89.)

> **(2) wherein each of the plurality of p-type regions has a lateral position only partly under the control terminal of a transfer device of the plurality of transfer devices…and the plurality of p-type regions has the lateral position at least partly under the corresponding node, and the plurality of p-type regions has the lateral position stopping short of the plurality of photodetectors and stopping short of a plurality of reset devices;**

As shown in figure 1(a) below, *Rhodes-647* discloses that halo implant 41 for each pixel in the array ("plurality of p-type regions") is positioned only partially under gate electrode 32. (Ex. 1008, FIG. 1(a), 5:32-34 ("The halo implant region 41…**extends under a portion of the transistor 15 gate**."), 7:41-48, 12:20-21; Ex. 1002, ¶90.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶90.) Thus, *Rhodes-647* discloses that "each of the plurality of p-type regions has a lateral position only partly under the control terminal of a transfer device of the plurality of transfer devices." (Ex. 1002, ¶90.)

Furthermore, as also shown in figure 1(a) above, *Rhodes-647* discloses that the halo implant 41 has a lateral position that is partly under the "node" formed by regions 28/40. (Ex. 1008, FIG. 1(a); *see also id.*, 12:6-13 ("floating diffusion region

comprising an active area extension region…and a halo implant region below said active area extension region"), 12:59-60 ("a halo implant region…below said single active area extension region").) Thus, *Rhodes-647* discloses "the plurality of p-type regions has the lateral position at least partly under the corresponding node." (Ex. 1002, ¶91.)

Additionally, as disclosed in figures 2(a), 2(b), and 11 of *Rhodes-647* (all of which show a plan view of pixel 10 from figure 1(a)), because halo implant 41 is only positioned along the boundary where gate electrode 32 of transistor 15 and regions 28/40 meet, halo implant 41 stops short of photodiode 12 and reset transistor 14. (Ex. 1002, ¶92; Ex. 1008, 4:34-47, FIGs. 2(a), 2(b), 11.)

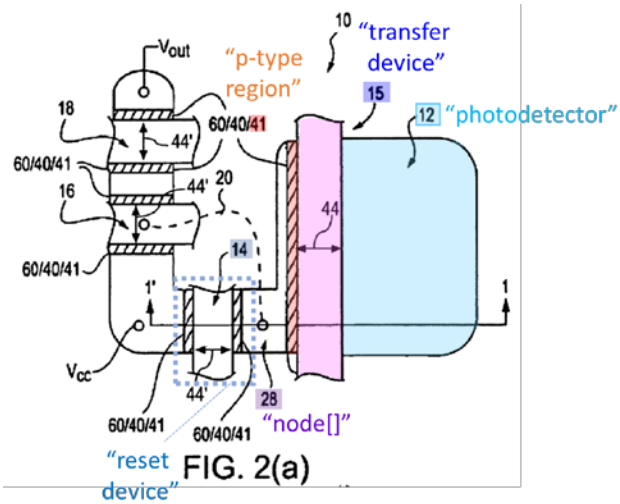


FIG. 2(a)

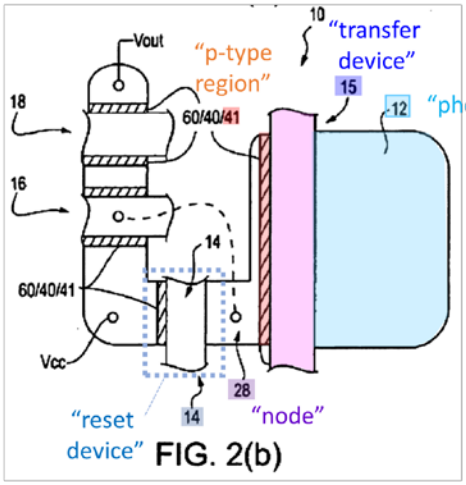


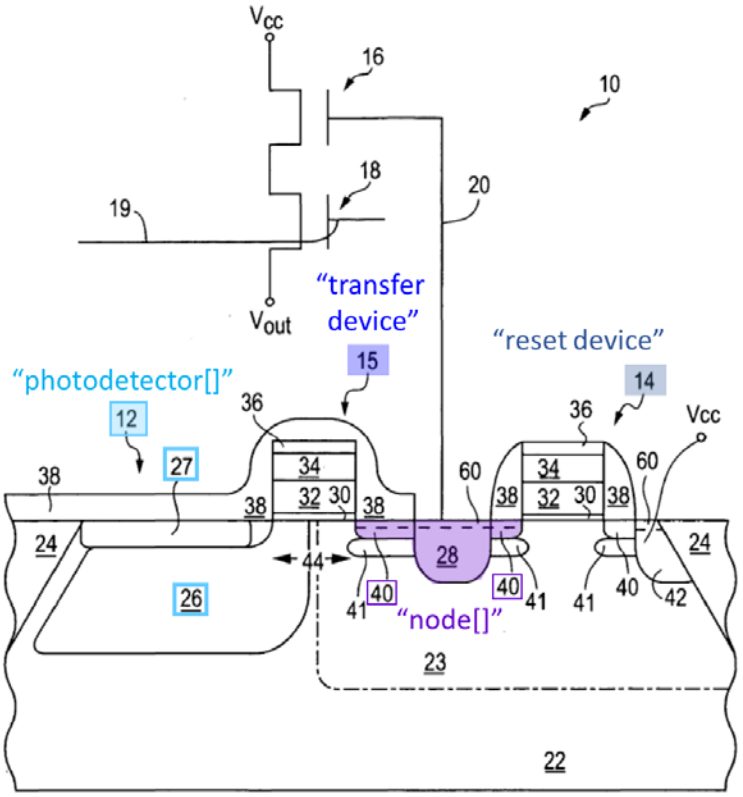
FIG. 2(b)

(Ex. 1008, FIGS. 2(a) and 2(b)(annotated); Ex. 1002, ¶92.) Accordingly, *Rhodes-647* discloses "the plurality of p-type regions has the lateral position stopping short

of the plurality of photodetectors and stopping short of a plurality of reset devices." (Ex. 1002, ¶92.)

f) the plurality of reset devices, wherein each of the plurality of nodes has a corresponding reset device of the plurality of reset devices, and said each of the plurality of nodes is reset when the corresponding reset device is active;

The *Rhodes-647-Kimura* combination discloses or suggests this limitation. (Ex. 1002, ¶¶93-94.) For instance, as shown in figure 1(a) below, each pixel includes a reset transistor 14 connected to the "node" formed by regions 28/40 ("plurality of reset devices, wherein each of the plurality of nodes has a corresponding reset device of the plurality of reset devices"). (Ex. 1008, 4:58-60, 5:2-4.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶93.)

The "node" corresponding to regions 28/40 is reset when the corresponding reset transistor 14 ("reset device") is active. (Ex. 1002, ¶94.) *Rhodes-647* discloses that reset transistor 14 "is connected to a voltage source (Vcc) at a source/drain region 42 for providing a resetting voltage to the floating diffusion region 28." (Ex. 1008, 5:4-6; *see also id.*, 9:15-17.) In order to provide a resetting voltage to the "node" formed by regions 28/40, a POSITA would have understood that reset transistor 14 would be turned on or "activated" such that the voltage Vcc at region 42 is provided to regions 28/40 through reset transistor 14. (Ex. 1002, ¶94; Ex. 1008, 5:4-6, 8:50-53; Ex. 1005,[9] 1:27-37.)

g) row and column circuitry; and

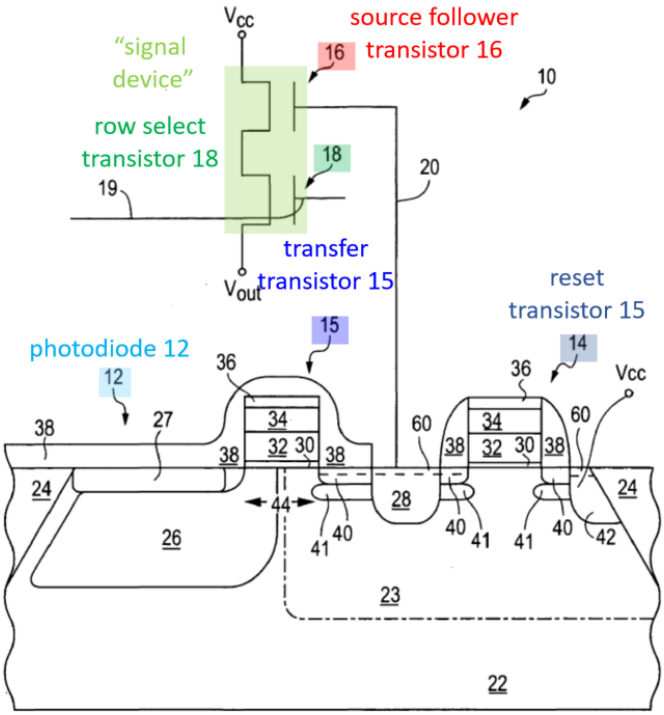
The *Rhodes-647-Kimura* combination discloses or suggests this limitation. (Ex. 1002, ¶95.) For instance, *Rhodes-647* discloses that the pixel array includes "an M×N array of pixels 10 arranged in rows and columns with the pixels 10 of the array accessed using row and column select circuitry." (Ex. 1008, 4:48-53; *see also id.*, 9:36-41.) The pixels in the array can be selectively output by row and column select lines using a combination of row and column circuitry, including, e.g., row driver 210, row address decoder 220, control circuit 250, column driver 260, and

[9] *Rhodes-413* demonstrates the knowledge of a POSITA at the relevant time.

column address decoder 270. (*Id.*, 9:41-60.) Thus, *Rhodes-647* discloses "row and column circuitry." (Ex. 1002, ¶95.)

h) a plurality of signal devices coupling the plurality of nodes to the row and column circuitry.

The *Rhodes-647-Kimura* combination discloses or suggests this limitation. (Ex. 1002, ¶¶96-97.) As shown in figure 1(a) below, regions 28/40 (the "node" for each pixel) are coupled to a source follower transistor 16 that is in turn coupled to a row select transistor 18 that outputs the pixel output onto column line 19. (Ex. 1008, 4:54-57, 8:53-56 (disclosing that "region 28 is electrically connected with the source follower transistor 16 and through transistor 16 with the row select transistor 18 and column line 19.").)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶96.)

Rhodes-647 discloses with reference to Figure 12 that CMOS imager 800 is operated by control circuit 250, controlling address decoders 220 and 270 to select the appropriate row and column lines for pixel readout, i.e., from regions 28/40. (Ex. 1008, 9:36-53.) A combination of row and column circuitry, including, e.g., row driver 210, row address decoder 220, control circuit 250, column driver 260, and column address decoder 270, allows the charge corresponding to each pixels to be selectively output. (*Id.*, 9:41-60.) Because, for each pixel, the charges in the node corresponding to regions 28/40 are read out by row and column circuitry in imager 800 via a source follower transistor 16 and a row select transistor 18 (together forming a "signal device" for each pixel), *Rhodes-647* discloses "a plurality of signal devices coupling the plurality of nodes to the row and column circuitry." (Ex. 1002, ¶97; Ex. 1008, 1:15-18, 4:48-53, 8:60-67.)

2. Claim 2

a) The circuit of claim 1, wherein the control terminal is made of p-type polysilicon.

As discussed above in Section IX.A.1(d)(4), the *Rhodes-647-Kimura* combination discloses or suggests using p-type polysilicon to form the transfer gate electrode, which corresponds to the claimed "control terminal." (Ex. 1006, ¶¶[0131]-[0132], FIG. 8; *Supra* Section IX.A.1(d)(4); Ex. 1002, ¶¶98-99.)

3. Claim 3

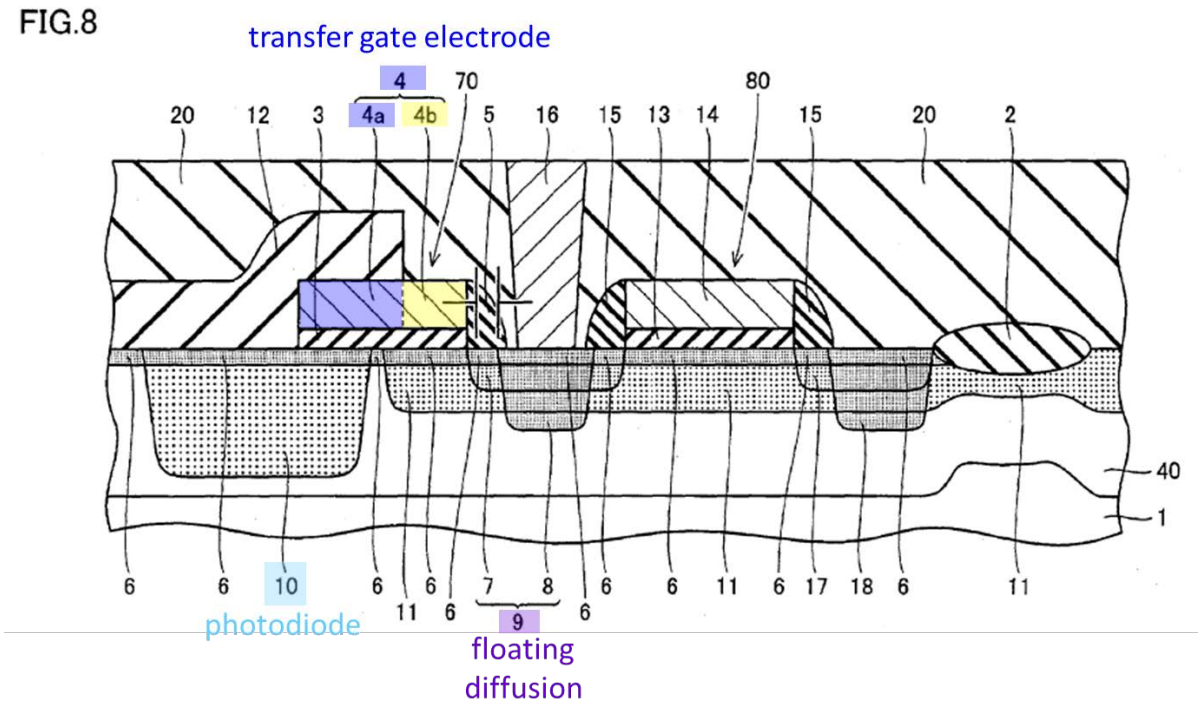
a) The circuit of claim 1, wherein the body has a first Fermi level, the control terminal has a second Fermi level, and a difference between the first Fermi level and the second Fermi level causes the electric field.

The *Rhodes-647-Kimura* combination discloses or suggests this limitation. (Ex. 1002, ¶100.) As discussed above in Section IX.A.1(d)(4), the channel ("body") and gate electrode 32 ("control terminal") in the *Rhodes-647-Kimura* combination have different work functions, where the difference in work functions creates an electric field. (*Supra* Section IX.A.1(d)(4).) Given that the body and the control terminal have different work functions, a POSITA would have understood that they also have different Fermi levels (i.e., a first and second Fermi levels) because the work-function of a material is defined as the amount of energy required to remove an electron from the Fermi level of the material. (Ex. 1002, ¶¶28-37, 100; Ex. 1007, 5:1-4, Ex. 1010, 458-459.) Moreover a POSITA would have understood that the difference between the Fermi level of the channel ("body") and the Fermi level of the graded p-type poly-silicon gate structure ("control terminal") causes the electric field. (Ex. 1002, ¶¶28-37, 100; *see also* Section IX.A.1(d)(4).)

4. Claim 5

a) The circuit of claim 1, wherein a doping of the control terminal is graded in a direction along a channel length in the body.

As discussed above in Section IX.A.1(d)(4), the *Rhodes-647-Kimura* combination discloses or suggests using a p-type transfer gate electrode, where the doping concentration is graded along the channel length of the body, similar to Figure 8 of *Kimura* below. (Ex. 1006, ¶¶[0131]-[0132]; *Supra* Section IX.A.1(d)(4).) The transfer gate electrode has a low p-type concentration region (4b) and a high p-type concentration region (4a). (Ex. 1006, ¶¶[0131]-[0132]; *see also id.*, ¶¶[0134]-[0136]; Ex. 1002, ¶101.)



(Ex. 1006, FIG. 8 (annotated); Ex. 1002, ¶101.)

5. Claim 6

a) The circuit of claim 1, wherein the electric field reduces dark current in the portion of the body by the control terminal.

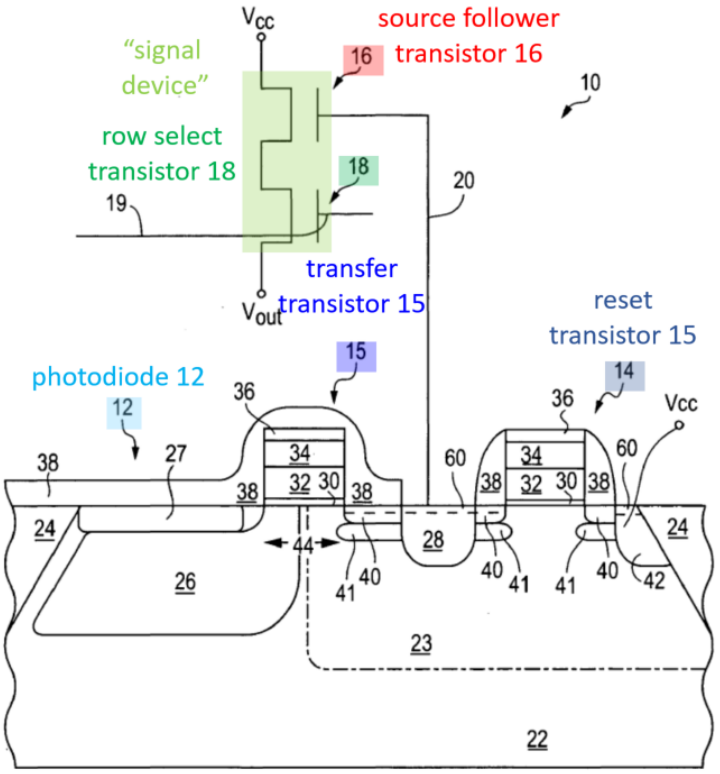
As discussed above in Section IX.A.1(d)(4), the *Rhodes-647-Kimura* combination discloses using p-type polysilicon for the transfer gate electrode, which creates an electric field to repel electrons in the channel region of transfer transistor 15. (*Supra* Section IX.A.1(d)(4).) Given that dark current is caused by the thermal generation of electrons, a POSITA would have understood that a p-type polysilicon gate electrode would reduce the dark current in the transistor channel as the created electric field repels electrons. (Ex. 1002, ¶102; Ex. 1014, 1:21-26.) This is consistent with the '145 patent's disclosure that a p-type polysilicon gate electrode "eliminates dark current." (Ex. 1001, 2:13-17; Ex. 1002, ¶102.)

6. Claim 9

a) The circuit of claim 1, wherein the plurality of signal devices includes a plurality of row select transistors coupled to the row and column circuitry and a plurality of source follower transistors coupled to the plurality of nodes.

As discussed in Section IX.A.1(h), *Rhodes-647* discloses that each pixel includes a "signal device" including source follower transistor 16 and row select transistor 18 ("plurality of signal devices") (*Supra* section IX.A.1(h).) As shown in figure 1(a) below, source follower transistor 16 is coupled to the regions 28/40

("plurality of source follower transistors coupled to the plurality of nodes"), and the row select transistor 18 is coupled to the column line 19, which is coupled to the row and column circuitry, including, e.g., row driver 210, row address decoder 220, control circuit 250, column driver 260, and column address decoder 270. ("plurality of row select transistors coupled to the row and column circuitry"). (*Id.*; Ex. 1002, ¶103; Ex. 1008, 4:54-57, 8:53-56, 9:36-60; *see also id.*, 1:15-18, 4:48-53, 8:60-67.)



(Ex. 1008, FIG. 1(a) (annotated); Ex. 1002, ¶103.)

7. Claim 10

a) The circuit of claim 1, wherein the plurality of photodetectors is a plurality of photodiodes.

As discussed above in Section IX.A.1(b), *Rhodes-647* discloses that each pixel 10 includes photodiode 12 as a photodetector. (*Supra* Section IX.A.1(b); Ex. 1008, 4:30-33; Ex. 1002, ¶104.)

8. Claim 12

a) A computer readable description of an image sensor integrated circuit comprising:

Claim 12 recites "a computer readable medium containing a description of an image sensor integrated circuit comprising" the limitations of claim 1. (*Compare* Ex. 1001, claim 12 *with* claim 1; Ex. 1002, ¶105.) As discussed in Section IX.A.1, the *Rhodes-647-Kimura* combination discloses or suggests the image sensor integrated circuit of claim 1. (*Supra* Section IX.A.1) A POSITA would have understood that the design and manufacture of semiconductor integrated circuits, like the image sensors disclosed in *Rhodes-647* and *Kimura*, is typically performed using computer aided (CAD) tools that result in a design/description of the integrated circuits that would have been understood, in the context of the *Rhodes-647-Kimura* combination, as a "computer readable description of an image sensor integrated circuit." (Ex. 1002, ¶106; Ex. 1009, Abstract, 1:6-7, 4:33-44.) Indeed, the creation of such computer-readable designs has been known in the industry for decades, and

a typical IC designer would be aware of such computer-readable descriptions, capable of creating such a computer-readable description, and motivated to create such a computer-readable description, as using computer aided design tools greatly simplifies the IC design and fabrication process. (Ex. 1002, ¶106.) Accordingly, because the creation of a computer-readable description of the image sensor of the *Rhodes-647-Kimura* combination would have been obvious to a POSITA, the *Rhodes-647-Kimura* combination discloses or suggests all of the features of claim 12 for the same reasons discussed above in Section IX.A.1. (*Supra* section IX.A.1; Ex. 1002, ¶107.)

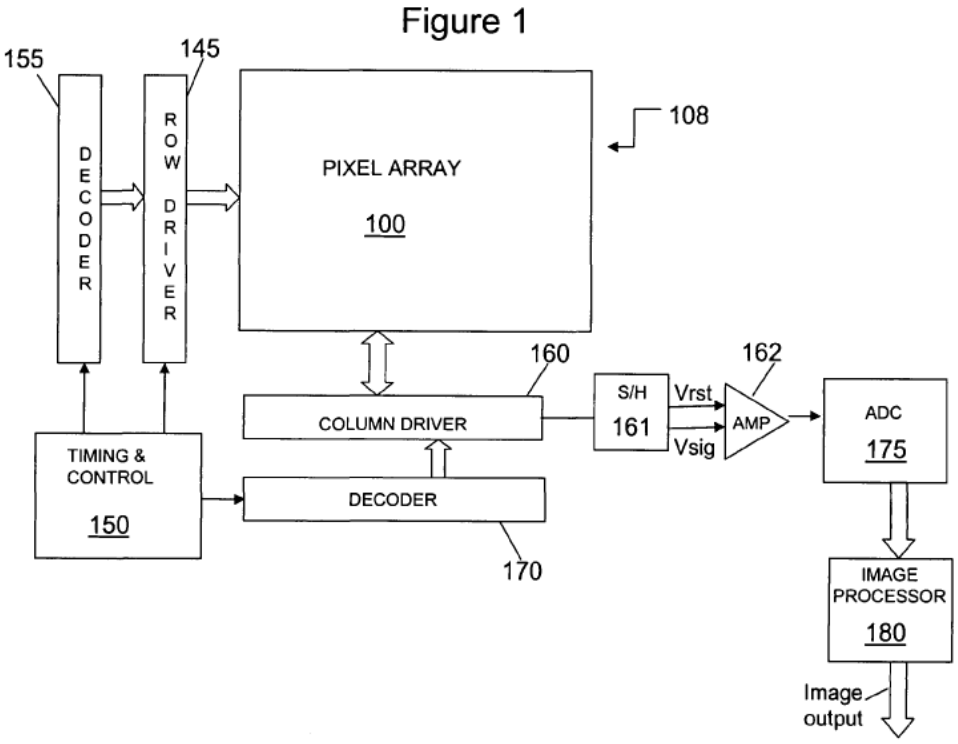
B. Ground 2: *Rhodes-413* in view of *Kimura* and *Rhodes-042* Renders Obvious Claims 1-3, 5, 6, 9, 10, and 12[10]

1. Claim 1

a) Claim 1[a]

To the extent the preamble of claim 1 is limiting, *Rhodes-413* discloses the limitations therein. (Ex. 1002, ¶¶108-111.) *Rhodes-413* discloses an imager device 108 including a pixel array 100 shown in figure 1. (Ex. 1005, 1:38-42, FIG. 1; *see also id.*, 1:12-16; Ex. 1002. ¶109.)

[10] Petitioners do not repeat the language of the challenged claims, which are presented above in Ground 1.

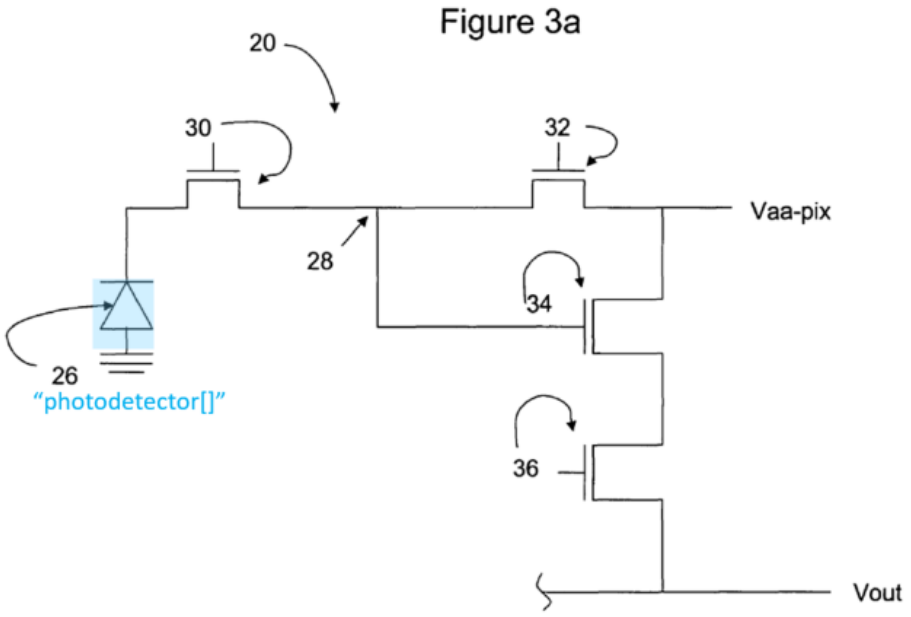


(Ex. 1005, FIG. 1.)

Rhodes-413 discloses that the imager device 108 (including pixel array 100) may be combined with other components in a single integrated circuit. (Ex. 1005, 1:38-65, 8:39-42, FIG. 1; *see also id.*, 4:16-34, FIGS. 2-6 (disclosing various pixel embodiments).) Given that *Rhodes-413* discloses an integrated circuit imager device 108 that includes pixel array 100 that includes a photosensor for each pixel, *Rhodes-413* discloses an "image sensor integrated circuit," as claimed. (Ex. 1002, ¶¶110-111; *infra* Sections IX.B.1(b)-(h).)

b) Claim 1[b]

Rhodes-413 discloses this limitation. (Ex. 1002, ¶¶112-113.) Each pixel in array 100 may be 4T pixel like that shown in figure 3a below. (Ex. 1005, 2:27-28, 8:13-15; FIGs. 1, 3a.) Each 4T pixel in the array includes a photosensor ("a plurality of photodetectors") that converts photons to charges ("generating electrons excited by incident photons"). (Ex. 1005, 1:12-16, 1:27-29, 2:31 ("A photosensor 26 converts incident light into charge."), 2:41-43, 5:7-12; Ex. 1002, ¶¶112-113.)

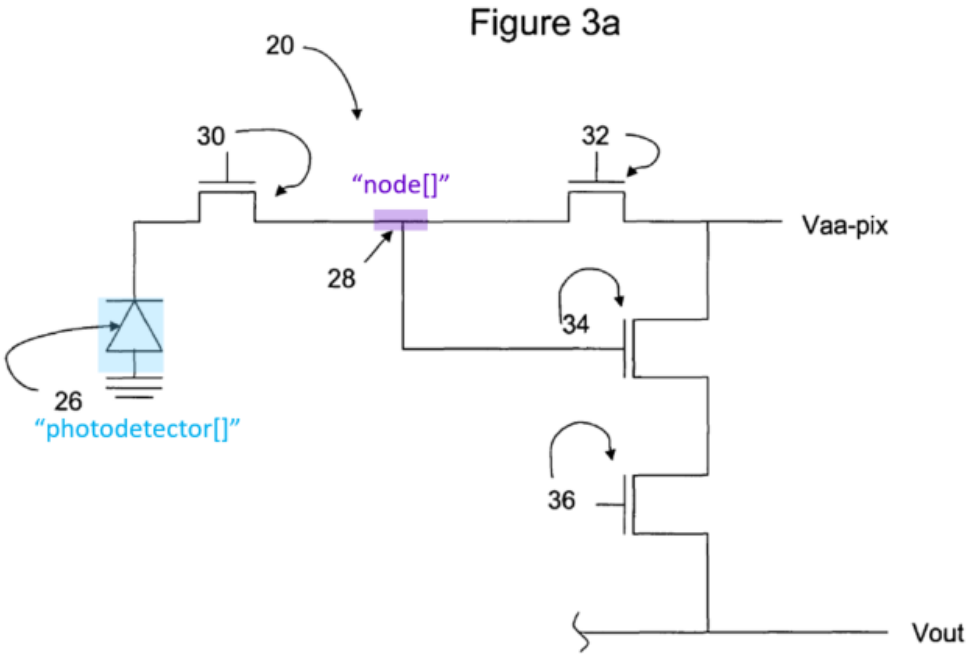


(*Id.*, FIG. 3a (annotated); Ex. 1002, ¶112.)

c) Claim 1[c]

Rhodes-413 discloses this limitation. (Ex. 1002, ¶114.) Each of the 4T pixels in array 100 includes a "floating diffusion region 28" ("node") that "receives charges from the photosensor 26 through the transfer gate 30 (when activated)." (Ex. 1005,

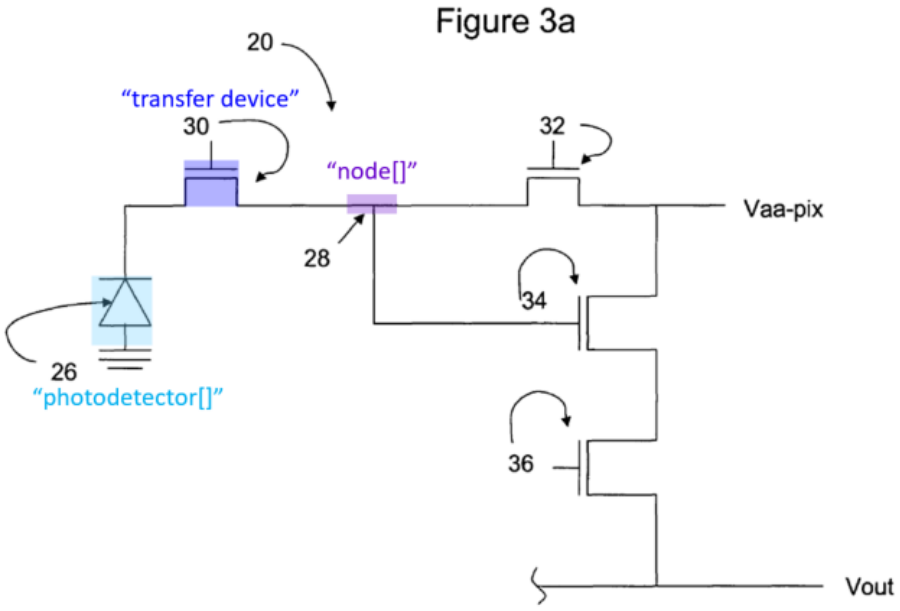
2:31-35; *see also id.*, 1:27-30.) The "node" 28 for each 4T pixel is highlighted in figure 3a of *Rhodes-413* below.



(*Id.*, FIG. 6 (annotated); Ex. 1002, ¶114.)

d) Claim 1[d]

Rhodes-413 discloses this limitation. (Ex. 1002, ¶¶115-116.) As shown in figure 3a below, each 4T pixel includes a transfer gate 30 ("plurality of transfer devices"), where when the transfer gate 30 is activated, charges from photosensor 26 are transferred to region 28 ("controlling a transfer of the electrons from said each of the plurality of photodetectors to the corresponding node"). (Ex. 1005, 2:31-35; *see also id.*, 1:21-24; Ex. 1002, ¶115.)



(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶115.)

A POSITA would have understood that transfer gate 30 is a CMOS transistor that can be turned on (i.e., activated) or off (i.e., deactivated) to control the flow of charges ("electrons") from photosensor 26 ("photodetector") to region 28 ("node"). (Ex. 1002, ¶116; Ex. 1005, 2:27-30.) Thus, *Rhodes-413* discloses this limitation. (*Id.*, ¶116; *infra* Sections IX.A.1(d)(1)-(4).)

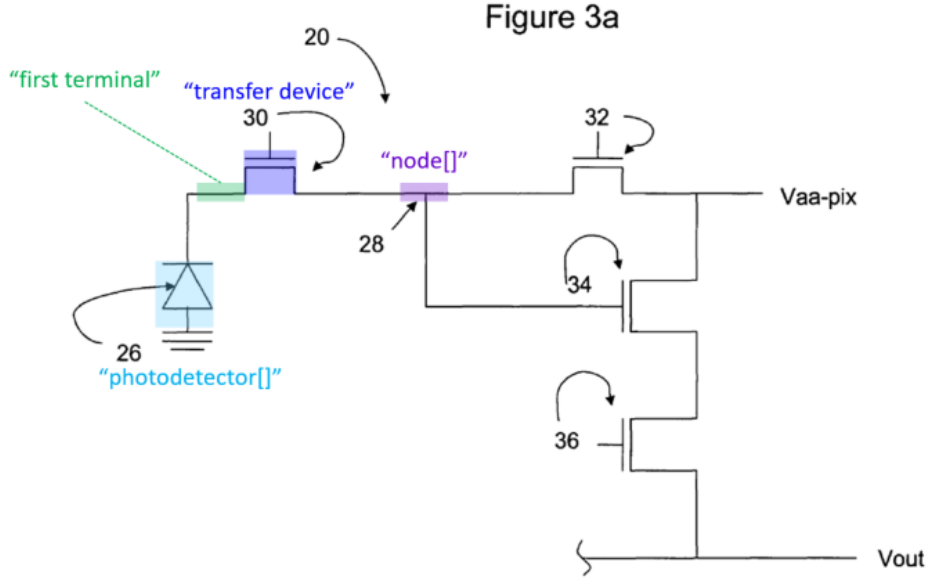
(1) Claim 1[d.1]

Rhodes-413 discloses this limitation. (Ex. 1002, ¶¶117-118.) A POSITA would have understood that transfer gate 30, which is a CMOS transistor, includes source, drain, and gate terminals, and a channel, where charge carriers flow from the

source to the drain through the channel when a sufficient gate bias is applied. (Ex. 1002, ¶¶23-27, 117; Ex. 1010,[11] FIG. 11.35, 484-485.)

As shown in figure 3a below, a first terminal of transfer gate 30 ("transfer device") is coupled to photosensor 26 ("first terminal coupled to one of the plurality of photodetectors"), where the transfer gate facilitates charge transfer. (Ex. 1005, 2:31-33, FIG. 3a; Ex. 1002, ¶119.)

Figure 3a



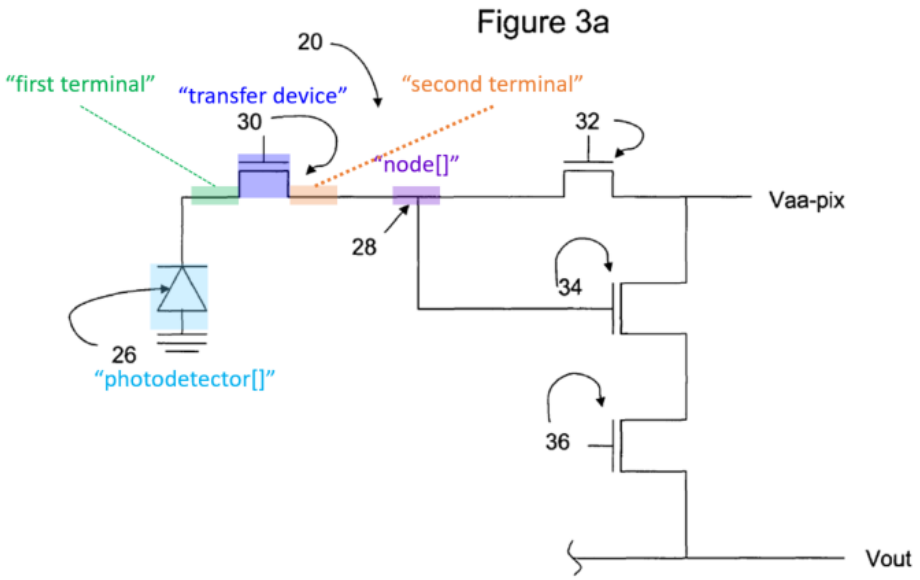
(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶118.)

(2) Claim 1[d.2]

Rhodes-413 discloses this limitation. (Ex. 1002, ¶119.) As shown in annotated figure 3a below, a second terminal of transfer gate 30 ("transfer device")

[11] *Neamen* demonstrates the knowledge of a POSITA at the relevant time.

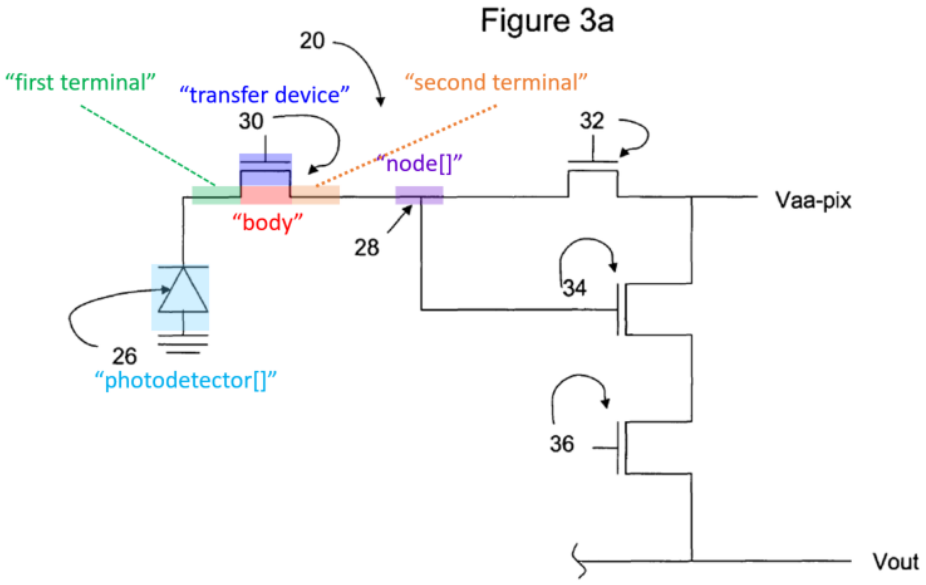
is coupled to region 28 ("node[]") ("second terminal coupled to one of the plurality of nodes") to facilitate charge transfer. (Ex. 1005, 2:31-33, FIG. 3a; Ex. 1002, ¶119.)



(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶119.)

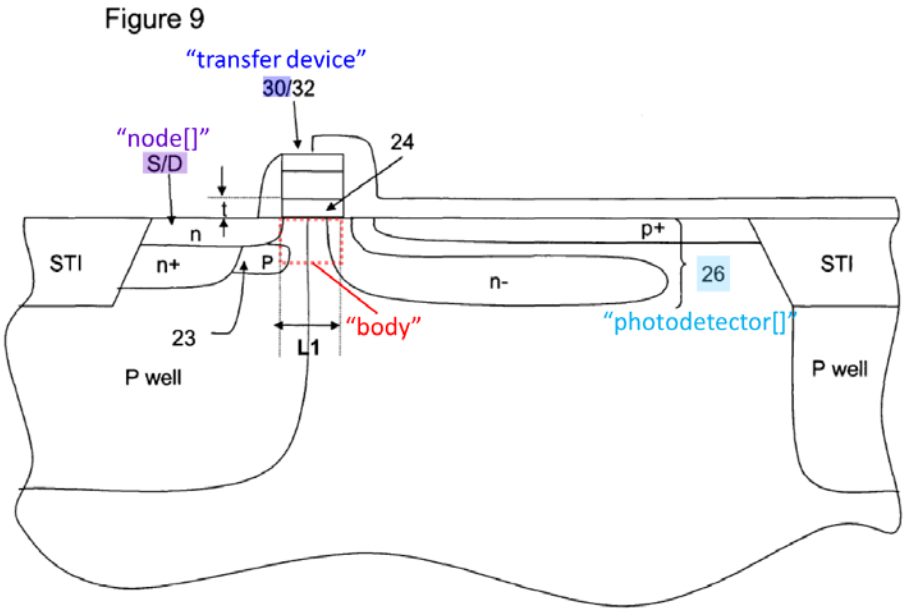
(3) Claim 1[d.3]

Rhodes-413 discloses this limitation. (Ex. 1002, ¶¶120-123.) As shown in annotated figure 3a below, transfer gate 30 includes a channel between the two terminals ("a body between the first terminal and the second terminal"). (Ex. 1005, 6:54-57, 7:10-26, FIGs. 3a, 9; Ex. 1002, ¶120.)



(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶120.)

Figure 9 of *Rhodes-413* shows "cross section of a typical pixel having features to minimize leakage, according to prior art techniques." (Ex. 1005, 7:6-7, FIG. 9.)



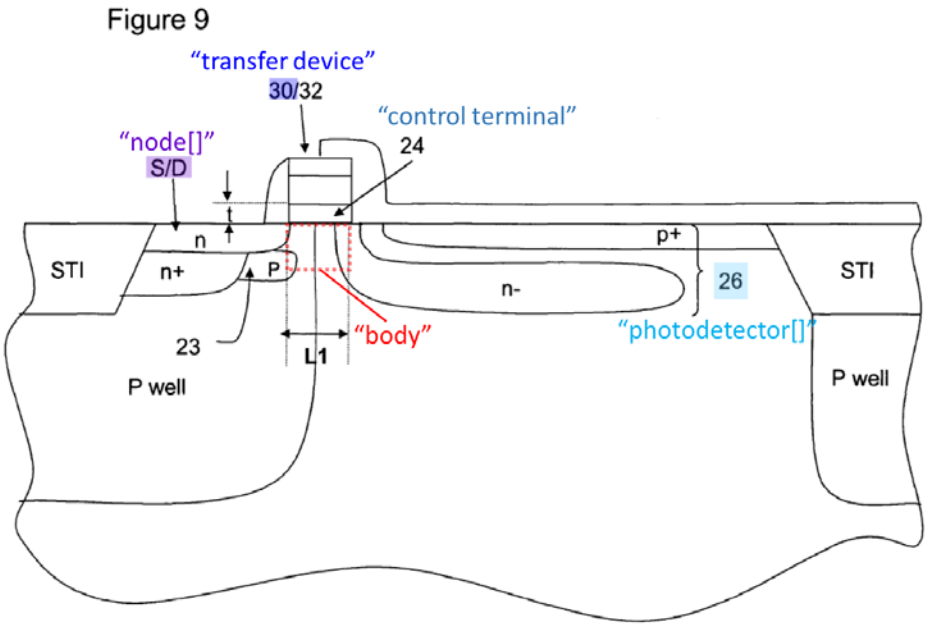
(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶121.)

Rhodes-413 further discloses that the transistor shown in figure 9 can be either a reset gate 32 or a transfer gate 30. (Ex. 1005, 7:8-12.) Therefore, a POSITA would have understood that *Rhodes-413* discloses that the prior art cross section disclosed in figure 9 is applicable to the prior art 4T pixel shown in figure 3a, and more specifically to the transfer gate 30 shown in annotated figure 3a above. (Ex. 1002, ¶122.) In other words, a POSITA would have understood that *Rhodes-413* discloses that one implementation of the 4T pixel in figure 3a would include components such as the transfer gate 30, photodetector 26, and node 28 that are implemented according to the cross section illustrated in figure 9. (*Id*.; Ex. 1005, 7:6-26, FIG. 9.)

Annotated figure 9 above shows the "body" of the transfer gate 30 in a manner consistent with figure 3a of *Rhodes-413* where transfer gate 30 connects photoconversion device 26 and region 28. Accordingly, *Rhodes-413* discloses "a body between the first terminal and the second terminal" for each transfer gate in the array of pixels. (Ex. 1002, ¶123.)

(4) Claim 1[d.4]

Rhodes-413 in view of *Kimura* discloses or suggests this limitation. (Ex. 1002, ¶¶124-136.) For instance, as shown in figure 9 below, transfer gate 30 ("transfer device") includes a gate electrode 24 ("control terminal"). (Ex. 1005, 7:6-38.)



(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶124.) Transfer device 30 in figures 3a and 9 is a CMOS transistor (Ex. 1005, 2:27-28), and a POSITA would have understood that gate 24 is electrically "coupled to" the channel ("body") of transfer device 430 (through the gate oxide) in a manner consistent with the limited disclosure of the '145 patent. (Ex. 1005, 2:34-35, 6:53-57, 7:33-36 (describing the analogous region 24' in figure 10 as 'the gate 24'").) For example, just as is the case with other CMOS transistors, the bias applied to the gate 24 controls the conductivity of the channel underlying the gate. (Ex. 1002, ¶¶23-27, 124; *see also* Ex. 1010, 450-455, 484-489.)

By applying a voltage exceeding the threshold voltage of transfer device 30 to its gate 24 ("control voltage of sufficient value applied to the control terminal"), transfer device 30 may be activated or turned "on", thereby causing "the transfer of the electrons occurs through the body between the first terminal and the second

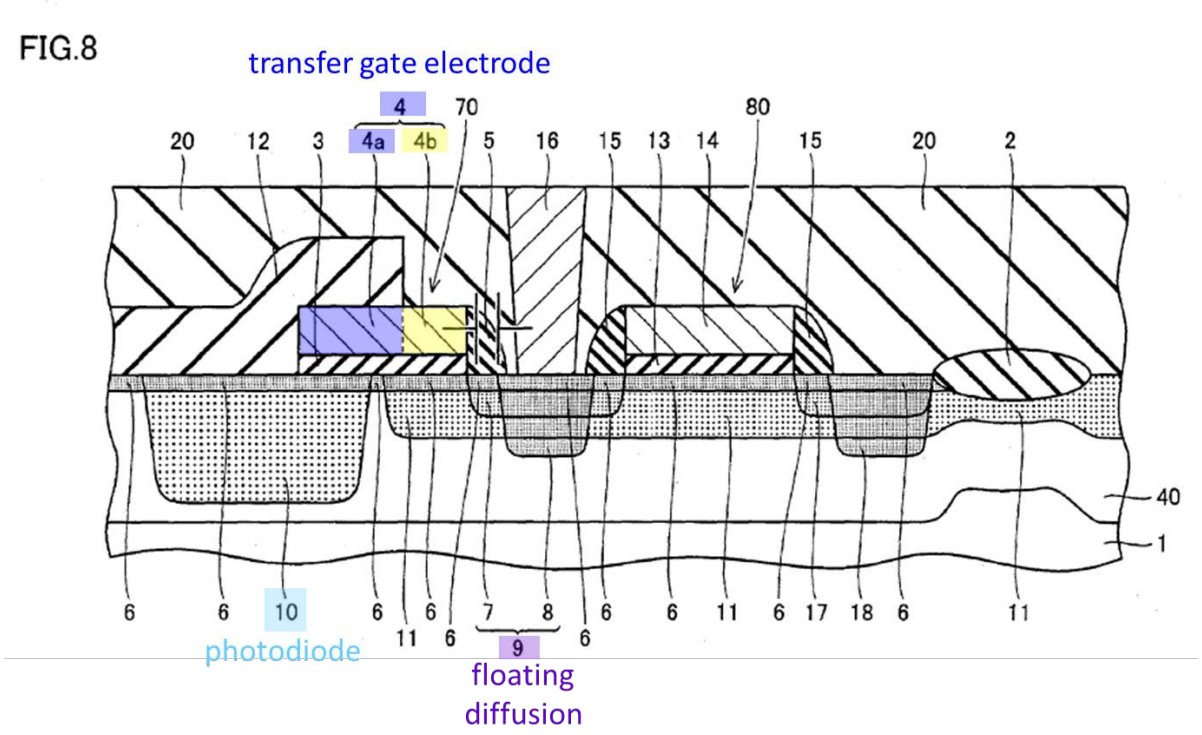
terminal in response to a control voltage of sufficient value applied to the control terminal". (Ex. 1002, ¶¶23-27, 125; *see also* Ex. 1010, 484-489; *see also* Ex. 1005, 1:22-24, 2:31-35, 6:52-53.)

If the voltage on gate 24 is less than transistor 30's threshold voltage, transistor 30 is not activated, and charges ("electrons") are not able to flow through the channel ("body") between the two terminals. (Ex. 1002, ¶126; Ex. 1010, 487.) Therefore, *Rhodes-413* discloses that "in an absence of the control voltage" (e.g., when not applying a voltage equal to or greater than the threshold voltage to gate 24), transfer device 30 is not activated and is in the "off-state." (Ex. 1002, ¶126; *see also* Ex. 1005, 4:3.)

Rhodes-413 does not expressly disclose that in an absence of the control voltage "the control terminal creates an electric field tending to repel the electrons from a portion of the body by the control terminal." Nevertheless, a POSITA would have found it obvious to implement such a feature for each of the pixels of *Rhodes-413* in view of *Kimura*. (Ex. 1002, ¶127.)

As shown in figure 8 below, *Kimura*, like *Rhodes-413*, discloses an imaging device that includes a photodiode, a floating diffusion region, and a charge transfer transistor that controls charge transfer. (Ex. 1006, ¶¶[0128]-[0137]; FIG. 8; Ex. 1002, ¶128.) Therefore, a POSITA would have reason to look to *Kimura* when

implementing as imaging device like that disclosed in *Rhodes-413*. (Ex. 1002, ¶128.)



(Ex. 1006, FIG. 8 (annotated); Ex. 1002, ¶128.)

As discussed above in Section IX.A.1(d)(4) *Kimura* discloses a graded p-type polysilicon gate for a transfer transistor. (*Supra* section IX.A.1(d)(4); Ex. 1002, ¶129.)

Rhodes-413 does not expressly disclose the formation of, or material making up, gate 24 for the transfer device of the 4T pixel shown in figure 3a as implemented consistent with the cross-section shown in figure 9. As such, a POSITA would have looked to other references, like *Kimura*, that disclose details regarding the formation

of such a transfer device gate. (Ex. 1002, ¶130; *see generally* Ex. 1005.) Having looked to *Kimura*, a POSITA would have found it obvious to include a graded p-type poly-silicon gate structure, like that disclosed by *Kimura*, when implementing transfer transistors for an imaging device as disclosed in *Rhodes-413*. (Ex. 1002, ¶130.) A POSITA would have been motivated to do so for the same reasons discussed above with respect to the *Rhodes-647-Kimura* combination discussed above in Section IX.A.1(d)(4). (*Supra* section IX.A.1(d)(4); Ex. 1002, ¶¶130-132.) For example, a POSITA would have found it beneficial to implement a graded p-type poly-silicon gate structure, like that disclosed in *Kimura*, in an imaging device as disclosed by *Rhodes-413* in order to suppress charge trapping and reduce parasitic capacitance as disclosed by *Kimura*. (*Supra* section IX.A.1(d)(4); Ex. 1002, ¶¶130-132.) Moreover, for the same reasons discussed above for the *Rhodes-647-Kimura* combination, a POSITA would have a reasonable expectation of success in implementing a graded p-type poly-silicon gate structure in the *Rhodes-413* image sensor. (*Supra* section IX.A.1(d)(4); Ex. 1002, ¶¶130-132.) For example, a POSITA would have had a reasonable expectation of success in implementing a graded p-type polysilicon gate structure since such polysilicon gate structures were well-known for semiconductor devices. (Ex. 1002, ¶¶130-132; Ex. 1007, 8:1-13 (disclosing that forming a p-type poly-silicon transfer gate is "known in the art"); *KSR*, 550 U.S. at 416 (2007))

As discussed above, a POSITA would have understood that such a graded p-type poly-silicon gate would "create an electric field tending to repel the electrons from a portion of the body by the control terminal," when not applying the threshold voltage to such a p-type poly-silicon gate electrode ("in an absence of the control voltage the control terminal") implemented in the *Rhodes-413-Kimura* combination. (*Supra* section IX.A.1(d)(4); Ex. 1002, ¶¶28-34, 133-136.)

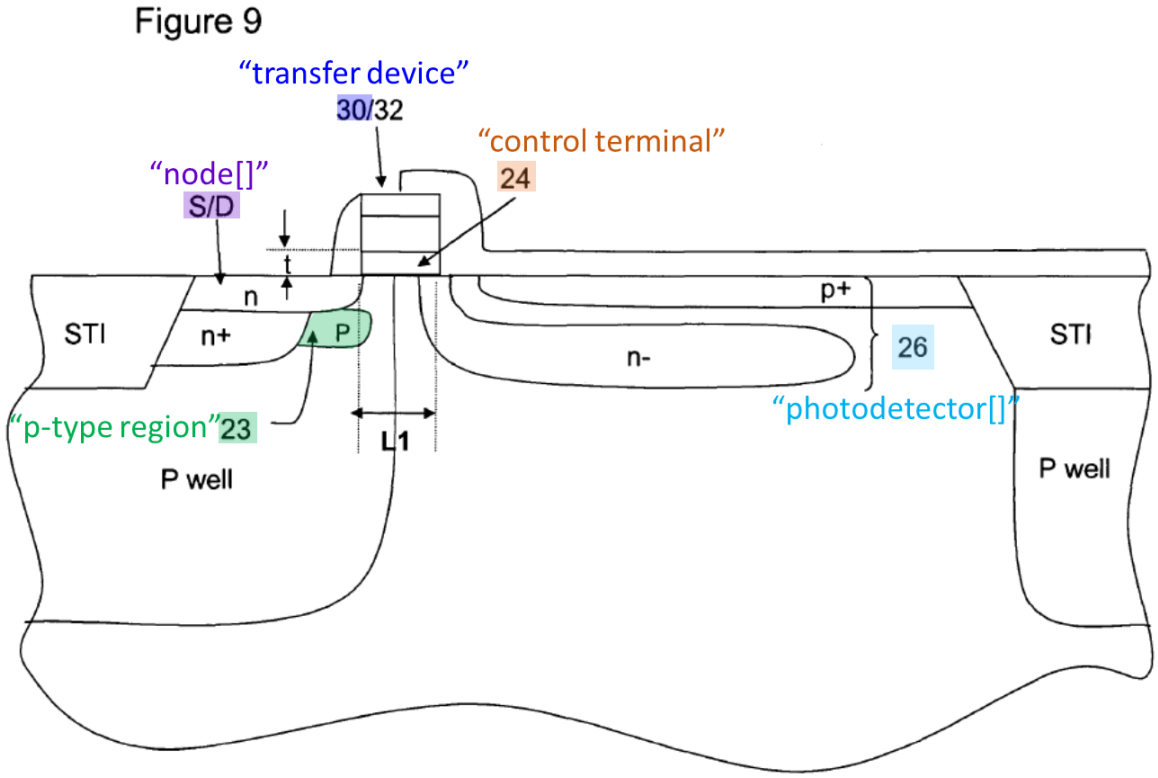
e) Claim 1[e]

The *Rhodes-413-Kimura* combination discloses or suggests this limitation. For clarity, this is discussed below in two parts. (Ex. 1002, ¶¶137-158.)

(1) Claim 1[e.1]

Rhodes-413 discloses that "doping profile of a transfer gate of a conventional pixel may only include a 'punch-through' protection on one side, to minimize leakage across the transistor and maintain control of its channel." (Ex. 1005, 6:54-57; *see also id.*, 6:60-63.) A POSITA would have understood that Figure 9 of *Rhodes-413* discloses a conventional pixel that only has a "punch-through protection implant 23" on one side. (Ex. 1002, ¶138; Ex. 1005, 4:40 ("FIG. 9 is a cross section of a pixel cell of prior art"), 7:6-7, FIG. 9.) Moreover, as discussed above in Section IX.B.1.d(3), a POSITA would have understood that *Rhodes-413* discloses that the conventional 4T pixel in figure 3a would include components such as the transfer

gate 30, photodetector 26, and node 28 that are implemented according to the cross section illustrated in figure 9. (*Supra* Section IX.B.1.d(3); Ex. 1002, ¶138.)



(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶138.)

Rhodes-413 discloses that such a punch-through protection implant 23 (also known as a "halo implant") is a boron implant. (Ex. 1005, 7:8-9.) Boron is a p-type dopant, and a POSITA would have understood that halo implant 23 is a "p-type region" as recited in claim 1. (Ex. 1002, ¶139; Ex. 1008, 5:1 (p-type, e.g., boron).)

Because the p-type halo implant 23 is deposited within a p-type well, a POSITA would have understood that the region where halo implant 23 is positioned has a stronger p-type concentration than that of the rest of the well. (Ex. 1002, ¶140;

supra Section IX.A.1(e)(1) (demonstrating the a similar halo implant in a similar pixel structure of *Rhodes-647*[12] has a higher p-type concentration than the p-well in which it is formed).)

Additionally, given that the p-type halo implant 23 is "designed to create barriers to change leakage across the channel" (Ex. 1005, 7:6-14), a POSITA would have understood that the halo implant 23 has a stronger doping concentration than the p-type well in order to form such a barrier (Ex. 1002, ¶141; Ex. 1011, 423, 834-835; Ex. 1012, 238-240 (describing that halo implantation "raises the doping concentration…").)[13] Accordingly, *Rhodes-413* discloses "a plurality of p-type regions having a concentration stronger than a background p-type concentration of the plurality of transfer devices." (Ex. 1002, ¶141.)

Rhodes-413 also discloses that the halo implant is implemented "to minimize leakage across the transistor and maintain control of its channel." (Ex. 1005, 6:54-57.) Additionally, as discussed above in Sections IX.B.1(d) and (d)(3), *Rhodes-413* discloses that transfer gate 30 controls the transfer of electrons from the photosensor 26 to the floating diffusion region 26 through the channel of transfer gate 30. (*Supra*

[12] *Rhodes-647* demonstrates the knowledge of a POSITA at the relevant time.

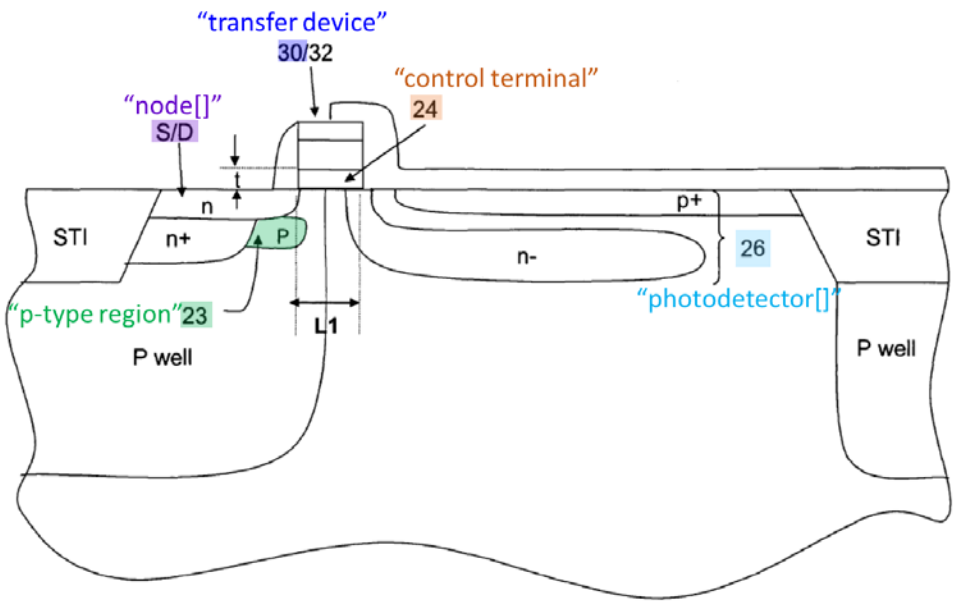
[13] *Wolf-V1* and *Wolf-V3* demonstrate the knowledge of a POSITA at the relevant time.

sections IX.B.1(d),(d)(3); *see also* Ex. 1005, 1:21-24, 2:27-28, 2:31-35, 7:6-26.) Accordingly, a POSITA would have understood that *Rhodes-413* discloses "the plurality of p-type regions controlling the transfer of electrons from a photodetector of the plurality of photodetectors to the corresponding node of the photodetector." (Ex. 1002, ¶142; Ex. 1011, 423, 834-835; Ex. 1012, 232, 238-240.)

(2) Claim 1[e.2]

As shown in figure 9 below, *Rhodes-413* discloses that halo implant 23 ("p-type region[]") has a lateral position that is partly under the "node" as annotated in figure 9. (Ex. 1005, FIG. 9; Ex. 1002, ¶143; *see also id.*, ¶¶144-158.)

Figure 9

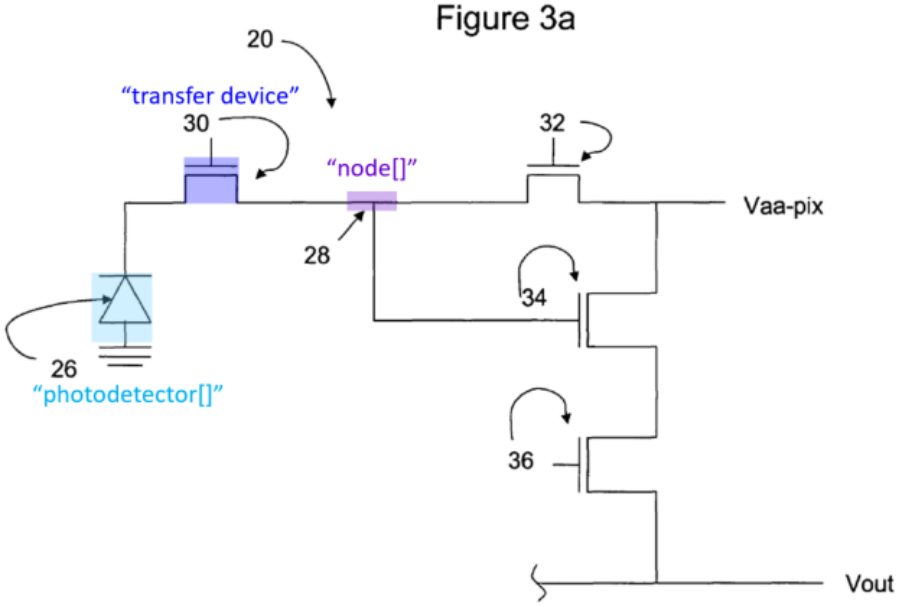


(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶143.)

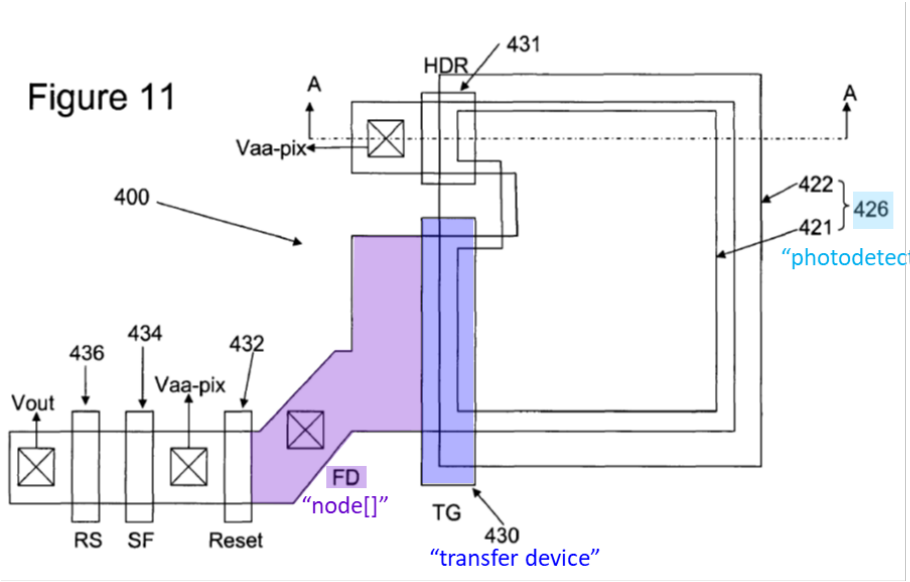
A POSITA would have understood that the n-type region denoted as "S/D" and highlighted as the "node" corresponds to floating diffusion 28 (given that the

S/D is on the opposite side of the transfer gate 24 from photosensor 26). (Ex. 1002, ¶144; Ex. 1005, 7:6-26.) Such an understanding is supported by figure 3a as well as figure 11, which illustrates a plan view of a pixel cell 400 consistent with architecture shown in figure 3a with the addition of a high dynamic range (HDR) transistor 431. (Ex. 1002, ¶144; Ex. 1005, 7:46-60.)

Figure 3a



(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶144.)



(Ex. 1005, FIG. 11 (annotated); Ex. 1002, ¶144.) Thus, *Rhodes-413* discloses "the plurality of p-type regions has the lateral position at least partly under the corresponding node." (Ex. 1002, ¶144.)

Furthermore, as shown in Figure 9 above, *Rhodes-413* discloses and/or suggests that halo implant 23 ("p-type region[]") is positioned only partly under gate 24, which is indicated in part by the vertical dashed lines extending from the lateral boundaries of gate 24. (Ex. 1005, FIG. 9; Ex. 1002, ¶145.)

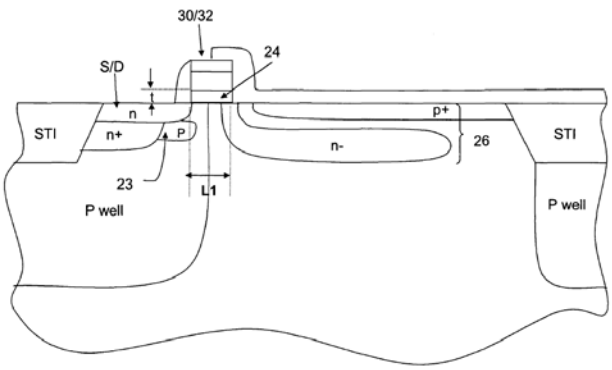
To the extent that Pictos argues or the Board finds that the *Rhodes-413* does not explicitly disclose that halo implant 23 has a lateral position that is only partly under the transfer gate 30 highlighted in figure 9 above, *Rhodes-042* discloses forming a halo implant using a directional implant that results in a halo implant that is only partly under the transfer gate, and it would have been obvious to combine *Rhodes-042* with *Rhodes-413* and *Kimura* such that the *Rhodes-413-Kimura-*

Rhodes-042 combination forms halo implant 23 to have a lateral position that is only partly under the transfer gate 30. (Ex. 1002, ¶145.)

Rhodes-042, like *Rhodes-413* and *Kimura*, discloses an imaging device including a pixel array where each pixel includes a photodiode, a floating diffusion region, and a charge transfer transistor that controls charge transfer. (Ex. 1013, 1:14, 1:29-38, 2:11-31, FIG. 2; Ex. 1002, ¶146.) Indeed, *Rhodes-042* is specifically referenced in *Rhodes-413*. (Ex. 1005, 3:50-55 (citing to Pat. App. No. 10/881,525), 7:60-62.) Therefore, a POSITA implementing an imaging device using pixel structures shown in figures 3a and 9 of *Rhodes-413* would have reason to look to *Rhodes-042*. (Ex. 1002, ¶146.)

As is apparent from comparing figure 9 of *Rhodes-413* (below left) with figure 5c of *Rhodes-042* (below right), both *Rhodes-413* and *Rhodes-042* disclose a transistor (e.g. transfer gate 30) that includes a p-type punch-through protection implant 23. (Ex. 1013, 7:3-15; Ex. 1002, ¶147.)

Figure 9



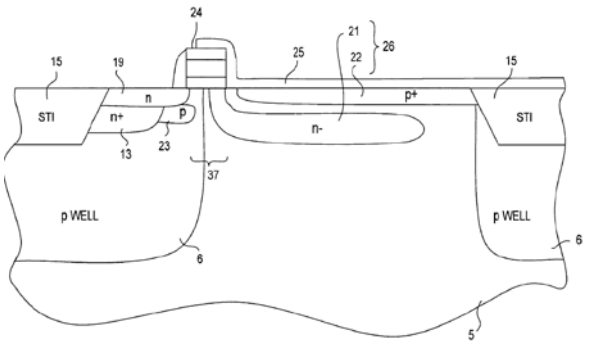


FIG. 5c

(*Compare* Ex. 1005, FIG. 9 *with* Ex. 1013, FIG. 5c; Ex. 1002, ¶147.)

Rhodes-042 discloses that the HDR transistor 24 shown in figure 5c can have the same doping profile as the transfer gate 30 for the same pixel cell. (Ex. 1013, 6:4-7, 7:11-15.) *Rhodes-042* discloses that "[t]he doping profile[] of the transfer gate 30…may include 'punch-through' protection implant on one side…which allows the transistors to maintain better control of their channels." (*Id*., 6:12-16.) Therefore, both *Rhodes-413* and *Rhodes-042* disclose transfer gates 30 that include halo ("punch-through") protection implants 23 shown in figures 9 and 5c of those respective references above. (Ex. 1002, ¶148.)

Rhodes-413 does not explicitly explain how the halo implant 23 is formed in transfer gate 30. *Rhodes-042*, however, discloses the various steps for forming implant 23 in conjunction with a transfer gate, and a POSITA would have found it obvious to form halo implant 23 in *Rhodes-413* based on the disclosure of *Rhodes-042*. (Ex. 1002, ¶149.) As discussed in more detail below, when halo implant 23 of *Rhodes-413* is formed based on *Rhodes-042*, halo implant 23 ("p-type region") has a lateral position extending only partially under transfer gate 30. As such, the *Rhodes-413-Kimura-Rhodes-042* discloses or suggests the "p-type regions has a lateral position only partly under the control terminal of a transfer device of the plurality of transfer devices." (*Id*.)

Figures 6-8 and 11-14 of *Rhodes-042* illustrate the formation of transistor 24 shown in figure 5c of *Rhodes-042* above, which, as discussed above, also corresponds to the doping profile of transfer gate 30. (Ex. 1013, 6:4-7, 7:11-15, 8:7-12.) Figure 11 of *Rhodes-042*, replicated below, shows a "halo angled implant of a first conductivity type (e.g., p-type) to implant a halo implanted region 35 below the charge collection region 19, as illustrated on FIG. 12." (*Id*., 8:18-21; Ex. 1002, ¶¶150-151.)

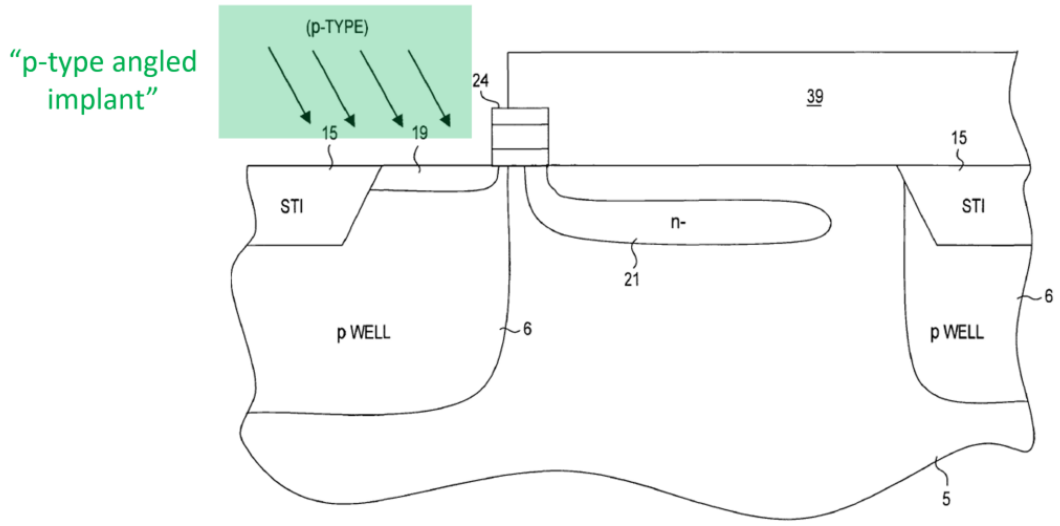


FIG. 11

(Ex. 1013, FIG. 11 (annotated); Ex. 1002, ¶151.)

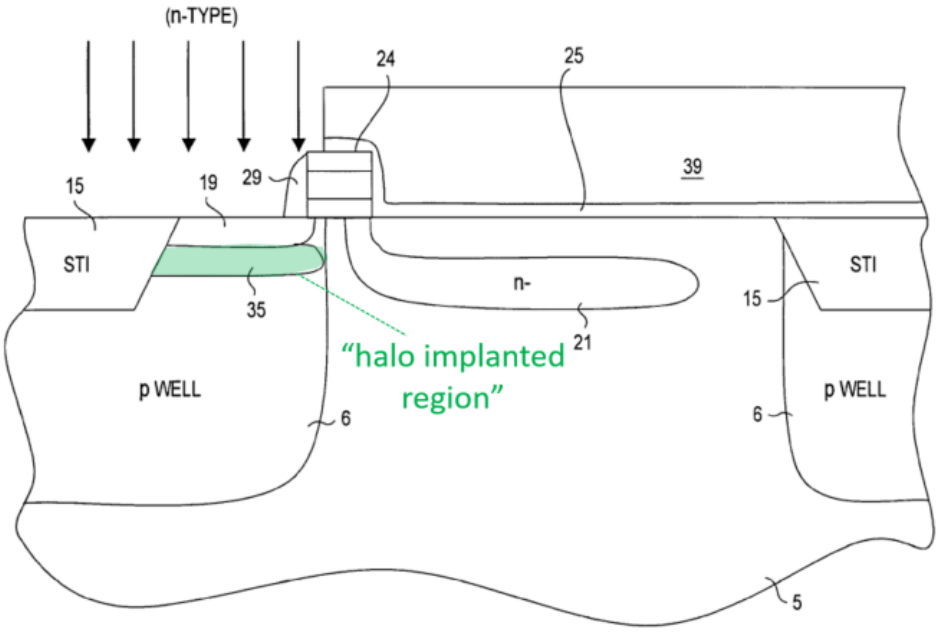


FIG. 12

(Ex. 1013, FIG. 12 (annotated); Ex. 1002, ¶151.)

Consistent with the disclosure of the halo implant in *Rhodes*-413, the halo implant in *Rhodes-042* can be a boron implant. (Ex. 1013, 8:21-23.) A POSITA would have understood from the disclosure of *Rhodes-042* that the implant is angled in order to allow the doping material to penetrate under a portion of the transfer gate, which is supported by the figures in both *Rhodes-042* and *Rhodes-413*. (Ex. 1002, ¶152.) Indeed, the structure shown in both *Rhodes-042* and *Rhodes-413* is similar to that discussed above for *Rhodes-647* in Section IX.A.1(e)(2), which is explicitly disclosed as extending under a portion of the gate and formed using an "angled" implant that is consistent with the angled implantation described in *Rhodes-042*.

(Ex. 1008[14], FIG. 1(a), 5:32-34 ("The halo implant region 41 associated with the active area extension region 40 **extends under a portion of the transistor 15 gate**."), 7:41-48 (implant "**angled to penetrate partially below**" the gate), 12:20-21; Ex. 1002, ¶152.)

Rhodes-042 discloses that a sidewall spacer 29 is formed after the halo implant, and then an n-type implant (shown in figure 12 above) is used to form drain region 13 shown in annotated figure 13 below. (Ex. 1013, 8:32-41; Ex. 1002, ¶153.)

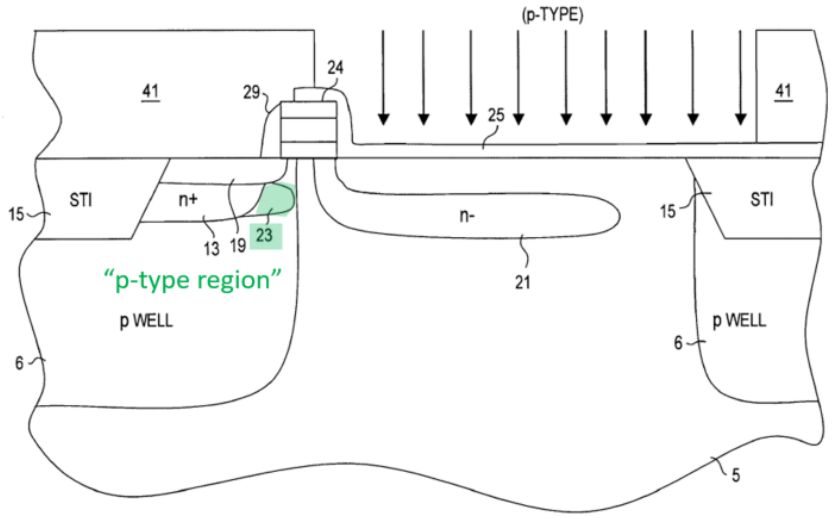


FIG. 13

(Ex. 1013, FIG. 13 (annotated); Ex. 1002, ¶153.)

The n-type implant is vertical (not angled) and uses the sidewall spacer to align the implant, "convert[ing] a portion of the p-type halo implant region 35 to a

[14] *Rhodes-647* demonstrates the knowledge of a POSITA at the relevant time.

n-type portion, leaving only a p-type hole which is the punch-through protection implant 23." (Ex. 1013, 8:37-41.) Therefore, *Rhodes-042* discloses formation of the halo implant 23 using an angled implant such that only a portion of the halo implant is under a portion of the transfer gate 30. (Ex. 1002, ¶154.)

Rhodes-413 does not expressly explain how to form the halo implant 23 in its figure 9 structure discussed above. As such, a POSITA would have looked to other references, like *Rhodes-042*, which discloses how to form such a halo implant. (Ex. 1002, ¶155.) Having looked to *Rhodes-042*, a POSITA would have found it obvious to form the halo implant 23 in *Rhodes-413* using an angled implant, like that disclosed by *Rhodes-042*. (Ex. 1002, ¶155.) A POSITA would have been motivated to do so because *Rhodes-042* and *Rhodes-413* disclose similar structures and *Rhodes-042* teaches details regarding formation of the halo implant 23 that are not disclosed by *Rhodes-413* and that help avoid punchthrough. (Ex. 1002, ¶155; Ex. 1005, 6:54-63 ("a transfer gate of a conventional pixel may only include a 'punch-through' protection implant on one side, to minimize leakage across the transistor and maintain control of its channel."), 7:6-14 (a halo "punch-through protection implant 23"); Ex. 1013, 6:12-23 ("The doping profiles of the transfer gate 30…may include a 'punch-through' protection implant on one side…which allows the transistors to maintain better control of their channels.").)

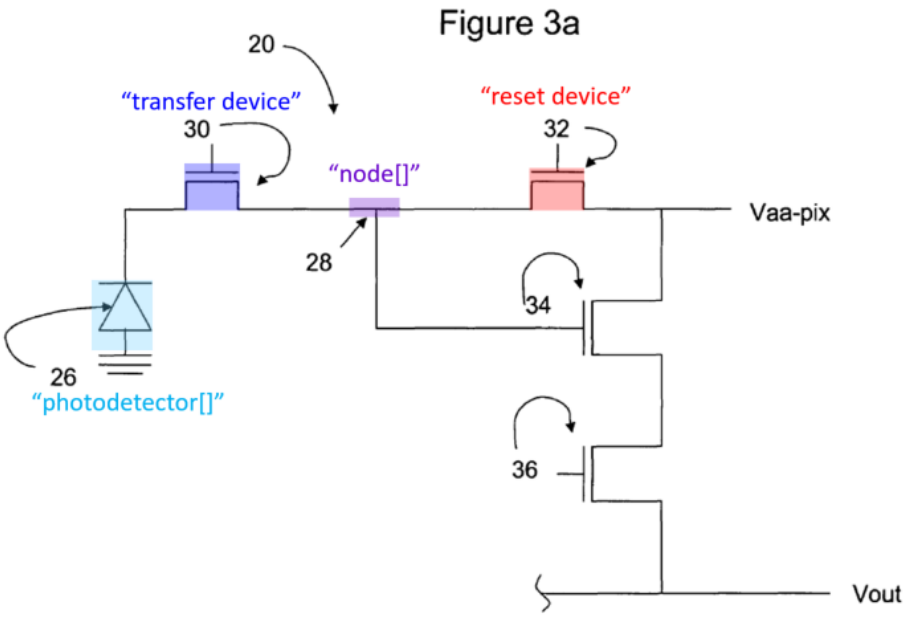
A POSITA would have had a reasonable expectation of success in implementing the halo implant 23 in *Rhodes-413* based on *Rhodes-042*'s teachings, which discloses a halo implant process that would have been readily understood and appreciated by such a POSITA, and given that both *Rhodes-413* and *Rhodes-042* share similar device structures, both including a punch-through protection implant. (Ex. 1002, ¶156; *compare* Ex. 1005, FIG. 9 *with* Ex. 1013, FIG. 5c.) The combination would have required nothing more than using well-known, rudimentary, and widely available techniques for an angled implant to realize the halo implant in *Rhodes-413* where the halo implant extends partially under the transfer gate 30. Indeed, using of angled halo implantation process was well-known. (Ex. 1002, ¶156; Ex. 1011, 834 (forming halo implants with a "high (30°) tilt angle"); Ex. 1012, 238-240 (disclosing "a large-angle tilt (LAT) implant of boron ions in NMOS…to form a halo-like structure.") Such a combination would not have detracted from the overall functionality of *Rhodes-413's* system, which would have continued to operate as described in *Rhodes-413*. (Ex. 1002, ¶156.)

Therefore, the *Rhodes-413-Kimura-Rhodes-042* combination discloses or suggests that halo implant 23 has a lateral position that is only partly under the transfer gate 30 highlighted in figure 9 of *Rhodes-413* ("each of the plurality of p-type regions has a lateral position only partly under the control terminal of a transfer device of the plurality of transfer device"). (Ex. 1002, ¶157.)

Lastly, as disclosed in Figures 9 and 11 of *Rhodes-413*, because the halo implant 23 is only positioned along the boundary where gate 24 (or transfer gate 30) and floating diffusion 28 meet, the halo implant 23 stops short of photosensor 426 and reset transistor 432. (Ex. 1002, ¶158; Ex. 1005, FIGs. 9, 11.) Accordingly, *Rhodes-413* discloses "the plurality of p-type regions has the lateral position stopping short of the plurality of photodetectors and stopping short of a plurality of reset devices." (*Id.*, ¶158.)

f) Claim 1[f]

Rhodes-413 in view of *Kimura* discloses or suggests this limitation. (Ex. 1002, ¶159.) As shown in figure 3a below, each pixel includes a reset transistor 32 connected to floating diffusion 28 ("node"). (Ex. 1005, FIG. 3a, 2:27-40.) Furthermore, *Rhodes-413* discloses that each reset transistor 32 resets its corresponding floating diffusion region 28 ("node") to a known potential "prior to transfer of charge from photosensor." (Ex. 1005, 2:38-40; *see also id.*, 1:27-37.)



(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶159.) In order to reset the node corresponding to floating diffusion region 28 to a known potential, a POSITA would have understood that reset transistor 32 would be turned on or "activated" such that a current path is created through the reset transistor 432 and the charges on the node 428 can be reset based on the power supply $V_{aa\text{-}pix}$. (Ex. 1002, ¶¶23-27, 159; Ex. 1005, 5:49-53 (disclosing that reset transistor can be turned on to drain out charges), 6:42-46.) Accordingly, *Rhodes-413* discloses that "each of the plurality of nodes is reset when the corresponding reset device is active." (Ex. 1002, ¶159.)

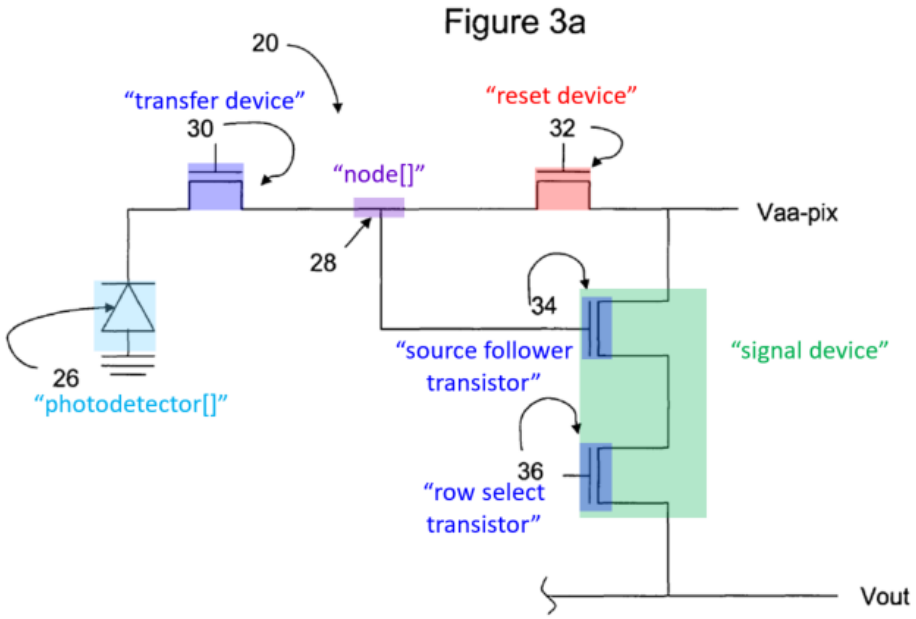
g) Claim 1[g]

Rhodes-413 in view of *Kimura* discloses or suggests this limitation. (Ex. 1002, ¶160.) For instance, pixel array 100 comprises pixels arranged in columns and rows, where the pixels of each row are controlled via a row select line by row

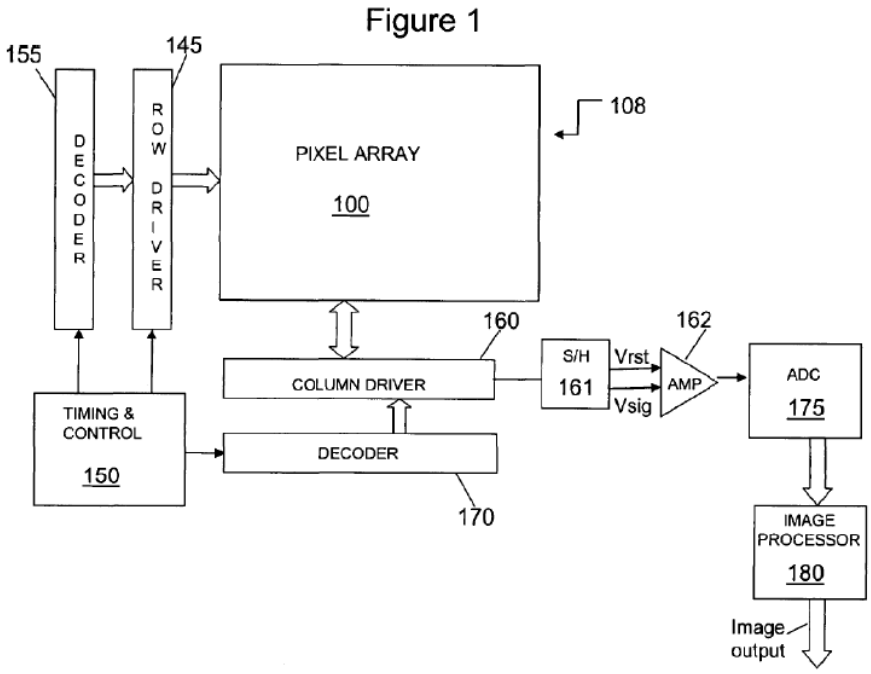
driver 145 in response to row address decoder 155, and the pixels of each column are controlled via column select lines by column driver 160 in response to column address decoder 170. (Ex. 1005, 1:38-51, FIG. 1; Ex. 1002, ¶160.)

h) Claim 1[h]

Rhodes-413 in view of *Kimura* discloses or suggests this limitation. (Ex. 1002, ¶161.) For example, as shown in figure 3a below, each pixel includes a source follower transistor 34 and a row select transistor 36 (together a "signal device" for each pixel and hence a "plurality of signal devices") coupled to floating diffusion region 28 ("node") where, when enabled, the row select transistor 36 outputs a signal for the pixel to a column line, where the signal is to be readout by the row and column circuitry (e.g., row/column drivers and decoders) shown in Figure 1. (Ex. 1005, FIG. 1, 2:28-38 ("**A floating diffusion region 28** receives charge from the photosensor 26 through the transfer gate 30 (when activated) and is connected to the reset transistor 32 and the **gate of the source follower transistor 34**. The source follower transistor 34 outputs a signal proportional to the charge accumulated in the floating diffusion region 28 to a sampling circuit when the **row select transistor 36** is turned on."), 7:54-55; *see also id.*, 1:16-19, 1:38-65, 2:35-38, 8:13-15.)



(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶161.)



(Ex. 1005, FIG. 1; Ex. 1002, ¶161.)

2. Claim 2

As discussed above in Section IX.B.1(d)(4), the *Rhodes-413-Kimura* combination discloses or suggests using p-type polysilicon as the transfer gate. (Ex. 1006, ¶¶[0131]-[0132], FIG. 8; Section IX.B.1(d)(4); Ex. 1002, ¶162.)

3. Claim 3

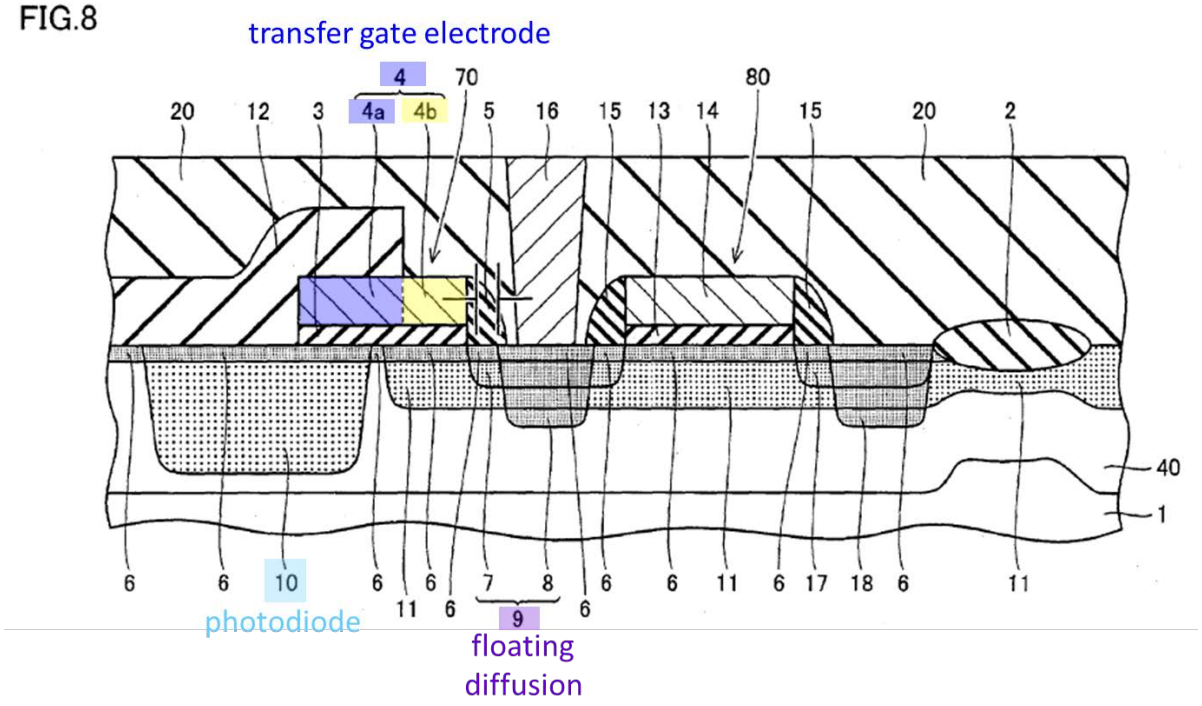
As discussed above in Section IX.B.1(d)(4), the channel ("body") and gate electrode 32 ("control terminal") in the *Rhodes-413-Kimura* combination have different work functions, where the difference in work functions creates an electric field. (*Supra* Sections IX.B.1(d)(4), IX.A.1(d)(4).) Given that the channel and the gate electrode have different work functions, a POSITA would have understood that they also have different Fermi levels (i.e., a first and second Fermi levels) because the work-function of a material is defined as the amount of energy required to remove an electron from the Fermi level of the material. (Ex. 1002, ¶¶28-37, 163; Ex. 1007, 5:1-4; Ex. 1010, 458-459.) Moreover, a POSITA would have understood that the difference between the Fermi level of the channel ("body") and the Fermi level of the graded p-type poly-silicon gate structure ("control terminal") causes the electric field. (Ex. 1002, ¶¶28-37, 163.)

4. Claim 5

As discussed above in Section IX.B.1(d)(4), the *Rhodes-413-Kimura* combination discloses or suggests using p-type polysilicon as the transfer gate

electrode having a doping concentration graded along the channel length of the body, similar to as shown in Figure 8 of *Kimura* below. (Ex. 1005, [0131]-[0132]; *Supra* Section IX.B.1(d)(4).) The transfer gate electrode has a low p-type concentration region (4b) and a high p-type concentration region (4a). (Ex. 1006, ¶¶[0131]-[0132]; *see also id.*, ¶¶ [0134]-[0136]; Ex. 1002, ¶164.)

FIG.8



(Ex. 1006, FIG. 8 (annotated); Ex. 1002, ¶164.)

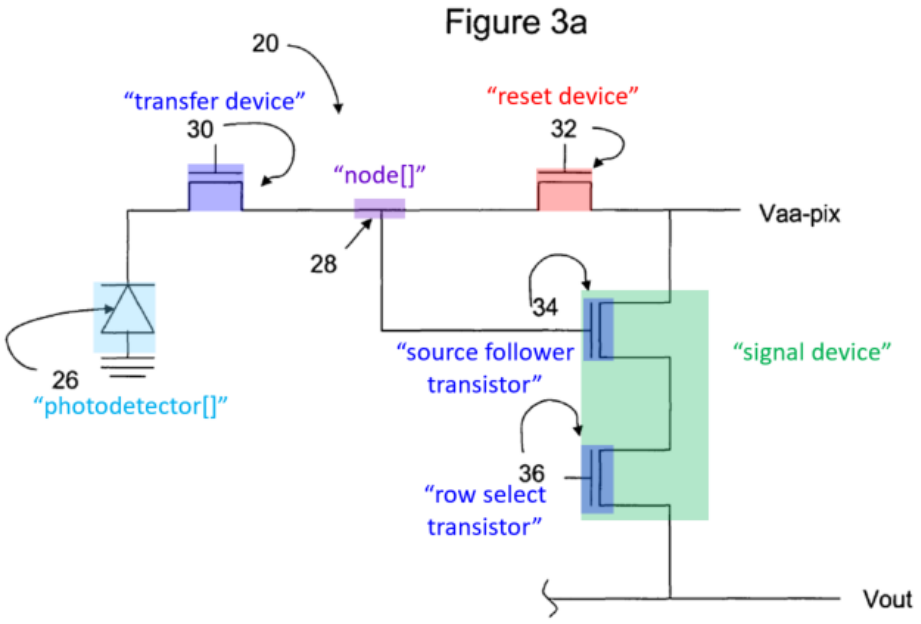
5. Claim 6

As discussed above in Section IX.B.1(d)(4), the *Rhodes-413-Kimura* combination discloses using p-type polysilicon for the transfer gate, which creates an electric field to repel electrons in the channel region of transfer device 30. (*Supra* Section IX.B.1(d)(4).) Given that dark current is caused by the thermal generation

of electrons, a POSITA would have understood that using such a p-type polysilicon gate would have reduced the dark current in the transistor channel as the created electric field repels electrons. (Ex. 1002, ¶165; Ex. 1014, 1:21-26.) This is consistent with the '145 patent's disclosure, which acknowledges that the use of p-type polysilicon gate electrode "eliminates dark current." (Ex. 1001, 2:13-17; Ex. 1002, ¶165.)

6. Claim 9

The *Rhodes-413-Kimura* combination discloses or suggests this limitation. (Ex. 1002, ¶166.) As discussed above in Section IX.B.1(h), *Rhodes-413* discloses that each pixel in the pixel array includes a "signal device" that includes a source follower transistor 34 and a row select transistor 36 ("plurality of signal devices") (*Supra* section IX.B.1(h).) As shown in annotated figure 3a below, the source follower transistor 34 for each pixel is coupled to the node 28 ("plurality of source follower transistors coupled to the plurality of nodes") and the row select transistor 36 for each pixel is to the output of the pixel, where, when enabled, transistor 36 outputs a signal for the pixel to a column line, where the signal is to be readout by the row and column circuitry (e.g., row/column drivers and decoders) shown in Figure 1. ("plurality of row select transistors coupled to the row and column circuitry"). (Ex. 1005, 2:28-38, 7:54-55; *see also id.*, 1:16-19, 1:38-65, 2:35-38; Ex. 1002, ¶166.)



(Ex. 1005, FIG. 3a (annotated); Ex. 1002, ¶166.)

7. Claim 10

As discussed above in Section IX.B.1(b), *Rhodes-413* discloses a plurality of photosensors ("photodetectors"). (Section IX.B.1(b).) *Rhodes-413* further discloses that each such photosensor may be "a photodiode." (Ex. 1005, 1:12-16, 2:41-43; Ex. 1002, ¶167.)

8. Claim 12

Claim 12 recites "a computer readable medium containing a description of an image sensor integrated circuit comprising" the limitations of claim 1. (*Compare* Ex. 1001, claim 12 *with* claim 1; Ex. 1002, ¶168.) As discussed in Section IX.B.1, the *Rhodes-413-Kimura-Rhodes-042* combination discloses or suggests the image

sensor integrated circuit of claim 1. For the same reasons discussed above in section IX.A.8 for the *Rhodes-647-Kimura* combination, a POSITA would have found it obvious to create a computer-readable description of the image sensor of the *Rhodes-413-Kimura-Rhodes-042*. (*Supra* section IX.A.8.) For example, A POSITA would have understood that the design and manufacture of semiconductor integrated circuits, like the image sensors disclosed in the *Rhodes-413-Kimura-Rhodes-042* combination, is typically performed using computer aided (CAD) tools that result in a design/description of the integrated circuits that would have been understood, in the context of the *Rhodes-413-Kimura-Rhodes-042* combination, as a "computer readable description of an image sensor integrated circuit." (Ex. 1002, ¶169; Ex. 1009, Abstract, 1:6-7, 4:33-44.) Accordingly, because the creation of a computer-readable description of the image sensor of the *Rhodes-413-Kimura-Rhodes-042* combination would have been obvious to a POSITA, the *Rhodes-413-Kimura-Rhodes-042* combination discloses or suggests all of the features of claim 12 for the same reasons discussed above in Section IX.B.1. (*Supra* section IX.B.1; Ex. 1002, ¶170.)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE HERE

The Board's decision in *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (Sept. 12, 2018) (precedential), does not apply here, because an evaluation of the six factors under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019,

Paper 11 (Mar. 20, 2020) (precedential), favor institution. As discussed below, while the '145 patent is involved in an ITC investigation, Petitioner diligently filed this Petition less than two months after institution of the ITC investigation, six of the eight challenged claims are not asserted in the ITC investigation, the ITC involves different evidentiary standards and burdens, and—most importantly—the ITC cannot invalidate a patent.[15] Accordingly, the Board should institute IPR based on the Petition, which presents strong arguments for unpatentability.

The **first factor (stay)** is neutral, because the ITC favors suspension of remedial orders that conflict with an IPR decision (e.g., issued near the end of an ITC investigation) over staying investigations at the onset. *See In the Matter of Certain Unmanned Aerial Vehicles and Components Thereof*, ITC-337-TA-1133, 2020 WL 5407477, at *1, *20-*22 (ITC Sept. 8, 2020).

The **second factor (proximity of trial)** is neutral, if not slightly for granting institution, because of Petitioner's diligence in filing the Petition. First, Petitioner

[15] Whether *NHK Spring* and *Fintiv* should apply to an ITC investigation was recently raised in a request for rehearing by the Board and the Precedential Opinion Panel in *Garmin Int'l, Inc. v. Koninklijke Philips N.V.*, IPR2020-00754, Paper 12 (Nov. 19, 2020).

filed its Petition ***less than two months*** after institution of the ITC investigation.[16] (Ex. 1018, 3.)

Second, the Board's institution decision will likely issue around July 2021, which is before the ITC's initial determination set for December 1, 2021 (Ex. 1023, 3). And, while the investigation hearing is set for August 16-20, 2021 (Ex. 1022, 1; Ex. 1023, 3) and the target completion date is set for April 1, 2022 (Ex. 1021, 2), those dates are "subject to change because of restrictions and uncertainty due to the COVID-19 pandemic" (*id.*, 2; Ex. 1022, 2). Indeed, the ITC has recently delayed a significant number of investigations in which a violation was found. (*See, e.g.*, Ex. 1024.)

Third, the hearing before the ALJ is merely the initial step in the ITC's decisional process. *See* 19 C.F.R. § 210.36(a). The ALJ's initial determination is subject to a review by the full Commission, which must issue a final determination. *Id.* §§ 210.43(d), 210.45-46. Additionally, if the Commission finds a violation, it must "transmit" a copy of its final determination and recommended actions (together with the full record) to the President, *see* 19 U.S.C. § 1337(j)(1)(B), and only upon the President's approval or the expiration of the 60-day presidential review period

[16] PO amended its complaint on October 23, 2020, and further supplemented it in November 2020. (Ex. 1018, 1.)

would the ITC's final determination become final (and subject to appeal), *see id.* § 1337(j)(4). Thus, even though the target completion date in the ITC Investigation is set to predate the Board's final written decision, the ultimate completion of the investigation will occur closer to and possibly after the Board's final written decision (per typical Commission extensions).

The **third factor (investment)** weighs in favor of institution. To date, the ITC investigation is in its infancy and thus the Commission and parties have not yet invested substantial resources. (Ex. 1023, 2; Ex. 1017.) While activity in the investigation will subsequently increase at a pace typical of ITC actions, Samsung's diligence in filing this Petition—***less than two months after investigation institution***—weighs against discretionary denial. (Ex. 1018, 2.) *See Philip Morris Prods., S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00919, Paper 9 at 10 (Nov. 16, 2020); *Fintiv*, Paper 11 at 11. Concluding otherwise would mean that this factor would always weigh against institution when there is a parallel ITC investigation because such investigations always require a rapid investment of resources at the outset.

The **fourth factor (overlap)** weighs strongly in favor of institution. Only claims 1 and 12 of the '145 patent remain at issue in the ITC investigation (Ex. 1017, 12; Ex. 1018, 2), so resolution of the investigation will not resolve the parties' dispute concerning patentability of the ***six*** other claims challenged in the Petition.

See Samsung Elecs. Co. Ltd. v. Dynamics Inc., IPR2020-00505, Paper 11 at 13 (Aug. 12, 2020).

Moreover, the ITC investigation does "not render [this] proceeding duplicative or … a waste of the Board's resources," because the ITC involves "differen[t] … evidentiary standards and burdens" and "does not have the authority to invalidate a patent." *Samsung Elecs. Co., Ltd. v. BitMicro, LLC*, IPR2018-01410, Paper 14 at 18 (Jan. 23, 2019); *see also Bio-Tech. Gen. Corp. v. Genentech, Inc.*, 80 F.3d 1553, 1564 (Fed. Cir. 1996) (The ITC cannot "set aside a patent as being invalid [and/or] render it unenforceable."). Indeed, even if the ITC finds any of the challenged claims invalid, PO can still assert those claims in district court. *See Renesas Elecs. Corp. v. Broadcom Corp.*, IPR2019-01040, Paper 9 at 7-8 (Nov. 13, 2019). That PO's predecessor unsuccessfully sued Samsung on invalid patents in the recent past strongly suggests it may do so again here. *See Imperium IP Holdings (Cayman) Ltd. v. Samsung Electronics Co., Ltd.*, 757 Fed. Appx. 974, 980 (Fed. Cir. 2019).

The **sixth factor (other circumstances)** likewise weighs strongly in favor institution. As demonstrated above (*supra* Section IX), the Petition presents strong arguments for unpatentability of the challenged claims. *See Dynamics*, Paper 11 at 14 (finding the "merits of the case weigh in favor" of institution). Thus, institution is consistent with the significant public interest against "leaving bad patents

enforceable." *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020). Indeed, this Petition is the ***sole*** challenge to the '145 patent before the Board—a "crucial fact" favoring institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (May 12, 2020). And there is currently no district court litigation to serve as an alternative forum that can issue a binding decision on the validity of the '145 patent.

Accordingly, based on a "holistic view of whether efficiency and integrity of the system are best served," the facts here weigh against exercising discretion under § 314(a) to deny institution. *Dynamics*, Paper No. 11 at 15. While factor 5 (parties) usually weighs against institution, the remaining factors are at least neutral (factors 1 and 2) or favor institution (factors 3, 4, and 6). Plus, the fact that this proceeding is not duplicative or a waste of the Board's resources (factor 4) and the strength of Petitioner's unpatentability positions (factor 6) outweigh other applicable factors, such as if the ITC investigation concludes before the final written decision is issued in this proceeding (factor 2) or if there were great investment in the ITC investigation (factor 3)—which typically occur when there is a parallel ITC investigation. *See 3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12 at 33-34 (May 26, 2020). Thus, institution here is proper.

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-3, 5, 6, 9, 10, and 12 of the ’145 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: January 15, 2021 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,800,145 contains, as measured by the word-processing system used to prepare this paper, 12,763 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: January 15, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on January 15, 2021, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,800,145 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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By: /Naveen Modi/
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